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**D E C I S I O N**
**of 9 November 1999**

**Case Number:** T 0225/94 - 3.4.3

**Application Number:** 87305165.0

**Publication Number:** 0250161

**IPC:** H01L 21/316

**Language of the proceedings:** EN

**Title of invention:**
Method of manufacturing devices including a semiconductor/dielectric interface

**Applicant:**
AT&T Corp.

**Opponent:**
-

**Headword:**
Ordered state of Dielectric layer/AT&T

**Relevant legal provisions:**
EPC Art. 56, 84, 54

**Keyword:**
"Novelty (after amendments) - yes"
"Inventive step - yes"
"Clarity - (functional features) - yes"

**Decisions cited:**
T 0068/85, T 0418/89, T 0104/93

**Catchword:**

**Case Number:** T 0225/94 - 3.4.3

**D E C I S I O N**
**of the Technical Board of Appeal 3.4.3**
**of 9 November 1999**

**Appellant:** AT&T Corp.
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NY 10013-2412 (US)

**Representative:** Watts, Christopher Malcolm Kelway, Dr.
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**Decision under appeal:** **Decision of the Examining Division of the European Patent Office posted 6 October 1993 refusing European patent application No. 87 305 165.0 pursuant to Article 97(1) EPC.**

**Composition of the Board:**

**Chairman:** R. K. Shukla
**Members:** G. L. Eliasson
A. C. G. Lindqvist

**Summary of Facts and Submissions**

I. European patent application No. 87 305 165.0 was refused by a decision of the examining division dated 4 October 1993 on the ground that the subject matter of claim 1 as originally filed lacked novelty having regard to the prior art document

D1: Patent Abstracts of Japan, vol. 7, No. 65, 18 March 1983 & JP-A-57 211 328.

In the decision under appeal, the examining division essentially argued that although in document D1 it was not explicitly stated that at least a monolayer of $SiO_2$ was in an ordered state, this must be the case, since an underlying silicon layer was formed on GaAs and was thus strained. Since according to one of the embodiments described in the application in suit, growth of an oxide layer on a strained silicon layer leads to the oxide having an ordered state at the interface between the two layers, it followed that the method disclosed in D1 necessarily resulted in a dielectric having at least a monolayer in an ordered state.

II. The appellant (applicant) lodged an appeal on 27 November 1993 and paid the appeal fee on 25 November 1993. The statement of the grounds of appeal was filed on 2 February 1994 along with new claims 1 to 16 and a translation of JP-A-57 211 328, which will be referred to as document D1a hereinafter.

The appellant essentially argued that document D1 concerned metal-insulator-semiconductor devices using

Group III-V semiconductor materials, and that the problem set out in D1 was entirely in terms of Group III-V semiconductor devices. The skilled person faced with a problem concerning Group IV semiconductor devices would not thus consider the teaching of document D1.

III. In response to communications from the Board, the appellant filed with the letters dated 7 May 1999, 7 September 1999, and 20 October 1999 new claims 1 and 14 and amended pages of the description. The appellant requested that the decision under appeal be set aside and a patent be granted on the basis of the following documents:

**Claims:** Claim 1 filed on 20 October 1999 with the letter of 20 October 1999
Claims 2 to 13, 15, and 16 filed with the statement of grounds of the appeal
Claim 14 filed on 10 September 1999 with the letter of 7 September 1999

**Description:** Pages 2 and 6 filed on 7 May 1999 with the letter of 7 May 1999
Pages 1, 3 to 5, 7, 8 as originally filed

**Drawings:** Sheets 1/2 and 2/2 as originally filed.

IV. Claims 1 to 3 and 14 of the above request read as follows:

"1. A Group IV semiconductor device comprising (i) a Group IV semiconductor material and (ii) a layer (25) comprising a dielectric compound of a

constituent element of said Group IV semiconductor material;

said layer having an interface with at least a region of a surface of said semiconductor material;

CHARACTERIZED IN THAT, at said interface, at least a monolayer of said dielectric compound is in an ordered state."

"2. The device according to claim 1, CHARACTERIZED IN THAT said ordered state is induced by an ordered state of said Group IV semiconductor material at said interface."

"3. The device of claim 2 in which said ordered state of said Group IV semiconductor material is induced by strain."

"14. A method for making a device according to claim 3, comprising the following steps:

(i) a step which results in the production of said strain in at least a portion of a surface layer of said Group IV semiconductor material, and subsequently

(ii) a step which results in the formation of said layer (25) comprising said dielectric compound whereby said interface is formed in at least a region of said portion of a surface layer of said Group IV semiconductor material, whereby at least a monolayer of said dielectric compound at said interface is in an ordered state."

## Reasons for the Decision

1. The appeal complies with Articles 106 to 108 and Rule 64 EPC and is therefore admissible.

2. *Amendments (Article 123(2) EPC)*

With respect to the claims, the present claims have been amended in that "semiconductor material" is replaced everywhere by "Group IV semiconductor material", and that present claim 1 is now directed towards "a Group IV semiconductor device" instead of "a semiconductor device."

The basis for the above restriction can be found on page 4, lines 16 to 21 and 28 to 33, as well as in Examples 1 to 5 described in the application as filed.

3. *Clarity and support of the claims (Article 84 EPC)*

In the decision under appeal, the only ground for the refusal of the application was that under Article 54(1) and 54(2) EPC. In the decision, however, it was also observed that independent claim 14 relating to a method did not comply with Article 84 EPC, since the statements in the claim that the first step "results in the production of said strain" and that the second step "results in the formation of a dielectric compound ... whereby at least a monolayer of said dielectric is in an ordered state" defined the method steps in terms of desired results to be achieved without specifying details of the method steps.

In a number of decisions, the boards of appeal have held that functional features defining a technical result to be achieved are permissible in a claim, if such features cannot otherwise be defined more precisely without restricting the scope of the invention, and if these features provide sufficient clear instructions to reduce them to practice (see, e.g. T 68/85, OJ EPO 1987, 228; T 418/89, OJ EPO 1993, 20; T 104/93, unpublished).

In the present case, it is evident from the prior art document "Physical Review Letters, vol. 55, No. 10, pages 1106 - 1109" referred to in the application in suit that techniques for producing strained semiconductor films by epitaxial growth on a substrate of dissimilar lattice constant are well-known in the art. Moreover, it is also disclosed in the application in suit (see page 3, line 33 to page 4, line 10) that the degree of lattice mismatch and thereby the resulting strain, can be adjusted by changing the composition of the Group IV semiconductor material and its thickness. Furthermore, it follows from the application in suit (see page 4, lines 11 to 27) that techniques such as molecular beam epitaxy or chemical vapour deposition which are employed in the application in suit for the formation of a dielectric layer on a substrate are per se well-known in the art. In the Board's view, therefore, the skilled person in the art would be in a position to carry out these method steps without any undue burden. Moreover, he would also be in a position to verify by the known diffraction techniques such as LEED, RHEED or transmission electron diffraction mentioned in the application in suit (see page 3, lines 23 to 30) whether or not the desired

results, i.e., a strained region and an ordered monolayer of the dielectric, were achieved. In the Board's opinion, therefore, claim 14 clearly defines the subject matter for which protection is sought.

4. *Novelty (Articles 52(1) and 54 EPC)*

Document D1, which the Board considers to be the closest prior art, discloses a semiconductor device comprising a substrate 1 made of a Group III-V semiconductor material, such as GaAs, a layer 2 made of Si formed on the substrate 1, an insulating layer 3 made of $SiO_2$ (cf. D1, abstract). As also pointed out in D1, due to the difference in lattice constants between the substrate 1 and the Si layer 2, the Si layer will be strained.

The purpose of the Si layer is to provide a defect-free interface between the semiconductor and the insulating layer in a device with an MIS structure (cf. D1, abstract, "Purpose"), since the interface between a Group III-V semiconductor and an oxide of the Group III-V compound contains many defects, thereby deteriorating the properties of the semiconductor device. The thickness of the Si layer 2 is limited to 1 to 5 atom layers in order to firstly prevent defect formation in the strained Si layer, and secondly, to prevent the conduction channel of the MOS to be formed in the Si layer. Otherwise, a Si-MOS on a III-V substrate would be produced instead of a MIS device made of III-V semiconductor (cf. D1a, page 3, lines 17 to 27).

Thus, in contrast to the Group IV semiconductor device

according to claim 1, the device of document D1 is to be regarded as a Group III-V semiconductor device, despite the fact that it comprises a layer made of silicon.

The subject matter of claim 1 is thus new within the meaning of Article 54 EPC.

5. *Inventive step (Articles 52(1) and 56 EPC)*

5.1 In relation to document D1, the problem which the present application seeks to solve can be regarded as reducing the number of defects at a semiconductor/insulator interface of a Group IV semiconductor device. The number of defects at the semiconductor/insulator interface is known in the art to be crucial for the performance of MOS devices, and therefore, the technical problem is as such well-known in the art.

5.2 Document D1 also describes a method for reducing defects at an semiconductor/insulator interface, but only in the context of Group III-V semiconductor materials which are known to have a very large density of interfacial surface defects (of the order of $10^{11}$ to $10^{12}$ $cm^{-2}$) at the semiconductor/insulator interface. The high number of interfacial surface defects is believed to be caused by the non-stoichiometry of the III-V compound at the interface and the non-stoichiometry of the oxide film itself at the interface (cf. D1, the paragraph bridging pages 1 and 2). In the detailed description of the invention in document D1a (see page 2, last paragraph of page 3), it is stated "Also, between the Si film 2 and $SiO_2$ film 3, a good interface

is obtained and the low interfacial level density of less than $10^{11}$ $cm^{-2}$ is realized." It thus follows from the teaching of document D1a that the insertion of a silicon layer between a III-V compound substrate and a $SiO_2$ layer reduces such a high level of interfacial defect density which is known to exist at the interface of a III-V compound semiconductor and an insulator. The interface between a Group IV semiconductor such as Si and an insulator such as $SiO_2$ is known to have a considerably lower defect density than the interface between a III-V compound and $SiO_2$. Consequently, it cannot be derived from the teaching of document D1 that the insertion of a layer of Si would reduce further the interfacial defect density in the case of a Group IV semiconductor substrate, which is known to be considerably low in comparison with that in a Group III-V compound semiconductor. Moreover, it cannot be derived that the measure taught in document D1a would lead to the formation of an ordered monolayer of $SiO_2$.

For the foregoing reasons, in the Board's opinion, it was not obvious to extend the teaching of document D1 to a Group IV semiconductor device.

5.3 The remaining documents cited in the search report, do not provide a hint leading to the claimed invention. Although it was known in the art that a 7x7 reconstruction is preserved at a buried amorphous-Si/Si(111) interface (cf. the application, page 2, lines 13 to 17), this reconstruction is not preserved at a Si/$SiO_2$ interface (cf. Example 3 of the present application).

For the foregoing reasons, in the Board's judgement, the subject matter of claim 1 involves an inventive step within the meaning of Article 56 EPC and therefore meets the requirements of Article 52(1) EPC. Claims 2 to 16 meet the requirements of Article 52(1) EPC as well, since they all contain the features of claim 1.

## Order

**For these reasons it is decided that:**

1. The decision under appeal is set aside.

2. The case is remitted to the department of the first instance with the order to grant a patent on the basis of the following documents:

**Claims:** Claim 1 filed on 20 October 1999 with the letter of 20 October 1999
Claims 2 to 13, 15, and 16 filed with the statement of grounds of the appeal
Claim 14 filed on 10 September 1999 with the letter of 7 September 1999

**Description:** Pages 2 and 6 filed on 7 May 1999 with the letter of 7 May 1999
Pages 1, 3 to 5, 7, 8 as originally filed

**Drawings:** Sheets 1/2 and 2/2 as originally filed.

The Registrar: The Chairman:

D. Spigarelli R. K. Shukla