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D E C I S I O N
of 5 November 1998

Case Number: T 0158/94 - 3.4.1

Application Number: 85401583.1

Publication Number: 0174236

IPC: G01R 31/28

Language of the proceedings: EN

Title of invention:
Semiconductor integrated circuit device having a test circuit

Patentee:
Fujitsu Limited

Opponent:
CrossCheck Technolgy, Inc.

Headword:
-

Relevant legal provisions:
EPC Art. 100(a), 52(1), 54, 56, 104(1)

Keyword:
"Inventive step - main and auxiliary requests (no)"
"Costs - apportionment (no)"

Decisions cited:
T 0572/88, T 0763/89, T 0117/86

Catchword:
-

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Case Number: T 0158/94 - 3.4.1

D E C I S I O N
of the Technical Board of Appeal 3.4.1
of 5 November 1998

Appellant: (Proprietor of the patent)	Fujitsu Limited 1015, Kamikodanaka Nakahara-ku Kawasaki-shi Kanagawa 211 (JP)
Representative:	Descourtieux, Philippe Cabinet Beau de Loménie 158, rue de l'Université 75340 Paris Cédex 07 (FR)
Respondent: (Opponent)	CrossCheck Technology, Inc. 2833 Junction Ave., Suite 100 San Jose, California 95134 (US)
Representative:	Morgan, James Garnet Manitz, Finsterwald & Partner Patentanwälte Postfach 22 16 11 80506 München (DE)
Decision under appeal:	**Decision of the Opposition Division of the European Patent Office posted 24 January 1994 revoking European patent No. 0 174 236 pursuant to Article 102(1) EPC.**

Composition of the Board:

Chairman: G. Davies
Members: G. Assi
R. K. Shukla

Summary of Facts and Submissions

I. The appellant (patent proprietor) lodged an appeal, received on 18 February 1994, against the decision of the Opposition Division, dispatched on 24 January 1994, revoking the European patent No. 0 174 236 (application No. 85 401 583.1). The fee for the appeal was paid on 18 February 1994. The statement setting out the grounds of appeal was received on 30 May 1994.

Opposition was filed against the patent as a whole and was based on Article 100(a) EPC, in particular on the grounds that the subject-matter of the patent was not patentable within the terms of Articles 52(1), 54 and 56 EPC.

The Opposition Division held that the grounds of the opposition prejudiced the maintenance of the patent, having regard to the following documents:

(D1) IBM Technical Disclosure Bulletin, Vol. 18, No. 7, December 1975, "Test pad multiplexing" by D.K. Jadus et al.,

(D4) Article "Testing VLSI with random access scan" by H. Ando, COMPCON80 Conference, 25 to 28 February 1980, San Francisco (CA), published by IEEE under No. CH1491-0/80/0000-0050, 1980, pages 50 to 52, and

(D5) Article "Design for testability - a survey" by T.W. Williams et al., reprinted from Proceedings of the IEEE, Vol. 71, No. 1, January 1983, pages 98 to 112.

II. Documents D4 and D5 were filed by the respondent (opponent) during the opposition procedure with the letter of 13 January 1993 after the expiry of the nine-month opposition period.

III. The appellant requested that the decision under appeal be set aside and that the patent be maintained on the basis of the following documents:

Main request:
Claim 1 as filed with the letter of 5 October 1993,
Claims 2 to 9, columns 1 to 8, drawings 1/7-7/7 of the granted patent,

First auxiliary request:
Claim 1 as filed with the letter of 5 October 1998,
Claims 2 to 9, columns 1 to 8, drawings 1/7-7/7 of the granted patent,

Second auxiliary request:
Claim 1 as filed with the letter of 5 October 1998,
Claims 2 to 9, columns 1 to 8, Drawings 1/7-7/7 of the granted patent,

Third auxiliary request:
Claim 1 as filed with the letter of 5 October 1998,
Claims 2 to 9, columns 1 to 8, Drawings 1/7-7/7 of the granted patent,

Fourth auxiliary request:
Claims 1 to 9 as filed during the oral proceedings on 5 November 1998,
columns 1 to 8, drawings 1/7-7/7 of the granted patent,

Fifth auxiliary request:
Claims 1 to 9 as filed during the oral proceedings on 5 November 1998,
columns 1 to 8, drawings 1/7-7/7 of the granted patent.

Furthermore, the appellant requested:

- apportionment of costs on the ground that the respondent filed documents D4 and D5 during the opposition proceedings after the expiry of the period for opposition, and

- oral proceedings in the event that the above-mentioned requests were not granted.

IV. The respondent requested that the appeal be dismissed. Furthermore, he requested oral proceedings, as an auxiliary request.

V. The wording of **Claim 1** according to the **main request** reads as follows:

"1. A semiconductor integrated circuit chip comprising:
a plurality of gate cells (2) arranged in a matrix;
wiring means (DW) for connecting the gate cells (2) so as to constitute a logic circuit;
a test circuit comprising a plurality of row and column wires (3, 4) for selecting and reading out any gate cell to be tested,
characterized in that the selection wires are row selection wires (3) provided along said gate cells in a row direction and the read-out wires are column selection wires (4), provided along said gate cells in a column direction, and that the test circuit further comprises a plurality of switching means (5) located in the gate cell area and arranged in a matrix, the output of each gate cell (2) in a column direction being connected to a corresponding column read-out wire (4) through a switching means (5) and all switching means in a row direction being connected to a corresponding row selection wire (3) for turning ON/OFF these switching means and, thereby, connecting (ON state) or

disconnecting (OFF state) the respective gate cell outputs and the corresponding column read-out wire,
row selection means (9, 6) are connected to said row selection wires (3), for selecting any of said row selection wires and, thereby, said switching means (5) connected to said selected row selection wire and the corresponding gate cells (2), said row selection means having a function of turning OFF all switching means each provided between the output of a gate cell and the corresponding column read-out wire, in a non-test mode, and
output means (7, 8, 11) are provided for reading out any of said selected gate cells (2) arranged in said logic circuit through a corresponding column read-out wire (4)."

The wording of **Claim 1** according to the **first auxiliary request** has the following wording (amendments with respect to Claim 1 of the main request are underlined):

"1. A semiconductor integrated circuit chip comprising:
a plurality of gate cells (2) arranged in a matrix;
wiring means (DW) for connecting the gate cells (2) so as to constitute a logic circuit to be tested;
a test circuit comprising a plurality of row and column wires (3, 4) for selecting and reading out any gate cell to be tested,
characterized in that the selection wires are row selection wires (3) provided along said gate cells in a row direction, two adjacent rows of gate cells being separated by a row selection wire (3) and the read-out wires are column selection wires (4), provided along said gate cells in a column direction, two adjacent columns of gate cells being separated by a column selection wire, and that the test circuit further comprises a plurality of switching means (5), formed on a same bulk as the gate cells (2) and arranged in a

matrix, each of said switching means being located in a gate cell area and <u>being provided at an intersection of a row selection wire and a column selection wire</u>, the output of each gate cell (2) in a column direction being connected to a corresponding column read-out wire (4) through a switching means (5) and all switching means in a row direction being connected to a corresponding row selection wire (3) for turning ON/OFF these switching means and, thereby, connecting (ON state) or disconnecting (OFF state) the respective gate cell outputs and the corresponding column read-out wire,
row selection means (9, 6) are connected to said row selection wires (3), for selecting any of said row selection wires and, thereby, said switching means (5) connected to said selected row selection wire and the corresponding gate cells (2), said row selection means having a function of turning OFF all switching means each provided between the output of a gate cell and the corresponding column read-out wire, in a non-test mode, and
output means (7, 8, 11) are provided for reading out any of said selection gate cells (2) arranged in said logic circuit through a corresponding column read-out wire (4)."

The wording of **Claim 1** according to the **second auxiliary request** reads as follows (amendments with respect to Claim 1 of the first auxiliary request are underlined):

"1. A semiconductor integrated circuit chip comprising:
a plurality of gate cells (2) arranged in a matrix;
wiring means (DW) for connecting the gate cells (2) so as to constitute a <u>combinational</u> logic circuit to be tested;
a test circuit comprising a plurality of row and column

wires (3, 4) for selecting and reading out any gate cell to be tested,
characterized in that the selection wires are row selection wires (3) provided along said gate cells in a row direction, two adjacent rows of gate cells being separated by a row selection wire (3) and the read-out wires are column selection wires (4), provided along said gate cells in a column direction, two adjacent columns of gate cells being separated by a column selection wire, and that the test circuit further comprises a plurality of switching means (5), formed on a same bulk as the gate cells (2), but not forming part of the logic circuit to be tested, and arranged in a matrix, each of said switching means being located in a gate cell area and being provided at an intersection of a row selection wire and a column selection wire, the output of each gate cell (2) in a column direction being connected to a corresponding column read-out wire (4) through a switching means (5) and all switching means in a row direction being connected to a corresponding row selection wire (3) for turning ON/OFF these switching means and, thereby, connecting (ON state) or disconnecting (OFF state) the respective gate cell outputs and the corresponding column read-out wire,
row selection means (9, 6) are connected to said row selection wires (3), for selecting any of said row selection wires and, thereby, said switching means (5) connected to said selected row selection wire and the corresponding gate cells (2), said row selection means having a function of turning OFF all switching means each provided between the output of a gate cell and the corresponding column read-out wire, in a non-test mode, and
output means (7, 8, 11) are provided for reading out any of said selection gate cells (2) arranged in said logic circuit through a corresponding column read-out wire (4)."

The wording of **Claim 1** according to the **third auxiliary request** corresponds to that of Claim 1 of the second auxiliary request with the further feature that the semiconductor circuit chip is an "LSI" circuit chip.

The wording of **Claim 1** according to the **fourth auxiliary request** reads as follows:

"1. A method for testing a LSI semiconductor integrated circuit chip, said circuit chip comprising:
a plurality of gate cells (2) arranged in a matrix;
wiring means (DW) for connecting the gate cells (2) so as to constitute a logic circuit to be tested;
a test circuit comprising a plurality of row and column wires (3, 4) for selecting and reading out any gate cell to be tested,
the selection wires being row selection wires (3) provided along said gate cells in a row direction, two adjacent rows of gate cells being separated by a row selection wire, and the read-out wires being column selection wires (4), provided along said gate cells in a column direction, two adjacent columns of gate cells being separated by a column selection wire, the test circuit further comprising a plurality of switching means (5), formed on a same bulk as the gate cells and arranged in a matrix, located in a gate cell area and being provided at an intersection of a row selection wire and a column selection wire, the output of each gate cell (2) in a column direction being connected to a corresponding column read-out wire (4) through a switching means (5) and all switching means in a row direction being connected to a corresponding row selection wire (3) for turning ON/OFF these switching means and, thereby, connecting (ON state) or disconnecting (OFF state) the respective gate cell outputs and the corresponding column read-out wire,
row selection means (9, 6) being connected to said row selection wires (3), for selecting any of said row

selection wires and, thereby, said switching means (5) connected to said selected row selection wire and the corresponding gate cells (2), said row selection means having a function of turning OFF all switching means each provided between the output of a gate cell and the corresponding column read-out wire, in a non-test mode, and
output means (7, 8, 11) being provided for reading out any of said selected gate cells (2) arranged in said logic circuit through a corresponding column read-out wire (4),
said method comprising:
selecting a row selection wire with said row selection means (9, 6), during a logic operation of said circuit chip, thereby selecting the switching means connected to said selected row selection wire and the corresponding gate cells,
reading out any of said selected gate cells through a corresponding column read-out wire (4) with said output means, thus monitoring said gate cell in real time during a logic circuit operation of said circuit chip."

The wording of **Claim 1** according to the **fifth auxiliary request** corresponds to that of Claim 1 of the fourth auxiliary request with the further feature that the wiring means (DW) is for connecting the gate cells (2) so as to constitute a "combinational" logic circuit to be tested.

Claims 2 to 9 according to **all the requests** are dependent claims.

VI. The appellant's arguments may be summarised as follows.

As regards substantive matters:

Document D4 discloses the testing of a VLSI circuit. Figure 3 shows a well-known structure including a combinational portion together with a sequential portion which comprises addressable latches (see Figures 1 and 2) used as storage elements. In the art, testing of combinational circuits is not problematic. A controlled signal is introduced into the combinational circuit and an output signal is observed, from which a conclusion may be drawn about the operation of the circuit as a whole. A much more difficult problem is testing the sequential part of the circuit, because the outputs depend not only on the present inputs, but also on the past inputs. D4 solves this problem by a random access scan technique, according to which each latch, which actually belongs to the sequential circuit, is transformed into a "combinational element", but only from the testing point of view. In other words, any element of the circuit of Figure 3 can be considered as a combinational element, for testing purposes. The combinational portion is thus tested as a whole, with usual methods, whereas each element (latch) of the sequential portion is tested by adding one additional gate (see the gate with output -SDO in Figures 1 and 2) and by addressing the latch. The sentence on page 51, left-hand column, "Any point in <u>combinational circuits</u> (emphasis added) can be observed with one additional gate and one address, while shift approach requires two latches for every point.", has to be interpreted, therefore, in the light of the above explanation. It is clear that the expression "shift approach" means the technique mentioned on page 50, right-hand column, lines 13 to 16, and described in D5 (see page 316, point IV.A). According to D4, there is a functional relation between the gates of the combinational circuit

and the addressable latches, but certainly not a structural one. The problem solved by this document is absolutely not the one of testing the combinational circuit or a test point in this circuit, but is much more the one of testing latches like combinational elements, although they are per nature sequential elements. In this way, testing in real time is not possible.

Document D5 essentially corresponds to D4.

Document D1 discloses a testing device comprising an array of field effect transistors which are addressed by a decoder and by input/output pads S_i. The decoder involves multiplexing for selecting various row selection wires. Column wires are connected to pads S_i. D1 cannot be considered as the closest prior art and is not concerned with the problem of testing the gate cells of a logic circuit of LSI type. There is no reason to believe that this document implicitly discloses a semiconductor integrated circuit chip to be tested comprising a matrix of gate cells connected with wiring means. The skilled person would just install the device of D1 over a circuit to be tested, but would not integrate each FET with the circuit to be tested. Indeed, the technology disclosed by D1 is concerned with SSI devices, i.e. it is not applicable to LSI or VLSI technologies.

Thus, the claimed subject-matter according to all the requests is novel and inventive, having regard to any of documents D4, D5 or D1, each taken alone. Moreover, it is not possible to combine the documents, as far as inventive step is concerned. In particular, the skilled person, starting from D4 or D5, would not look for a solution in D1, because this document does not refer to any memory elements, which are the object of D4 and D5.

As regards apportionment of costs:

The request for apportionment of costs is justified by the fact that the late submission of the documents D4 and D5 has not been motivated by the respondent. Moreover, it appears to be totally unjustified.

VII. The respondent's arguments may be summarised as follows.

As regards substantive matters:

Document D1, taken alone, is particularly relevant. It is clear to the skilled person that D1 implicitly discloses a circuit device intended for testing integrated circuits. This results from the publication date of the document and from the terminology used, in particular terms like "chip", "kerf" or "multiplexing" which are usual in IC technology. D1 discloses a test circuit comprising a plurality of row and column wires as well as a matrix of field-effect transistors acting as switching means. These transistors are intended for connection to the gate cells of a logic circuit, which, although not expressly shown, is the object of the test by the circuit disclosed. The test circuit allows each node of the gate array to be tested. In particular, D1 enables a greater number of test points to be accessed from a limited number of test side pads. Considering that, according to the patent in suit, only the structure of the test circuit matters, it is irrelevant that D1 does not disclose in detail the actual circuits to be tested. D1, in general, shows the concept of accessing any point in a circuit on a semiconductor substrate, whether it is a chip or a wafer, and whether or not the tested device is an independent circuit, a gate cell, a gate array, or a point in an interconnected circuit.

Document D4 is concerned with VLSI circuits and the testing thereof. Figure 3 shows a schematic diagram of the circuit comprising the combinational circuit, i.e. the portion of the logic circuit comprising gates interconnected with wiring means, and addressable storage elements (latches) associated therewith. Figure 3 would be understood by the skilled person as meaning that the addressable storage elements overlay the logic gates of the combinational circuit rather than being physically separate. X and Y decoders are provided to select individual latches via X and Y wires. The teaching according to D4 is that one should associate a switching means with a point to be observed in a combinational circuit, i.e. an array of gate cells which are interconnected to form a logic circuit, and should address these switching means through X and Y lines to read-out the state of any observed point in the combinational circuit during operation.

Document D5 comprises the same disclosure as D4.

Reasons for the Decision

1. The appeal is admissible.

2. *Amendments*

The Board is satisfied that the amended claims according to all the requests meet the requirements of Article 123(2),(3) EPC. The respondent has not raised any objection in this respect.

3. *Novelty*

3.1 Document D1

D1 is concerned with the problem of evaluating "semiconductor products", monitoring "product performance", and diagnosing "device and circuit failures". These expressions are quite general. Nevertheless, the skilled person understands that, in particular, D1 solves the problem of testing semiconductor integrated circuit devices, because the terminology used is specific for the IC technology (see terms like "chip" and "kerf"), the development of which had already reached the LSI level at the publication date of D1, as the respondent points out in his letter of 13 January 1993, page 3, third paragraph. According to D1, first paragraph, test site chips and kerfs were normally used, which however had the disadvantage of a limited number of test pads available for external connections to the devices and circuits contained on the chips. Thus, D1 discloses the solution of multiplexing a limited number of pads to a greater number of device or circuit test points than could normally be accommodated through fixed access. In particular, the Figure shows a matrix of addressable field-effect transistors acting as switching means, row selection wires, column wires acting as read-out wires, row selection means, and reading-out means.

In D1 there is no specific disclosure of the actual devices or circuits to be tested. In the notice of opposition of 12 April 1990, pages 7 and 8, points (b) and (c), the respondent argues that a logic circuit comprising a matrix of gate cells connected by wiring means forms part of the implicit disclosure of D1. The Board holds that, even though the skilled person will understand that a logic circuit contained on a chip

comprises gate elements which are somehow interconnected, D1 however fails to disclose the feature that the test circuit and the circuit to be tested are arranged in the same semiconductor IC chip, as recited in Claim 1 according to all the requests, and also the claimed structural relationship between the two circuits. In this respect, attention is drawn to the warning, expressed in decisions T 572/88 and T 763/89, against using the concept of "implicit prior description" in such a way that considerations relevant to the evaluation of inventive step are transferred to the assessment of novelty.

Therefore, the subject-matter of Claim 1 according to all the requests is novel, having regard to D1.

3.2 Document D4

D4 is concerned with the problem of VLSI testing which is solved by a random-access scan technique. The basic concept consists in reducing a given logic circuit, which is usually sequential, to a combinational one by logically eliminating all storage elements (see page 50, right-hand column, second sentence). An addressing scheme allows each storage element (latch) of the circuit to be uniquely selected, so that it can be tested. Suitable addressable latches are shown in Figures 1 and 2, whereas the overall view of the system configuration is shown in Figure 3. Basically, besides the combinational circuit the system comprises X-address means, Y-address means, the addressable storage elements, system clear and clock functions, the test input SDI, and the output SDO corresponding to the signals -SDO from all latches ANDed together.

Thus, D4 does not disclose a test circuit according to Claim 1 of all the requests, which allows testing each gate cell of the logic circuit. Indeed, in D4 only the elements of the sequential portion are addressed, whereas the combinational circuit is conventionally tested as a whole by providing test inputs and controlling the outputs obtained.

Therefore, the subject-matter of Claim 1 according to all the requests is novel, having regard to D4.

3.3 Document D5

The disclosure of document D5 (see point IV.D) essentially corresponds to that of D4, so that novelty is acknowledged also having regard to this document.

4. *Inventive step*

4.1 Main request

4.1.1 Claim 1 refers to a semiconductor IC chip comprising a logic circuit and a test circuit. The logic circuit comprises a matrix of gate cells connected by wiring means. The test circuit comprises a matrix of switching means located near the gate cells, row selection wires, column read-out wires, row selection means and reading-out means. The switching means arranged in a row direction connect (ON state) or disconnect (OFF state) respective gate cell outputs and corresponding column read-out wires.

4.1.2 In his letter of 5 October 1998, point VI.1, the appellant contends that D1 cannot be regarded as the closest prior art because it is not concerned with the same problem as the patent in suit. Moreover, the structural similarities between the known system, which

shows row and column wires, FETs being located at the intersections thereof, and the claimed chip are of a purely superficial nature. According to the appellant (see point VI.2 of the cited letter), the choice of D5 (or D4) as the closest prior art would be more "logical" than the choice of D1.

On the contrary, the respondent is of the opinion that D1 is indeed relevant because, considering its publication date, it concerns, as a particular case, the testing of gate cells connected in a logic integrated circuit (see the letter of 26 June 1991, page 6, second sentence). Moreover, it shows a row/column test circuit to be associated to devices and circuits included in semiconductor products (see the same letter, page 7, first sentence). The respondent maintained this view during the oral proceedings on 5 November 1998.

The Board draws attention to the following considerations as regards the choice of the document reflecting the closest state of the art.

At the publication date of D1, i.e. December 1975, integrated circuits were known. According to the respondent (see the letter of 13 January 1993, page 3, second and third paragraphs), the development had reached, at that time, the level of large scale integration (LSI), which corresponds to that of the circuit to be tested according to the patent in suit (see the description, column 1, lines 5 to 9, column 2, lines 21 to 24). It is noted, in this respect, that the development time frame presented by the respondent is not contested by the appellant. In view of this, the Board holds that the test circuit shown in D1 may well take the form of an integrated circuit and, moreover, be used for testing integrated circuits of LSI type. This interpretation is indeed supported by the

terminology used in D1. In particular, according to the first sentence, "test site chips and kerfs" are used to evaluate "semiconductor products" and to diagnose "devices and circuit failures". As the respondent points out in the letter of 26 June 1991, page 5, end of point 1, a "kerf" is the region between adjacent ICs on a wafer, which is frequently used for test circuitry. Thus, the skilled person will understand that, in particular, D1 refers to the diagnostics of integrated circuits and, moreover, that the test circuit itself, as shown on the first page, can be an integrated circuit on a chip.

As regards D4 (or D5), in the circuit shown in Figure 3, there is no structural correspondence between a gate of the combinational part and a latch of the sequential part. During operation of the circuit as a whole, both parts exchange information, but the number of gates of the combinational part has nothing to do with the number of latches involved in the sequential part. In other words, the relation between both parts is functional, not structural. Therefore, it is not possible to monitor each gate cell of the circuit. Moreover, the solution disclosed in D4 does not need the plurality of switching means, which are necessary, according to the patent in suit, for selecting the gates to be tested. D4 solves the testing problem in a different way. The combinational circuit is tested as a whole with usual methods, i.e. a test input is introduced and the output is observed, whereas each latch of the sequential circuit is transformed into a combinational element, from the point of view of testing. This is achieved by providing one additional gate in each latch (see the gate with output -SDO in Figures 1 and 2) and by addressing the latch (see inputs X-ADR and Y-ADR in Figure 1 and 2). The method disclosed in D4 is thus advantageous as compared with other solutions like the shift approach, which requires

two latches for every test point (see D4, page 51, left-hand column, sentence "Any point in combinational circuits ... two latches for every point.", and D5, page 320, left-hand column, first paragraph, Figure 10(a)). A further difference consists in that the latch state -SDO signals from all latches are ANDed together to produce the chip scan out signal SDO (see Figure 3).

Therefore, the solution known from D4 is basically different from that according to the patent in suit.

For these reasons, the Board considers document D1 as the closest state of the art. As stated above, the document discloses a test circuit on a chip, suitable for testing LSI circuits. The disclosure of D1, however, does not comprise any feature concerning the products, devices and circuits to be tested. In other words, compared to Claim 1 of the main request, D1 does not disclose the claimed arrangement of the test and logic circuit on the same chip, the specific features concerning the logic circuit to be tested, and the structural relationship with the test circuit (see the appellant's letter dated 5 October 1998, page 14/18). In order to assess inventive step with regard to Claim 1, the following questions should then be considered in the light of the disclosure of D1 as understood by the skilled person with his technical knowledge:

(i) whether or not the claimed features of the logic circuit as such are commonly known in the art,

(ii) whether or not, in the frame of the LSI technology, it would be obvious to integrate the logic circuit and the test circuit on the same chip, and

(iii) whether or not the claimed features concerning the structural relationship between the two circuits are usual.

With regard to question (i), in the Board's view, logic circuits comprising a matrix of gate cells interconnected by wiring means are generally known in the art.

As regards question (ii), the appellant contended that a LSI circuit has such a high density of gates that it would be difficult to integrate further elements belonging to the test circuit, i.e. the row/column wires and the plurality of switching means (see the letter of 5 October 1998, point VI.B.5 on pages 15/18 and 16/18). In this respect, the Board draws attention to the fact that the test circuit according to D1 is, as stated above, suitable for LSI applications, and not for SSI devices, as the appellant points out in the cited paragraph. This means that such an integration might be difficult but not impossible. In other words, there was no technical reason which would have prevented the skilled person from the integration of the logic circuit in the same chip as the test circuit. Moreover, Claim 1 does not mention any measure specifically allowing the integration. The Board holds that the claimed arrangement of the test circuit elements with respect to those of the logic circuit should not be seen as the solution to the integration problem, but rather as the obvious result of the need to interconnect the gate cells with the switching means and to select a given gate cell with the row/column wires. Question (iii) is thus also answered.

In view of the foregoing, the Board comes to the conclusion that the structure of the chip according to Claim 1 of the main request results from normal design considerations of the skilled person, who would analyse the possible applications of the test system disclosed in D1 within the context of his routine activities.

Therefore, the subject-matter of Claim 1 of the main request does not involve an inventive step, having regard to D1 alone.

4.2 First auxiliary request

Claim 1 according to the first auxiliary request essentially differs from Claim 1 of the main request in that it comprises further features of a topological nature. In particular, two adjacent rows (columns) of gate cells are separated by a row (column) selection wire, and each of the switching means is provided at an intersection of a row selection wire and a column selection wire. Moreover, the plurality of switching means is formed on a same bulk as the gate cells.

The first two features mentioned are obvious for the skilled person. The test circuit known from D1 comprises FETs (acting as switching means) which are provided at the intersections of the row selection wires and the column selection wires. Since the FETs should be connected to the gate cells of the circuit to be tested, it is obvious from a design point of view to arrange the gate cells in such a way that two adjacent rows (columns) of gate cells are separated by a row (column) selection wire. Moreover, the feature that the switching means is formed on a same bulk as the gate cells is an obvious specification of the feature that both the test circuit and the logic circuit are arranged on the same chip.

Therefore, the subject-matter of Claim 1 of the first auxiliary request does not involve an inventive step, having regard to D1 alone.

4.3 Second auxiliary request

As compared to Claim 1 of the first auxiliary request, Claim 1 according to the second auxiliary request further comprises the features that the logic circuit is combinational, and that the plurality of switching means does not form part of the logic circuit to be tested.

Whereas the first feature is trivial, the second one is part of the disclosure of D1. While testing a circuit with the circuit of D1, the FETs do not form part of the logic circuit to be tested.

Therefore, the subject-matter of Claim 1 of the second auxiliary request does not involve an inventive step, having regard to D1 alone.

4.4 Third auxiliary request

Claim 1 according to the third auxiliary request differs from Claim 1 of the second request in that the chip comprises a LSI circuit.

As already stated above, the system known from D1 is suitable for testing LSI circuits.

Therefore, the subject-matter of Claim 1 of the third auxiliary request does not involve an inventive step, having regard to D1 alone.

4.5 Fourth auxiliary request

Claim 1 of the fourth auxiliary requests relates to a method for testing a LSI semiconductor integrated circuit chip, the chip comprising the features recited in Claim 1 according to the first auxiliary request. The method essentially consists in selecting a row wire with the row selection means, thereby activating the switching means connected to the selected row wire, and reading-out any of the selected gate cells through a corresponding column read-out wire, the gate cells being thus monitored in real time.

The same steps can be inferred from D1. The solution disclosed in this document consists in multiplexing a limited number of kerf or test site pads to a greater number of circuit or device test points than could normally be accommodated through fixed access (see second paragraph). Multiplexing is accomplished by employing decoders or shift registers to act as switches for access to many test points from a limited number of external test pads (see third paragraph). Thus, in order to activate the FET located near the gate cell to be tested and connected to this cell, the corresponding row wire is multiplexed and the output of the gate cell is read-out by means of the corresponding column wire connected to the I/O pad. The gate cell can thus be monitored in real time.

Therefore, the subject-matter of Claim 1 of the fourth auxiliary request does not involve an inventive step, having regard to D1 alone.

4.6 Fifth auxiliary request

As compared to Claim 1 of the fourth auxiliary request, Claim 1 according to the fifth auxiliary request further comprises the feature that the logic circuit is combinational. This feature is trivial.

Therefore, the subject-matter of Claim 1 of the fifth auxiliary request does not involve an inventive step, having regard to D1 alone.

5. In view of the foregoing, none of the appellant's requests concerning the maintenance of the patent in amended form is allowable.

6. *Apportionment of costs*

Under Article 104(1) EPC each party to the proceedings shall meet its own costs. However, for reasons of equity, the opposition divisions or boards of appeal may order a different apportionment of costs incurred during taking of evidence or in oral proceedings. Article 117(1) EPC makes it clear that the expression "taking of evidence" covers the case of producing evidence in proceedings before the EPO, whatever the form of such evidence, including, in particular, the production of documents (Article 117(1)(c) EPC). This interpretation has been repeatedly confirmed in the case law of the boards of appeal (see paragraph 10.2 on page 307 of the book "Case Law of the Boards of Appeal of the EPO", © 1996 EPO). As far as the meaning of "equity" is concerned, the EPC does not give any definition. However, apportionment of costs is justified if the conduct of a party is not in keeping with the care required in the exercise of its legal rights.

In the present case, the circumstance that led to the appellant's request for apportionment of costs is the late submission of documents. In particular, as far as the filing of documents D4, D5 and a further one by the respondent after the expiry of the nine-months' period for opposition laid down in Article 99(1) EPC is concerned, the Board holds that this was in response to submissions made by the appellant and observations made by the opposition division in the course of the proceedings (envisaged maintenance of the patent in amended form - see the communication of 3 April 1992, point 9a). Moreover, the circumstances are not such that it reasonably can be held that the respondent acted in bad faith. Therefore, in agreement with the case law reported on page 309 of the above-cited book, first paragraph of "(b) Late submission justified", the Board takes the view that no abuse of procedure has taken place with the belated submission of D4, D5 and a further one. This view also takes account of the administrative character of the opposition procedure. Thus, the appellant's request for apportionment of costs is not justified.

With regard to the decision T 117/86 (OJ 1989,401) cited by the appellant with the letter of 30 May 1994 (see point 6.i), attention is drawn to the fact that this decision refers to a case in which the circumstances differ from those in the present one. Indeed, in T 117/86, the appellant had produced together with the statement of grounds of appeal two new documents and an affidavit, whereas in the case in suit the documents D4 and D5 were filed in opposition proceedings before any decision of the opposition division was taken.

Order

For these reasons it is decided that:

1. The appeal is dismissed.

2. The request for apportionment of costs is refused.

The Registrar: The Chairman:

M. Beer G. Davies