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D E C I S I O N
of 8 June 1994

Case Number: T 0051/94 - 3.5.2

Application Number: 89301152.8

Publication Number: 328339

IPC: H03K 3/037

Language of the proceedings: EN

Title of invention:
Frequency-dividing circuit

Applicant:
Oki Electric Industry Company, Limited

Headword:
-

Relevant legal norms:
EPC Art. 84
EPC R. 67

Keyword:
"Clarity of claims (yes)"
"Reimbursement of appeal fee (no)"

Decisions cited:
-

Catchword:
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Case Number: T 0051/94 - 3.5.2

D E C I S I O N
of the Technical Board of Appeal 3.5.2
of 8 June 1994

Appellant: Oki Electric Industry Company, Limited
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Decision under appeal: **Decision of the Examining Division 068 of the European Patent Office dated 21 October 1993 refusing European patent application No. 89 301 152.8 pursuant to Article 97(1) EPC.**

Composition of the Board:

Chairman: E. Persson
Members: W.J.L. Wheeler
M.R.J. Villemin

Summary of Facts and Submissions

I. The Appellant contests the decision of the Examining Division to refuse application No. 89 301 152.8. The reason given for the refusal was that Claim 1 was not clear.

II. Claim 1 reads as follows:

"A frequency dividing circuit comprising:

a latch circuit (20) formed from first and second cross coupled logic gates (21, 22, 121, 131);

a first delay means (31) having its input coupled to an input of the first logic gate (21, 121, 131);

a second delay means (32) having its input coupled to an input of the second logic gate (22);

first and second switches (11, 12) each having a control electrode for receiving a common input signal (CK) to be frequency divided and responsive to the common input signal (CK) to connect the outputs of the first and second delay means (31, 32) respectively with said inputs of respective ones of the first and second logic gates (21, 22, 121, 131); and

output means arranged to output a signal (OUT, $\overline{OUT}$), having half the frequency of the common input signal (CK);

wherein the first and second switches (11, 12) comprise pass transistors (11, 12) and the first and second delay means (31, 32) comprise cascaded inverter circuits (31a, ... 31e, 32a, ... 32e)."

III. The Examining Division took the view that Claim 1 did not specify any connection between the output means and the remaining circuitry and that therefore the output means was not connected to the rest of the circuit at all. In a communication under Rule 51(4) EPC, dated 24 March 1993, the Examining Division proposed, inter alia, that the paragraphed section of Claim 1 beginning with the words "output means" should be amended to read:

"output means connected to the outputs of said first and second delay means (31, 32), said output means being arranged to output a signal (OUT, $\overline{OUT}$), having half the frequency of the common input signal (CK);".

IV. In a letter dated 10 June 1993, the Appellant approved the text sent with the communication under Rule 51(4) EPC, subject to deletion of the above amendment and a corresponding amendment on page 6 of the description.

V. In a subsequent communication dated 19 July 1993, the Examining Division proposed that the paragraphed section of Claim 1 beginning with the words "output means" should be amended to read:

"output means arranged to output a signal (OUT, $\overline{OUT}$), having half the frequency of the common input signal (CK), said frequency-divided signal being derived at at least one of the outputs of said first and second delay means (31, 32);".

VI. The Appellant objected to this proposed amendment and the Examining Division issued its decision to refuse the application.

VII. The Appellant then filed the present appeal and requested that the Examining Division carry out an interlocutory revision and that the appeal fee be reimbursed. The Appellant argued essentially that Claim 1 defined a frequency dividing circuit comprising a latch circuit, a first delay means, a second delay means, first and second switches and output means, these items being specified in a list, so that it was quite clear that the output means formed part of the frequency dividing circuit. The proposed amendments were unduly restrictive, because it was readily apparent from the application as originally filed that the output of the frequency divider could be taken from a number of different places which were not within the scope of the Examining Division's proposed claim, e.g. nodes N21, N22, N31, N32. As a result, the Appellant would be deprived of a fair reward for the disclosure of the invention, because there would be no protection for obvious variants.

The Examining Division had committed a substantial procedural violation in issuing the communication under Rule 51(4), because the amendments proposed therein went far beyond minor linguistic corrections and corrections of an obvious nature, contrary to the Guidelines for Examination in the EPO, C-VI 15.1.

Reasons for the Decision

1. The appeal is admissible. It is implicit in the reqest for interlocutory revision that the Appellant seeks the grant of a patent on the basis of the text as approved in the letter dated 10 June 1993 (see paragraph IV above).

2. It is clear from the correspondence between the Examining Division and the Appellant that the Examining Division considered the present application met the requirements of the EPC except for the fact that, in the opinion of the Examining Division, Claim 1 was not clear in that it did not recite any connection between the output means and the remaining circuitry.

2.1 Although Claim 1 does not specify the exact location of the output means, it does recite that the output means is arranged to output a signal having half the frequency of the common input signal. In the opinion of the Board, the only reasonable interpretation of this passage is that it specifies the functional requirement that the output means is connected to the rest of the circuitry specified in the claim in such a way as to output a signal having half the frequency of the common input signal. As is explained on pages 10 and 11 of the present application with reference to Figures 4 and 5, signals having half the frequency of the input signal (CK) exist at nodes N21, N22, N31, N32, OUT and $\overline{OUT}$. It is clear that this applies analogously to all the other embodiments described. The originally filed independent claims do not specify a precise point in the circuit at which the frequency-divided output is derived. Thus, the present application, as originally filed and in its

present form, makes it clear to the skilled reader that it is not necessary to derive the frequency-divided output at the points marked OUT and $\overline{OUT}$ in the figures showing the preferred embodiments; the output may be taken from any one of several other points in the circuit, such as the nodes N21, N22, N31 and N32.

2.2 In these circumstances it is appropriate to specify the broad functional requirement of the output means being arranged to output a signal having half the frequency of the common input signal. In the opinion of the Board, it would be manifestly unjust to force the Appellant to limit the protection to frequency divider circuits in which the output means outputs a frequency-divided signal derived from at least one of the outputs of the delay means. Such a limitation would allow others to copy the invention by simply taking the output from one of the other nodes where the frequency-divided signal exists.

2.3 In the opinion of the Board the claims, in the form approved by the Appellant, define the matter for which protection is sought in a clear manner. They are also supported by the description. Thus, the requirements of Article 84 EPC are met. The Board thus comes to the conclusion that the decision under appeal must be set aside.

3. The Appellant has submitted that the Examining Division committed a substantial procedural violation in issuing a communication under Rule 51(4) in which amendments were proposed which would drastically reduce the scope of the claims, contrary to the Guidelines for Examination in the EPO, C-VI 15.1, which state that such proposed amendments should

never extend beyond minor linguistic corrections and corrections of obvious errors.

3.1 Although it is normally desirable for Examining Divisions to act in accordance with the Guidelines, the Board wishes to point out that the Guidelines are guidelines, not rules of law, so that failure to follow a procedure set out there is not in itself a substantial procedural violation. Furthermore, the Examining Division did give the Appellant an opportunity to present comments, which the Appellant did in the letters dated 10 June 1993 and 11 August 1993, so that there was no infringement of Article 113(1) EPC. The fact that the Board has come to the conclusion that the decision under appeal must be set aside does not in itself justify reimbursement of the appeal fee.

Order

For these reasons, it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the first instance with the order to grant a patent on the basis of the claims, description and drawings sent with the communication under Rule 51(4) EPC, dated 24 March 1993, subject to the deletion of the handwritten insertion: "connected to the outputs of said first and second delay means (31, 32), said output means being" from Claim 1 and the deletion of the corresponding handwritten insertion on page 6 of the description.

3. The request for reimbursement of the appeal fee is refused.

The Registrar: The Chairman:

M. Kiehl E. Persson