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D E C I S I O N
of 14 September 1994

Case Number: T 0964/93 - 3.4.1

Application Number: 88106396.0

Publication Number: 0288052

IPC: H01L 23/12

Language of the proceedings: EN

Title of invention:
Semiconductor device comprising a substrate, and production method thereof

Applicant:
SUMITOMO ELECTRIC INDUSTRIES LIMITED

Opponent:
-

Headword:
-

Relevant legal norms:
EPC Art. 123(2), 56

Keyword:
"Main, first, second, fourth, fifth, sixth auxiliary requests: subject-matter which extends beyond the content of the application as filed (yes)"
"Third, seventh, eighth auxiliary requests: Inventive step (no)"

Decisions cited:
T 0169/83 OJ EPO 1985, 193; T 0204/83 OJ EPO 1985, 310;
T 0056/87 OJ EPO 1990, 188

Catchword:
-

Case Number: T 0964/93 - 3.4.1

D E C I S I O N
of the Technical Board of Appeal 3.4.1
of 14 September 1994

Appellant: SUMITOMO ELECTRIC INDUSTRIES LIMITED
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Decision under appeal: **Decision of the Examining Division of the European Patent Office dated 29 June 1993 refusing European patent application No. 88 106 396.0 pursuant to Article 97(1) EPC.**

Composition of the Board:

Chairman: G. D. Paterson
Members: H. J. Reich
Y. J. F. van Henden

Summary of Facts and Submissions

I. European patent application No. 88 106 396.0 (publication No. 0 288 052) was refused by a decision of the Examining Division.

II. The reason given for the refusal was that the subject-matter of independent Claims 1 and 4 filed on 19 May 1993 did not satisfy the requirements of Articles 52(1) and 56 EPC having regard to documents;

D1: DE-A-2 704 373 and
D4: Patent Abstracts of Japan, Vol. 7, No. 258 (E-211) [1403], 17 November 1983, corresponding to JP-A-58 143 556.

The Examining Division took essentially the following view: In the closest prior art disclosed in document D1, the use of bonding wires is already avoided by embedding a compound semiconductor chip in a concave portion of a silicon substrate so that the level of the top surface of the chip coincides with the level of the upper surface of the substrate, patterning a covering insulating layer to expose the electrodes on the chip and the substrate and forming thereon a connecting circuit pattern. Since it creates no technical difficulties and the advantages are readily contemplated in advance, it would be obvious to modify the conventional vertical wall structure of the concave portion to inclined sidewalls such as disclosed in document D4 for providing a minute space between chip and substrate. The inclusion of an etching stopper layer into the silicon substrate in order to form a recess of prescribed depth would be normal practice taught in textbooks.

III. The Appellant lodged an appeal against this decision, filing new sets of claims as main and first auxiliary requests, and maintaining the rejected version of claims as second auxiliary request.

IV. In a communication preparing oral proceedings the Board drew the Appellant's attention additionally to documents:

D2: IEEE Journal of Solid State Circuits, Vol. SC-21, No. 5, October 1986, pages 845 to 851, and
D3: Microelectronic Engineering, Vol. 3, No. 1/4, December 1985, pages 221 to 234

which had been also cited by the Examining Division, and informed the Appellant of its provisional view that inter alia the following claimed features cannot be derived from the content of the application as filed (Article 123(2) EPC):

(b) a compound semiconductor chip having "electrodes that do not project above the top surface of the chip", respectively said electrodes of the semiconductor chip (55) "do not project above the top surface thereof"; and

(c) to bring the level of the top surface of the compound semiconductor chip (55) approximately into coincidence with the level "of the supper surface of the **first circuit pattern** (60)", respectively the level of the top surface of the compound semiconductor chip (55) approximately coinciding with "the level of the upper surface of the first connecting circuit pattern (60)".

V. In reply to this communication the Appellant filed on 17 August 1994 nine new versions of claim sets as main and first to eight auxiliary requests.

Independent Claims 1 and 4 of the **main request** read as follows:

"1. A method for producing a semiconductor device comprising:

- forming an etching stopper layer (52) at a predetermined depth in a substrate (51);

- forming a first connecting circuit pattern (60) on said substrate (51);

- etching a predetermined area of said silicon substrate (51) up to the etching stopper layer (52) to form a concave portion (54) having an inclined side wall (54a);

- securing a compound semiconductor chip (55), having electrodes that do not project above the top surface of the chip, in the concave portion (54), the predetermined depth at which the etching stopping layer (52) is formed being such as to bring the level of the top surface of the compound semiconductor chip (55) approximately into coincidence with the level of the upper surface of the first circuit pattern (60);

- applying an insulating film layer (56) which covers said first circuit pattern (60), said chip (55) and its electrodes and the space between the inclined side wall (54a) of the concave portion (54) and the side wall of the compound semiconductor chip (55);

- patterning the insulating film layer (56) to expose said underlying first connecting circuit pattern (60) and the underlying electrodes of said chip (55); and

- forming a second connecting circuit pattern (57) on the insulating film layer (56), said second connecting circuit pattern (57) being itself in electrical contact both with said first connecting circuit pattern (60) and with said chip electrodes.

4. A semiconductor device comprising:

- a silicon substrate (51) having a concave portion (54) defined on the substrate (51);

- a compound semiconductor chip (55) which is disposed in said concave portion (54) and includes electrodes;

- insulating flattening means (56) covering over a space between the compound semiconductor chip and a side wall (54a) of the concave portion (54) to provide a flat surface;

- an electrical conductor means (60); and

- an electrical connector means (57) formed on the flat surface and connecting an electrode of the compound semiconductor chip (55) and the electrical conductor (60);

characterised in that:

- said electrodes of the semiconductor chip (55) do not project above the top surface thereof;

- said electrical conductor means (60) comprises a first connecting circuit pattern (60) formed on the surface of the silicon substrate (51), the level of the top surface of the compound semiconductor chip (55) approximately coinciding with the level of the upper surface of the first connecting circuit pattern (60);

- said side wall of said concave portion (54) is an inclined side wall (54a);

- said insulating flattering means (56) covers said first connecting circuit pattern (60), said chip (55) and its electrodes and is patterned to expose said underlying first circuit connecting pattern (60) and the underlying electrodes of said chip (55); and

- said electrical connector means (57) comprises a second connecting circuit pattern which is itself in electrical contact both with said exposed portions of said first circuit connecting pattern (60) and with said chip electrodes."

The **first auxiliary request** (1st alternative main request) maintains the claim wording of the main request cancelling feature (b) mentioned in paragraph IV above: i.e. the wording

in Claim 1: electrodes "that do not project above the top surface of the chip"; and

in Claim 4: "said electrodes of the semiconductor chip (55) do not project above the top surface thereof".

The **second auxiliary request** (2nd alternative main request) maintains the claim wording of the main request amending feature (c) mentioned in paragraph IV above: i.e. the wording

in Claim 1: as to bring the level of the top surface of the compound semiconductor chip approximately into coincidence with the level of the upper surface "of the first circuit pattern (60)" into "of the substrate (51)"; and

in Claim 4: the level of the top surface of the compound semiconductor chip (55) approximately coinciding with the level of the upper surface "of the first connecting circuit pattern (60)" in to "of the substrate (51)".

The **third auxiliary request** (3rd alternative main request) maintains the claim wording of the main request with the modifications of the first **and** second auxiliary requests.

Claims 2, 3 and 5 to 7 of the main to third auxiliary requests are identically worded and dependent on claim 1 or Claim 4 respectively.

The **fourth to seventh auxiliary requests** (1st auxiliary request and 1st to 3rd alternative 1st auxiliary requests) correspond to the main to third auxiliary request respectively wherein Claim 4 of the fourth to seventh auxiliary requests comprises additionally the feature:

"an etching stopping layer (52) is provided at a predetermined depth of the silicon substrate (51), said etching stopping layer (52) forming the base of the concave portion (54)"

Claims 2, 3, 5 and 6 of the fourth to seventh auxiliary requests are identically worded and dependent on Claim 1 or Claim 4 respectively.

Independent Claims 1 and 4 of the **eighth auxiliary request** (2nd auxiliary request) read as follows:

"1. a semiconductor device comprising:

a silicon substrate (51) having a first connecting circuit pattern (60) formed on the surface of the silicon substrate (51) and a portion (54) defined on the substrate (51) said portion (54) having an inclined side wall (54a);

a compound semiconductor chip (55) which is disposed in the portion (54), the level of the top surface of the compound semiconductor chip (55) approximately coinciding with the level of the upper surface of the silicon substrate (51);

flattening means for covering over a space between the compound semiconductor chip and the surrounding walls to provide a flat surface; and

a second connecting circuit pattern (57) formed on the flat surface, said second connecting circuit (57) connecting electrodes on the compound semiconductor chip (55) with the first connecting circuit pattern (60) on the silicon substrate (51);

said portion (54) being a concave portion; there being provided a minute space between the compound semiconductor chip (55) and the respective opposing sloping wall (54a), and an etching stopper layer (52) being provided at a predetermined depth of the silicon substrate (51), said etching stopper layer (52) forming the base of the concave portion (54).

4. A method for producing a semiconductor device comprising:

a process of forming an etching stopper layer in a predetermined depth of said substrate;

a process of forming a first circuit pattern on the substrate;

a process of etching a predetermined area of silicon substrate up to the etching stopper layer to form a concave portion having an inclined side wall (54a);

a process of accommodating a compound semiconductor chip in the concave portion, the level of the top surface of the compound semiconductor chip (55) approximately coinciding with the level of the upper surface of the silicon substrate (51);

a process of forming an insulating film layer for covering the space between the peripheral wall of the concave portion and the side wall of the compound semiconductor chip;

a process of patterning said insulating film to expose electrodes on said compound semiconductor chip and said first connecting circuit pattern on said silicon substrate; and

a process of forming a second connecting circuit pattern on the insulating film for connecting between the electrodes on the compound semiconductor chip and said first connecting circuit pattern,"

Claims 2, 3, 5 and 6 of the eighth auxiliary request are dependent on Claim 1 or Claim 4.

VI. Oral proceedings were duly held on 14 September 1994, during which the Board invited the Appellant inter alia to comment on the question of inventive step in view of document D1 and document D3, in particular the abstract on page 221; Figure 2 and the corresponding description on pages 223 and 224; and Figure 6 and the corresponding description on page 226.

VII. In support of his requests the Appellant argued essentially as follows:

Allowability of amendments

(a) The feature that the chip has electrodes which do not project above the top surface of the chip, i.e. feature (b) mentioned in paragraph IV above, is derivable from the drawings, since there would be some graphic indication, if the electrodes were projecting, and from the text of description column 5, lines 20 to 23. This text: "polyimide is coated .... on the **surface** (and not on the surfaces) of the electrodes" indicates that the electrodes of the application have no exposed side walls.

(b) The feature that the level of the top surface of the chip approximately coincides with the upper surface of the **first circuit pattern**, i.e. feature (c) mentioned in paragraph IV above, is manifestly part of the invention which distinguishes it over the prior art, and can therefore - according to Decision T 169/83, OJ EPO 1985, 193 - be derived solely from Figures 2(c) to 2(e) of the application. Decision T 204/83, OJ EPO 1985, 310 would not apply to the present case, since the skilled person

would interpret a diagrammatic drawing in the light of his expert knowledge. Knowing from document D1 Figure 2(d), page 7 (printed number), paragraph 3 and page 9, paragraph 4 to page 10, paragraph 6 that planarisation of the levels of the electrodes to be connected is technically important, the drawings of the application disclose to the skilled person the planarised electrode levels of feature (c). Decision T 56/87, OJ EPO 1990, 188, in particular page 193, paragraph 5 underlines that the skilled person interprets dimensions in diagrammatic drawings on the basis of the corresponding dimensions of the particular device used in practice. Therefore, a skilled person derives feature (c) from the entirety of the original application documents, being able to realise that feature (c) is indispensable in practice for achieving the disclosed technical result. Since original Claim 2 discloses that the level of the top surface of the compound semiconductor chip coincides with the level of the upper surface of the silicon **substrate** only "approximately", there is no technical contradiction between figure and description.

Inventive step

(c) The essential technical difference of the present invention over the closest prior art disclosed in document D1, is the fact that the conventional alignment step of the connecting terminals on chip and substrate by an additional planarisation step as disclosed in Figure 2(d) of document D1 and the corresponding description, is replaced by providing an etching stopper layer at a predetermined depth in the substrate. Hence, the present invention solves the problem of avoiding bonding wires in a different way which makes use of a more simple planarisation step and results in more reliable

electrical interconnections. This essential principle underlying the present invention, to achieve coincidence of the levels of the surfaces to be electrically connected by an etching stopper layer, is not derivable from the prior art. In the device disclosed in document D2, the chip is placed into a throughhole of the substrate and planarisation is realised by the same flat surface on which chip and substrate are placed for gluing the chip into the throughhole. The device disclosed in document D4, is not relevant since the wirings on chip and substrate are interconnected by a separate wiring substrate.

(d) Though document D3 on pages 223, 224 and 226 discloses to employ an etching stopper layer in a silicon substrate for the fabrication of a concave portion with inclined side walls, it does not at all teach to make use of an etching stopper layer for aligning a chip secured in the concave portion. to the upper substrate surface. Therefore, a skilled person would not combine the teachings of documents D1 and D3 in order to suppress the conventional alignment etching step of the method disclosed in document D1.

(e) Moreover, in the embodiment of Figure 2 of document D1 the substrate has no connecting circuit pattern as the embodiment of Figure 6 of document D1, but only a connecting terminal.

VIII. At the conclusion of the oral proceedings, the decision was announced that the appeal is dismissed.

Reasons for the Decision

1. *Main, first, second, fourth, fifth, sixth auxiliary requests - Article 123(2) EPC.*

1.1 The subject-matter of independent Claims 1 and 4 of the main, first, second, fourth, fifth and sixth auxiliary requests comprises either feature (b) or feature (c) or features (b) and (c) mentioned in paragraph IV above. Hence, in order to answer the question whether these requests are allowable under Article 123(2) EPC, it is necessary to examine whether a skilled person is able to derive features (b) and/or (c) from the original documents of the present application.

While useful general principles are set out in the decisions relied upon by the Appellant, the answer to the above question depends upon the proper interpretation of the application documents as originally filed.

1.2 In the diagrammatic representation of the compound semiconductor chip (55) in Figures 2(c) to 2(e) of the present application there is no separate reference sign for the electrodes of the chip. The upper surfaces of the chip and its electrodes are symbolised by the same continuous linear dash, allowing thus no conclusion whether the electrodes project above the top surface of the chip or not. Hence, feature (b) cannot "clearly, unmistakably and fully" be derived from the drawings and therefore does not satisfy the established requirements for disclosure by a drawing on its own. The text of the original description is totally silent about any particular form of the electrodes on the chip. In the Board's view, the generally accepted meaning of the term "surface" is that of a sum of the total area which

borders a body against its neighbouring space. There is no hint in the original description that the term "surface" is limited to an area in one geometrical plane only.

1.3 In the diagrammatic representation of chip and substrate in Figures 2(c) to (e) of the application it is the level of the upper surface of the **first circuit pattern** (60) and not the level of the upper surface of the **substrate** (51) which approximately coincides with the dash which globally symbolizes the upper surface of the chip and its electrodes. These dimensions obtained from the diagrammatic representation, technically contradict the teaching of the description in column 5, lines 15 to 18, reading "... the level of the surface of the gallium arsenide chip 55 coincides with the level of the surface of the silicon **substrate** 51." Contrary to the Appellant's submission in paragraph VII-(b) above, the addition of the term "approximately" before "coincides" in original Claim 2 is meant to include practical alignment deficiencies into the protection, and does not invalidate the technical teaching of the description mentioned above. Document D1, Figure 2(d) teaches to align the levels of the metallic surfaces to be electrically interconnected. The presentation of the chip surface and its electrodes by one and the same dash disregards the concrete thickness of the chip electrodes which is normally of the same order of magnitude as that of first circuit pattern 60. If the non-negligible thickness of the electrodes was taken into account in the drawing, this would lower the level of the upper surface of chip (55) in Figures 2(c) to (e) and thus remove the contradiction. Therefore, in the Board's view, making use of his expert knowledge and interpreting Figures 2(c) to (e) on the basis of the dimensions in practice, the skilled person would recognise that the contradiction between the description

and drawings results from the diagrammatic and therefore relatively inaccurate nature of the drawings, so that he would follow the description rather than the drawings when interpreting the information content of the application as filed.

1.4 For the reasons set out in paragraphs 1.2 and 1.3 above, the Board is satisfied that a skilled person would not derive features (b) and (c) mentioned in paragraph IV from the application as filed. Therefore, Claims 1 and 4 of the main, first, second, fourth, fifth and sixth auxiliary requests contain subject-matter which extends beyond the content of the application as filed and thus contravene Article 123(2) EPC. The further claims of these requests fall because of their dependence on the respective independent claim.

2. *Article 56 EPC - Claim 1 third and seventh auxiliary requests*

2.1 From the closest prior art disclosed in document D1 there is known in the identical wording of Claims 1 of the third and seventh auxiliary requests:

"A method for producing a semiconductor device comprising : ... forming a first connecting circuit pattern (see D1, 3 in Figure 2(a). The description of document D1, page 6 (printed number), lines 26 and 27 discloses that "connecting terminal**s** 3 of circuit element A (Verbindungs **anschlüsse 3** des Schaltungselements A)" are formed on the substrate. In the Board's view, a plurality of terminals of a circuit element, which is also derivable from Figure 3 of document D1, represents - contrary to the submission of the Appellant in paragraph VII-(e) - a connecting circuit pattern as claimed.) on said (silicon) substrate (1 in Figure 2(a); page 6 (printed), line 25) ...

securing (Figure 2(b)) a compound semiconductor chip (5; page 6, last paragraph) having electrodes (4) in the concave portion (2) ...; applying (Figure 2(c)) an insulating film layer (6; page 7 printed number, line 2) which covers said first circuit pattern, said chip and its electrodes and the space between the ... side wall of the concave portion and the side wall of the semiconductor chip;" etching "the insulating film layer to expose (Figure 2(d)) said underlying first electrodes of said chip; and forming a second connecting circuit pattern (7 in Figures 2(e) and 3) on the insulating film layer, said second connecting circuit pattern being itself in electrical contact both with said first connecting circuit pattern and with said chip electrodes (page 7 (printed number), paragraph 4)."

2.2 Starting from the closest prior art disclosed in document D1, the objective problem underlying the present invention is to indicate a method for producing a semiconductor device not requiring wire bonding, which method makes use of technically simplified production steps and results in more reliable electrical interconnections,; see also paragraph VII-(c) above. In the Board's view, the formulation of such problem belongs to the routine activities of a skilled person in further developing a conventional device.

2.3 The above technical problem is solved by the following measures:

(a) "forming an etching stopper layer at a predetermined depth of a substrate; etching a predetermined area of said silicon substrate up to the etching stopper layer to form a concave portion having an inclined side wall" and

(b) "the predetermined depth at which the etching stopping layer is formed being such as to bring the level of the top surface of the compound semiconductor chip approximately into coincidence with the level of the upper surface of the substrate"

2.4 The remaining feature distinguishing the subject-matter of Claim 1 over the closest prior art according to document D1 is that in the conventional method the **complete** surface of the insulating film layer is etched to expose the first circuit pattern on the substrate and the chip electrodes (see D1, Figure 2(d)), whereas according to the wording of Claim 1 of the present application the insulating film layer is **patterned** for the same purpose. Interpreting the claimed term "patterning" in the light of the embodiment in Figure 2(d) of the application, the distinction over the closest prior art consists in that only parts of the insulating film layer are etched off in order to form contact holes in the insulating film. Etching of contact holes is a generally known alternative to the complete removal of a dielectric film layer; see for instance Figure 2 of document D2 as expert opinion. Due to the fact that the Appellant in paragraph VII-(c) underlines that in the present invention the etching step which exposes the first circuit pattern and the electrodes, has no planarisation effect on their respective thickness, the Board takes the view that the "patterning" does not contribute to solve the objective problem set out in paragraph 2.2 above. It is regarded to be a generally known alternative, the use of which lies within the discretion of the skilled person and does not involve an inventive step.

2.5 It was not contested that distinguishing feature (a) in paragraph 2.3 above is disclosed in document D3. The steps of "forming an etching stopper layer at a predetermined depth of a silicon substrate and etching a predetermined area of said silicon substrate up to the etching stopper layer are disclosed in document D3, page 223 last two lines and page 224, lines 1 and 2. Etch parameters which result in the formation of a concave portion having an inclined side wall are disclosed in document D3, page 226. The abstract of document D3 on page 221 hints a skilled person to make use of this conventional micro-mechanical structuring technique of silicon bodies "for manufacturing complex integrated circuits" and thus also in the method disclosed in document D1. Due to the fact that document D1 is silent about the particular measures for producing the conventional concave portion, a skilled person would look for known structuring techniques of silicon bodies and thus fill out the gap of information in document D1 by the explicit measures disclosed in document D3. The Board regards it necessary to mention that the particular embodiments of etchant and etch stopper layer disclosed in the present application, i.e. ethylenediamine and a boron doped layer, are identical to the corresponding means disclosed in document D3. It is generally known that the implantation energy of the ions can be determined precisely and that for this reason the implantation of boron ions allows to produce doping profiles with very accurate local concentration distribution. In the Board's view, a skilled person is able to recognise this technical advantage and will make use of the measures disclosed in document D3 (i.e. feature (a)) in the method disclosed in document D1.

2.6 In the Board's view a skilled person will maintain the advantage of coinciding levels of the conventional method. Hence, distinguishing feature (b) in paragraph 2.3 above, i.e. the selection of the appropriate depth of the etching stopper layer for achieving level coincidence, represents a logical adaptation step in the obvious use of the structuring technique of document D3. Measuring the thickness of the chip and providing the etching stopper layer in a depth of the silicon substrate which corresponds to the measured chip thickness, lies within the normal intellectual capacities which can be expected from a skilled person.

2.7 For the reasons indicated in detail in paragraphs 2.1 to 2.6 above, in the Board's judgment, Claims 1 of the third and seventh auxiliary requests lack an inventive step within the meaning of Article 56 EPC.

3. *Article 56 EPC - Claim 4 - third auxiliary request*

3.1 Document D1 in Figures 2(e) and 3 with the corresponding description discloses the following features of independent device Claim 4 of the third auxiliary request:

"A semiconductor device comprising: a silicon substrate (D1, 1 in Figure 2(e)) having a concave portion (2 in Figure 2(a)) defined on the substrate; a compound semiconductor chip (5) which is disposed in said concave portion and includes electrodes (4), the level of the top surface of the compound semiconductor chip approximately coinciding with the level of the upper surface of the substrate (derivable from Figure 2(b)); insulating flattening means (6) covering over a space between the compound semiconductor chip and a side wall of the concave portion to provide a flat surface; an

electrical conductor means (3); and an electrical connector means (7) formed on the flat surface and connecting an electrode of the compound semiconductor chip and the electrical conductor; characterised in that: said electrical conductor means (3) comprises a first connecting circuit pattern (in the Board's view, the plurality of terminals 3 of a circuit element A forms a connecting circuit pattern; see also paragraph 2.1 above); ... said insulating flattening means (6) covers said first connecting circuit pattern (3), said chip and its electrodes and is "etched" to expose said underlying first circuit connecting pattern and the underlying electrodes of said chip (figure 2(d)); and said electrical connector means comprises a second connecting circuit pattern (see the plurality of parallel linear aluminium connectors 7 in Figure 3) which is itself in electrical contact both with said exposed portions of said first circuit connecting pattern (3) and with said chip electrodes (4; page 7 (printed number) paragraph 4)".

Hence, the independent device claim of the third auxiliary request is distinguished over the closest prior art disclosed in document D1 in that:

(a') "said side wall of said concave portion is an **inclined** side wall";

and in that said insulating flattening means is not etched but "patterned" to expose the first circuit connecting pattern and the electrodes. The Board holds this substitution of known exposing measures to be obvious for the reasons set out in paragraph 2.4 above.

3.2 Distinguishing feature (a') i.e. a concave portion in a silicon substrate with an inclined side wall is disclosed in document D3, Figure 6 with the

corresponding description on page 226; see also paragraph 2.5 above. In the Board's view, a skilled person can be expected to foresee that - with regard to the vertical side walls of the concave portion in the substrate of document D1 - an inclined side wall such as disclosed in document D3, will exercise a centring effect on the chip during its insertion into the concave portion and thus contributes to solve the objective problem set out in paragraph 2.2 above in that it improves the relative positioning of substrate and chip and thus makes electrical interconnections more reliable. Therefore, in the Board's view, a skilled person has a recognisable technical reason to make use of the inclined side wall structure according to document D3 in the substrate disclosed in document D1 and arrives at the subject-matter of Claim 4 of the third auxiliary request in an obvious way.

3.3 For the above reasons, the Board considers independent Claim 4 of the third auxiliary request not to involve an inventive step within the meaning of Article 56 EPC.

4. *Claim 4 - seventh auxiliary request*

4.1 Independent device Claim 4 of the seventh auxiliary request adds to Claim 4 of the third auxiliary request the feature:

(a") "an etching stopper layer is provided at a predetermined depth of the silicon substrate, said etching stopping layer forming the base of the concave portion."

Hence, the subject-matter of Claim 4 of the seventh auxiliary request forms the direct product of method Claim 1 of the third and seventh auxiliary requests.

4.2 Distinguishing feature (a") is disclosed in document D3, page 223, last two lines to page 224, lines 1 and 2 and its additional use in the substrate of the closest prior art disclosed in document D1 (the subject-matter of feature (a") in paragraph 4.1 and feature (a') in paragraph 3.1 corresponding to that of feature (a) in paragraph 2.3) is obvious for the reasons set out in paragraph 2.5 above.

4.3 Therefore, the subject-matter of Claim 4 of the seventh auxiliary request does not satisfy Article 56 EPC.

5. As stated in paragraphs 2.7, 3.3 and 4.3 above, the independent Claims of the third and seventh auxiliary requests are considered to lack an inventive step and not to be allowable with regard to Articles 52(1) and 56 EPC. The further claims of these requests fall because of their dependence on the respective independent claim.

6. *Eighth auxiliary request*

6.1 The Appellant did not contest that the subject-matter of device Claim 1 of the eighth auxiliary request corresponds to that of Claim 4 of the seventh auxiliary request (concave portion with etching stopper base) and that the subject-matter of method Claim 4 of the eighth auxiliary request corresponds to that of Claim 1 of the third and seventh auxiliary requests.

6.2 Hence, Claim 1 of the eighth auxiliary request is considered to lack an inventive step for the reasons set out in detail in paragraphs 3.1, 3.2, 4.1, 4.2 and 2.5 above, and Claim 4 of the eighth auxiliary request is considered to lack an inventive step for the reasons set out in detail in paragraphs 2.1 to 2.6 above. Claims 2, 3, 5 and 6 of the eighth auxiliary request fall because of their dependence on Claim 1 or Claim 4.

Order

For these reasons it is decided that:

The appeal is dismissed.

The Registrar: The Chairman:

M. Beer G. D. Paterson