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D E C I S I O N
of 24 November 1994

Case Number: T 0448/93 - 3.5.1

Application Number: 85401065.9

Publication Number: 0163580

IPC: G 06F 11/20

Language of the proceedings: EN

Title of invention:
Semiconductor integrated circuit with redundant circuit replacement

Applicant:
FUJITSU LIMITED

Opponent:

Headword:

Relevant legal provisions:
EPC Art. 123(2), 52(1), 56

Keyword:
"Inventive step - main request (no)"
"Inventive step - subsidiary request (yes)"

Decisions cited:
T 0004/80, T 0170/87

Catchword:

Europäisches Patentamt | European Patent Office | Office européen des brevets

Beschwerdekammern | Boards of Appeal | Chambres de recours

Case Number: T 0448/93 - 3.5.1

D E C I S I O N
of the Technical Board of Appeal 3.5.1
of 24 November 1994

Appellant: FUJITSU LIMITED
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Decision under appeal: **Decision of the Examining Division of the European Patent Office dated 1 December 1992 refusing European patent application No. 85 401 065.9 pursuant to Article 97(1) EPC.**

Composition of the Board:

Chairman: P. K. J. van den Berg
Members: A. S. Clelland
C. Holtz

Summary of Facts and Submissions

I. European patent application No. 85 401 065.9, filed on 30 May 1985 claiming the priorities of Japanese applications dated 31 May 1984 and 26 July 1984 and published under No. 163 580, was refused by a decision of the Examining Division dated 1 December 1992.

The reason given for the refusal was that the subject-matter of the independent Claim 1 as filed on 20 March 1992 lacked an inventive step having regard to the disclosure of the following prior art documents:

D1: WO 82/02793
D2: EP-A-86 310

II. On 10 February 1993 the Applicant lodged an appeal against this decision and paid the prescribed appeal fee. On 9 April 1993 a statement setting out the grounds of appeal was filed, together with a revised Claim 1.

III. In response to a communication from the Board pursuant to Article 110(2) EPC and dated 14 December 1993 the Appellant on 24 June 1994 filed a revised Claim 1 and revised pages 8 and 9 of description, together with arguments in support of patentability. In a further submission dated 27 July 1994 a subsidiary request was proposed, combining the subject-matter of the then valid Claim 1 with that of Claim 5. In response to a further communication from the Board dated 19 September 1994 inviting the Appellant to oral proceedings, the Appellant on 24 October 1994 proposed amendments to claim 1 of the main request, proposed a new subsidiary request whilst withdrawing that previously proposed, and

advanced further arguments in support of patentability. At the oral proceedings held on 24 November 1994 the Appellant filed new revised main and subsidiary requests.

IV. The Appellants **main request** is grant of a patent on the basis of the following document:

Claims:
1 to 11 as filed on 24 November 1994,
Description:
pages 1 to 7 and 10 to 13 as originally filed;
pages 8 and 9 as filed on 24 June 1994, with the amendment to page 8 proposed in the letter 24 October 1994,
Drawings:
sheets 1 to 10 as filed.

The Appellants **subsidiary request** is the grant of a patent on the basis of the following documents:

Claims:
1 to 10 as filed on 24 November 1994,
Description and drawings:
as for main request.

V. Claim 1 of the main request reads as follows:

"1. A semiconductor integrated circuit having memory cells and a redundant circuit portion for replacing failed memory cells comprising:

memory means (21) for storing address information of a failed circuit portion for replacing the failed circuit portion by a redundant circuit portion;

coincidence detection circuit means (2) comprising comparison means (24) for detecting coincidence between

data read from said memory means and a received input address; and

delivery means (8, 31, 32, 61, 62) for delivering data obtained from the comparison by said comparison means through an external connection terminal (7),

characterized in that said delivery means are connected between the comparison means (24), of said coincidence detection circuit means (2) and the external terminal (7) for operating when a predetermined voltage outside the usual operating range is applied to said external terminal (7), and for indicating the result of the comparison by the current passing through the same external terminal when said predetermined voltage is present thereat, and in that said delivery means (8, 31, 32, 61, 62) does not comprise a capacitor element".

Claim 1 of the subsidiary request reads as follows:

"1. A semiconductor integrated circuit having memory cells and a redundant circuit portion for replacing failed memory cells comprising:

memory means (21) for storing address information of a failed circuit portion for replacing the failed circuit portion by a redundant circuit portion;

coincidence detection circuit means (2) comprising comparison means (24) for detecting coincidence between data read from said memory means and a received input address; and

delivery means (8, 31, 32, 61, 62) for delivering data obtained from the comparison by said comparison means through an external connection terminal (7),

characterized in that said delivery means are connected between the comparison means (24), said coincidence detection circuit means (2) and the external terminal (7) for operating when a predetermined voltage outside the usual operating range is applied to said external terminal (7), and for indicating the result of

the comparison by the current passing through the same external terminal when said predetermined voltage is present thereat, and in that said comparison means (24) also comprises status detection means (25) for delivering a signal for indicating the written state of one of a plurality of memory cells (21) in said memory means from a terminal connected commonly to said plural memory cells, by supplying a specific address signal corresponding to said one memory cell, and in that said delivery means does not comprise a capacitor".

The Appellant's arguments in support of the patentability of the subject-matter of Claim 1 of the main request can be summarized as follows:

D1 used two separate pins for controlling and signalling. In order to provide the D1 arrangement with a single dual function pin the skilled person would require information from a further document, D2, referred to by the Examining Division. However, the design philosophy of D2 requires a current to be passed through a capacitive element, the resulting time constant causing the circuit to be too slow for practical use in memory testing. The skilled person would not therefore make use of the D2 external pin arrangement in connection with the D1 circuit. Even though Claim 1 was not specifically limited to a fast circuit, the Board having in one of its communications objected to the introduction of the word "quick", it would nevertheless be clear to the skilled man that such a circuit was intended. The introduction to the description specifically stated that one of the objects of the invention was to provide quick detection of the state of the memory circuit. The skilled man could not simply remove the capacitor from the D2 circuit since it was essential to the operation of the circuit.

Nor would the skilled person derive from D1 alone the teaching necessary to arrive at the claimed arrangement.

The subject-matter of the subsidiary request, which added the provision of a status detection line, was nowhere suggested in any of the cited prior art.

Reasons for the Decision

1. The appeal complies with Article 106 to 108 and Rule 64 EPC and is, therefore, admissible.

2. *Added Subject-Matter*

2.1 Claim 1 of both the main and auxiliary requests includes, in addition to features clearly derivable from the application as originally filed, the feature "that said delivery means... does not comprise a capacitor element". The originally filed application makes no reference to a capacitor element and includes no suggestion that any advantage is derived from the absence of such an element.

2.2 The established jurisprudence of the Boards of Appeal, see e.g. T 4/80 OJ EPO 1982, 149, is that originally disclosed subject-matter may be excluded from a wider claim by a disclaimer if the subject-matter remaining in the claim cannot technically be defined directly (positively) more clearly and concisely. It is observed that a disclaimer is more usually used in the chemical field to limit the Applicant to a range of values narrower than that disclosed in the examples in the description. Reference is also directed to T 170/87, OJ EPO 1989, 441, in which it was stated that if a disclaimer is by way of insertion of a new feature, such

that the technical teaching contained in the original documents would be substantially modified, then "this can be no more permissible by way of a disclaimer than it would be in any other way".

2.3 Nevertheless, the question of whether or not the present disclaimer is allowable or gives rise to objection under Article 123(2) EPC can in the Board's view - at least as regards the main request - be left undecided in view of the findings set forth below as regards clarity and inventive step. Although the Board would have been entitled to refuse to admit the claims to the proceedings - the amendment including the disclaimer having been filed for the first time in the course of the oral proceedings - it has taken the view that in the interest of procedural expediency the revised claims of both requests should be admitted so that the substantive issues may be decided.

2.4 The Board considers that despite clear difficulties with the language of the claims it is possible to discern the subject-matter underlying them and to apply Article 69 EPC and its Protocol to their interpretation, so that the substantive issues may be decided in the present proceedings.

3. *Closest prior art*

3.1 It is common ground that the single most relevant prior art document is D1. D1 discloses all the features of the preamble of Claim 1 of both requests. D1 also discloses at page 9, lines 4 and 5 the provision of an "abnormal condition detector" 26 connected via a signal line 24 to an external pin 22 of the integrated circuit. Detector 26 serves to detect the presence of a "normally disallowed state" on pin 22 and in response to place the circuit in a test mode. From page 10, lines 3 to 6 and

from the arrangement of transistors 40 in Figure 2 it can be seen that the "normally disallowed state" is an abnormally high signal.

3.2 D1 thus discloses means connected to an external terminal for operating when a predetermined voltage outside the usual operating range is applied to the external terminal. These means do not include a capacitor element.

3.3 Claim 1 of both requests accordingly differs from the disclosure of D1 in specifying that the aforementioned means is delivery means (for delivering data) connected between the comparison means and the external terminal to which the predetermined voltage outside the usual operating range is applied. In accordance with D1 a separate terminal for data output and voltage input is provided. The subject-matter of Claim 1 of both requests is accordingly novel.

4. *Inventive step (main request)*

4.1 From the above it can be seen that the D1 arrangement has the disadvantage that two external connection terminals must be used in order to derive the comparison information. However, D1 also states at page 9, lines 12 to 17 that, although two separate terminals are illustrated, "a single external pin may be utilised ... such that signal line 24 would be interconnected to external pin 20". No embodiment incorporating this principle is shown but clearly the result of the comparison must in some way be indicated through the line receiving the predetermined voltage outside the usual operating range.

4.2 The subject-matter of Claim 1 accordingly adds to the known disclosure of D1 only that the result of the comparison is indicated by the current passing through the external terminal when the predetermined voltage is present. However, once a predetermined voltage is supplied to the terminal it is difficult to see how else this skilled person could measure data at this terminal. The Board accordingly concludes that the skilled person, given the disclosure of D1 and desiring to follow the suggested path of using only a single external terminal, would without the exercise of invention derive the result of the comparisons carried out by measuring the current passing through the external terminal when the predetermined voltage is applied. The subject-matter of Claim 1 of the main request accordingly lacks an inventive step.

5. *Inventive step (auxiliary request)*

5.1 Claim 1 of the auxiliary request differs from that of the main request in including the subject-matter of the original Claim 5. The claim is accordingly directed to those embodiments, such as the Figure 5 embodiment, which provide a status detection line. This line indicates when a coincidence is detected on any one of the address lines. In other words, whereas in the Figure 4 embodiment the line 31 gives an output when a complete address of a failed memory cell is detected - i.e. when all coincidence detection circuits indicate coincidence and the line 31 goes high - the Figure 5 embodiment gives an output on the status detection line 41 when one bit of the cell address is detected and any one of the coincidence detection circuits goes high. This appears to have the advantage that instead of cycling through all the memory addresses in order to detect a failed cell, requiring 2^{n+1} cycles, each address line can be addressed in turn, thereby determining from the

individual address lines the failed cell and requiring only n+1 cycles. It is observed that this system would only appear to work if a single memory cell is defective, an issue not addressed in the application.

5.2 It is noted that the introduction to the description goes out from a state of the art according to which 2^{n+1} cycles are required to test a circuit, the object of the invention being stated to be the provision of "quick and correct detection" of the written state of the memory circuit. The Figure 4 embodiment would not appear to achieve this object, differing from the acknowledged prior art at Figure 1 only in the provision of the external terminal which - as noted at paragraph 4 above - is known per se from D1.

5.3 None of the prior art known to the Board discloses the use of memory testing by way of the individual address lines rather than the individual cells. Although in its decision the Examining Division does not explicitly discuss the subject-matter now included in Claim 1 of the auxiliary request it is noted that in its first communication the Examining Division drew attention to D1 at page 11, lines 19 to 22. However, although this refers to cycling through columns one at a time, it is clear in the context that this relates merely to the normal row and column select of a semiconductor memory rather than to individual address lines, the remainder of the cited paragraph in conjunction with Figure 3 making it clear that it is the memory cells rather than the address lines which are addressed individually. Attention is also directed to page 10, lines 27 to 35, according to which the decoder 70 is programmed with the address of a defective memory cell and "will respond to one particular combination of address inputs ... applied to the semiconductor memory to thereby generate a column of row select signal". The advantage in speed to be

gained by addressing the memory lines rather than the individual cells is not derivable from D1 or from any other document of which the Board is aware.

5.4 It will be appreciated that the above analysis is primarily based on a comparison of the Figure 5 embodiment of the application with D1 rather than on a strict reading of the wording of the claim. The Board has adopted this comparison in the interest of procedural efficiency as the representative had made clear in the oral proceedings that Claim 1 of the subsidiary request was intended to embrace the Figure 5 embodiment, although in the Board's view the claim is insufficiently clear to enable grant at the present stage of the procedure.

5.5 It will be observed that in the above conclusion on inventive step no account has been taken of D2. The Appellant's arguments on this document are therefore irrelevant. It is however observed that the assertion that the presence of a capacitor would slow down this circuit appreciably is not accepted by the Board. In the first place, the capacitor - designated Q_8 - is clearly an integrated circuit element formed by a transistor, as are all the other elements of the circuit. The capacitance is accordingly small. For the sake of completeness it is moreover observed that from D2 the skilled person learns - if he indeed needed to do so - that a single terminal supplied with a predetermined voltage could also be used as the data terminal; no invention can be seen in applying this knowledge to D1 at what ever speed that skilled person found necessary.

6. It is therefore necessary for the application to be remitted to the Examining Division for further prosecution on the basis of Claim 1 of the subsidiary

request. It will be necessary for the Examining Division to consider, inter alia:

(a) whether the term "comparison means" can be used to cover both the means 24 serving to detect whether a fuse has been blown for any given memory bit and the overall assembly of coincidence detection circuits;

(b) whether the reference to the status detection means being for delivering a signal "for indicating the written state of one of a plurality of memory cells in said memory means" is consistent with line 2 of the claim and with the description, the expression "memory cell" being generally used to refer to the main memory and replacement memory cells rather than the address memory incorporating the fused links which is apparently meant;

(c) whether the claim makes sufficiently clear that detection of a coincidence by any one of the circuits 2 causes a signal to be delivered to the terminal;

(d) whether the disclaimer "and in that said delivery means does not comprise a capacitor" is necessary and is supported by the subject-matter of the application as originally filed;

(e) whether the subordinate claims, in particular Claims 3 and 4, are consistent with the appreciation of the invention now put forward in the independent claim of the subsidiary request;

(f) whether Claims 6 to 9 are either consistent with, or add anything to, the preceding claims; and

(g) whether any embodiments are no longer covered by the independent claim and should therefore be deleted from the application.

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.

2. The main request is refused.

3. The case is remitted to the first instance with the order that further prosecution is to be based on the claims of the subsidiary request (paragraph IV above) having regard to the matters noted at paragraph 6 above.

The Registrar: The Chairman:

M. Kiehl P. K. J. van den Berg