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# D E C I S I O N
## of 6 December 1995

**Case Number:** T 0378/93 - 3.4.1

**Application Number:** 87102455.0

**Publication Number:** 0235705

**IPC:** H01L 21/28

**Language of the proceedings:** EN

**Title of invention:**
Self-aligned ultra high-frequency field-effect transistor, and method for manufacturing the same.

**Applicant:**
Kabushiki Kaisha Toshiba

**Opponent:**
-

**Headword:**
Field-effect transistor/Toshiba

**Relevant legal provisions:**
EPC Art. 56
EPC R. 34(1)(c); 88

**Keyword:**
"Inventive step (yes)"
"Correction of obvious errors"
"Deletion of prohibited matter"

**Decisions cited:**
T 0766/91

**Catchword:**
-

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**Case Number:** T 0378/93 - 3.4.1

# D E C I S I O N
## of the Technical Board of Appeal 3.4.1
## of 6 December 1995

**Appellant:** Kabushiki Kaisha Toshiba
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**Decision under appeal:** **Decision of the Examining Division of the European Patent Office dated 10 December 1992 refusing European patent application No. 87 102 455.0 pursuant to Article 97(1) EPC.**

**Composition of the Board:**

**Chairman:** G. D. Paterson
**Members:** Y. van Henden
U. Himmler

## Summary of Facts and Submissions

I. European patent application No. 87 102 455.0 (publication No. 0 235 705) was refused by decision of the Examining Division.

II. The reason given for the refusal was that, having regard to the state of the art which can be derived from the documents

D1: EP-A-0 034 729,

D2: IBM Technical Disclosure Bulletin, volume 24, No. 7A (December 1981), pages 3432 to 3433, New York (USA); H. S. Bhatia et al., "High performance MESFET structure",

D3: US-A-4 455 738,

D4: Applied Physics Letters, volume 40, No. 9 (1 May 1982), pages 805 to 807, New York (USA); R. L. Chapman et al., "Transcient annealing of selenium-implanted gallium arsenide using a graphite strip heater" and

D5: R. E. Williams :"Gallium Arsenide Processing Techniques", 1984, Dedham, MA (USA), pages 232 to 235, 270 to 273, 292 and 293,

independent Claims 1 and 3 of both a main and an auxiliary request filed on 21 October 1992 during oral proceedings before the Examining Division lacked an inventive step within the meaning of Article 56 EPC.

III. The Applicant lodged an appeal against the decision of the Examining Division.

With its Statement of Grounds of Appeal, the Appellant filed new pages of description numbered 4, 4a, 5, 5a, 5b, 6 and a set of five claims in replacement of the claims previously on file, requesting that a European patent be granted on this basis or, subsidiarily, that oral proceedings be scheduled.

IV. Claims 1 and 2 of the set filed with the Statement of Grounds of Appeal are independent claims reading:

1. A semiconductor device having source/drain electrodes and a gate electrode formed on a semiconductor substrate, comprising:

a one-conduction type lightly doped semiconductor layer (21) formed on said semiconductor substrate (20);

a gate electrode (23) formed on a predetermined region on said lightly doped semiconductor layer (21);

heavily doped source/drain regions (22a, 22b) formed in said lightly doped semiconductor layer (21) with prescribed intervals from both sides of said gate electrode (23), and

source/drain extraction electrodes (24a, 24b) of the same material as the gate electrode, formed on said heavily doped source/drain regions (22a, 22b) and with said prescribed intervals from both sides of said gate electrode;

characterized in that

the semiconductor substrate (20) is a GaAs semi-insulating substrate;

said heavily doped source/drain regions (22a, 22b) are doped with impurities of Se at an impurity concentration of 3 to 5 x $10^{19}cm^{-3}$, and

said gate electrode and said extraction electrodes (24a, 24b) are formed in a single layer structure of Al, Au or Ti/Al or by a multi-layer structure consisting of these metals, without alloying between said extraction electrodes (24a, 24b) and said heavily doped source/drain regions (22a, 22b).

2. A method for manufacturing a semiconductor device having source/drain electrodes and a gate electrode formed on a GaAs semiconductor substrate comprising the steps of:

forming a one-conduction type lightly doped semiconductor layer (21) on said semiconductor substrate (20);

forming a dummy gate (31) from a first material on a predetermined region on said lightly doped semiconductor layer (21);

forming a side wall film constituting member (32) from a second material on the exposed surface of said lightly doped semiconductor layer (21), the side wall film constituting member (32) covering said dummy gate (31);

performing an anisotropic etching for said side wall film constituting member (32) to form a side wall film (33) on each side of said dummy gate (31) and to expose the surface of said lightly doped semiconductor layer (21);

hot-ion implanting of Se impurity into said lightly doped semiconductor layer (21), by using as a mask said side wall films (33) and said dummy gate (31), and followed by lamp annealing so as to form heavily doped source/drain regions (22a, 22b) with an impurity concentration of 3 to 5 x $10^{19}cm^{-3}$;

selectively removing said dummy gate (31) so as to expose said lightly doped semiconductor layer (21) therebelow;

depositing an electrode constituting member (34) on said exposed lightly doped semiconductor layer (21) and said heavily doped source/drain regions (22a, 22b) using the remaining side wall films (33) as a mask, to form ohmic contact between said electrode constituting member (34) and said heavily doped source/drain regions (22a, 22b) without an alloying step, said electrode constituting member (34) being made in a single layer structure of Al, Au or Ti/Al or in a multi-layer structure consisting of these metals; and

removing said side wall films (33) and said electrode constituting member (34) deposited thereon so as to form a gate electrode (23) and source/drain extraction electrodes (24a, 24b) on said lightly doped semiconductor layer (21) and said heavily doped source/drain regions (22a, 22b), respectively.

The remaining Claims 3 to 5 are appended to Claim 2.

V. The Appellant's argumentation in support of its request may be summarized as follows:

The closest prior art is considered to be known from document (D3). According to the latter, the source and drain implants are made after removal of the dummy gate, whereby it may be assumed that the impurity concentration underneath the gate electrode will be high, as is consistent with the normal construction of a MESFET. This, however, is contrary to Claim 1, which states that the highly doped source/drain regions are formed before the dummy gate is removed. Besides, document (D3) relates to a silicon substrate only, whereas the contacts are made of platinum with formation of a silicide, i.e. a procedure equivalent to alloying.

As regards document (D2), it is impossible to remove the $SiO_2$ layer (13) without etching the $SiO_2$ side walls (15) and, owing to the ion bombardment, the etching rate of the latter may be higher than that of layer (13). In that case, the heavily doped regions (16) and metallic layers (17) cannot be self aligned. Furthermore, no indication concerning the metal to be used is found in document (D2) and, since no metal appears at the top of the side walls (15) after formation of the contacts, it may be assumed that a silicide has been formed.

Even a combination of the teachings in (D2) and (D3) does not solve the problem of forming the Schottky barrier at the gate region and ohmic contacts to the source and drain regions when using a GaAs substrate. Besides, it is not true that Table 11.1 of document (D5) indicates metals required for making electrodes, for such metals are actually listed in Table 11.2, which table does not include the metals mentioned in the claims.

It is furthermore noteworthy that both citations (D4) and (D5) express a prejudice against the use of lamp annealing techniques in presence of high levels of impurity. It is in particular stated in (D5) that many difficulties remain and that a maturation of such procedure in a foreseeable future is unlikely. The citation (D5) does not mention Se as impurity and leads away from solutions which do not use an alloying technique. On its side, document (D4) reinforce the opinion that no high concentration of Se in GaAs can be achieved without using an encapsulant, and cannot be obtained by lamp annealing. Nevertheless, the Applicant went away from these teachings and designed a device which functions correctly.

VI. The Board issued a communication pursuant to Article 11(2) RPBA taking the preliminary view that, having regard to the state of the art which can be derived from documents (D1) to (D5), either of the independent Claims 1 and 2 filed with the Statement of Grounds of Appeal lacks an inventive step. Nevertheless, the Board explained in its communication that a restriction of the claimed protection to the use of gold as constituent material of the contacts would be enough to render said Claims 1 and 2 allowable.

VII. The Appellant did not comment on the Board's communication and filed on 9 October 1995 alternative Claims 1 and 2 forming, with Claims 3 to 5 of the set received with the Statement of Grounds of Appeal, the basis of an auxiliary request. Pages 5a and 5b of description made consistent with said Claims 1 and 2 were jointly filed.

With respect to Claims 1 and 2 as filed with the Statement of Grounds of Appeal, the alternative Claims 1 and 2 differ in that:

- in the pre-characterising part of Claim 1, "extraction" is replaced by "extract ion";

- in the characterising part of Claim 1, the gate and extraction electrodes are said to be formed "in a single layer structure of Au", only;

- the preposition "for" has been replaced by "of" after "method" in the first line of Claim 2;

- in the last but one clause of Claim 2, the member (34) is said to be made "in a single layer structure of Au", only, and in that

- "deposited thereon" is replaced by "depositing therein" in the last clause of Claim 2.

VIII. The Appellant requests that the impugned decision be set aside and that a European patent be granted on the basis of the following documents:

**description:** pages 1 to 3 and 7 to 11 as originally filed; pages 4, 4a, 5, 5a, 5b and 6 filed with the Statement of Grounds of Appeal;

**claims:** 1 to 5 as filed with the Statement of Grounds of Appeal;

**drawings:** figures 1 to 4E of the application as originally filed.

Subsidiarily, the grant of a European patent is requested on the basis of the same documents, Claims 1 and 2 as well as pages 5a and 5b of description being replaced by corresponding claims and pages of description filed on 9 October 1995.

Appellant's request for oral proceedings is maintained if the Board does not consider at least the auxiliary request as acceptable.

## Reasons for the Decision

1. In Claim 1, the replacement of "extraction" by "extract ion" is an obvious clerical error, as evidenced by the correct spelling in the last clause. The same conclusion also applies to the replacement of "deposited thereon" by "depositing therein" in Claim 2, for the latter

formulation is grammatically incorrect and, from a technical standpoint, does not make any sense whatsoever. Correction of these mistakes under Rule 88 EPC is thus allowable.

2. The only question at issue was that of inventive step.

3. *State of the art*

3.1 Document (D2) discloses a method for manufacturing a semiconductor device having source/drain electrodes and a gate electrode - namely the so called "contact metallurgy" of Figure 6 - formed on a semiconductor substrate (11), for instance a GaAs substrate, comprising the steps of:

forming a "one-conduction type" semiconductor layer (10) on said substrate;

forming a dummy gate (13, 14) on a predetermined region of said layer (10);

forming a $SiO_2$ layer (15) by chemical vapour deposition, which layer thus covers the dummy gate (13, 14) and the exposed surface of the one-conduction layer (10) - see clause 5;

etching said $SiO_2$ layer to form a side wall film on each side of the dummy gate - what means that the $SiO_2$ layer (15) is a "side wall film constituting member" within the meaning of the present patent application - and to expose the surface of the one-conduction layer (10) - what implies that the etching is anisotropic;

ion implanting P or As impurity into the one-conduction layer (10) while using the side wall films (15) and the dummy gate (13, 14) as a mask so as to form source/drain regions (16) - see clause 6 and Figure 4;

selectively removing the dummy date (13, 14) so as to expose the one-conduction layer (10) therebelow, and

depositing an electrode constituting member (17) on the exposed one-conduction layer (10) and said source/drain regions (16) to form ohmic contact between said member (17) and source/drain regions, whereby the remaining side wall films (15) are used as a mask.

3.2 The subject-matter of Claim 2 according to the Appellant's main request is thus distinguished over the explicit disclosure in document (D2) in that:

(a) the one-conduction layer (21) is lightly doped;

(b) the dummy gate (31) is made of only one material;

(c) the layer (32) deposited in order to form the side wall films (33) is made of a second material, i.e. a material different from that of the dummy gate;

(d) hot-ion implanting is carried out;

(e) the ion implantation is followed by a lamp annealing;

(f) the implanted impurity is Se with a concentration of 3 to 5 x $10^{19}$ $cm^{-3}$;

(g) the "electrode constituting member (34)" is made in a single layer structure of Au, Al or Ti/Al, or in a multilayer structure consisting of these metals, and in that

(h) the side wall films (33) and the electrode constituting member (34) deposited thereon are removed.

The subject-matter of Claim 2 according to the auxiliary request is distinguished over said explicit disclosure in that it exhibits the above features (a) to (f) and (h), and in that the electrode constituting member (34) is made in a single layer structure of gold.

The Appellant did not contest these findings.

4. *Main request*

4.1 The present application relates to a ultra high frequency GaAs FET, i.e. to a semiconductor device having necessarily very small dimensions, hence in which the source/drain regions have to be accurately aligned with the gate electrode and with the source/drain extraction electrodes. It is indeed evident that the smaller the constitutive elements of a FET become, the most dramatically its operation is affected by a given deviation from the perfect alignment of said elements. As a matter of fact, this is the less disputable as document (D3) lays stress on the importance of such alignment in the case of miniaturised FETs - see column 1, lines 37 to 41.

Therefore, no inventive step can be perceived in setting the technical problem to be solved by the invention, namely finding the right procedure to be carried out in order to ensure a correct alignment of the constitutive

elements of miniaturised FET formed on a GaAs substrate, taking however into account that the use of this substrate material involves specific requirements and limitations.

4.2 Both document (D2) and the present application are concerned with the manufacture of miniaturised FETs - see: reference to VLSI in document (D2); lines 40 to 51 of column 3 in the published patent application.

The Appellant put forward in its Statement of Grounds of Appeal that, since the dummy gate (13, 14) formed on layer (10) while carrying out the method known from document (D2) comprises a layer (13) made of the same material as the side wall films (15), namely $SiO_2$, said side wall films too would undergo etching during the removal of the dummy gate. Therefore, no accurate alignment of the heavily doped source/drain regions (14) and metallic layers (17) would be achievable.

The Board nonetheless observes that the $SiO_2$ layer (13) is about 50 nm thick, whereas the $Si_3N_4$ top layer (14) is 100 to 200 nm thick - see clause 3 of the method. Therefore, the height of the side wall members (15) is about 3 to 5 times the thickness of the $SiO_2$ layer (13). When removing the dummy gate (13, 14), the first operation to be carried out consists in etching the comparatively thick $Si_3N_4$ layer (14), whereby it may be accepted that the $SiO_2$ side wall films (15) remain undamaged. The skilled person, in the present case a specialist of solid state physics having received university education and whose professional competence is not restricted to semiconductor devices formed on GaAs substrates, knows indeed that selective etching of $Si_3N_4$ without damage to neighbouring $SiO_2$ structures is possible - see document (D3), lines 27 to 30 of column 3, and notes that hydrochloric acid does not

attack silicon dioxide. He also knows that, during the heavy ion implant of impurity in the source/drain regions, the silicon dioxide will be damaged only at the top of the side walls (15) - see document (D3) again, lines 32 to 36 of column 3. Therefore, if the $Si_3N_4$ layer (14) is removed by means of HCl and if the $SiO_2$ layer (13) is removed by anisotropic etching while carrying out the method known from document (D2), said skilled person might expect the thickness of the side walls (15) at their foot not to be excessively changed, hence the achievement of a satisfactory alignment of the completed FET's components.

For these reasons, the Board takes the view that a skilled person attempting to manufacture miniaturised FETs on GaAs substrates would take into consideration the teachings of document (D2).

4.3 As already pointed out, the importance of a good alignment between the electrodes and source/drain regions of miniaturised FETs is known in the art, in particular from document (D3). Besides, semiconductor devices are usually mass produced and it must be borne in mind that memories comprise big amounts of FETs. Now, for obvious commercial reasons, manufacturers cannot take the risk of bringing on the market semiconductor devices that do not work satisfactorily, especially memories comprising one or even more FETs in which the tolerances in alignment would not be complied with. Therefore, before starting the production of integrated circuits comprising FETs suitable for operation at ultra high frequencies, numerous controls are performed at each stage of the fabrication.

Bearing this in mind, it may not be contended that a skilled person investigating the merits of the method disclosed in document (D2) would not detect deficiencies

in the alignment of the electrodes and source/drain regions of the FETs produced according to said method, or that he would not be able to understand that these deficiencies result from an unequal etching of the side walls in the direction parallel to the surface of the substrate - such defects are indeed revealed by microscopic observation. At this stage, he would also understand that the easiest way to obviate the drawback is to use a dummy gate and side walls made of different materials, said materials being liable to be removed separately by means of selective etchants. This solution is indeed disclosed in document (D3) - see Figure 1c and column 2, lines 37 to 50.

4.4 The Appellant did not contest the Board's view that the nature and concentration of the impurity implanted in the source/drain regions (feature f), the choice of the method for implanting said impurity in said regions (features d and e), the concentration of impurity in the gate region (feature a), the choice of the constituent material(s) and structure of the "electrode constituting member (34)" (feature g) and the removal of the side wall films (33) after completion of a FET (feature h) are not liable to affect the alignment of the source/drain regions (3a, 3b) with the gate electrode (4) and with the extraction electrodes (5a, 5b). It is indeed clear that, even if one or more of these features had some effect upon the extent of the source/drain regions and/or upon that of the gate electrode and extraction electrodes, this would not affect the alignment between these parts of a FET since said effect would be the same in all points of their periphery.

Therefore, whether the features (a, d, e, f, g, and h) merely achieve the results that should be normally expected from their provision or, in combination with one or more other features of the claimed subject-

matter, give rise to any unexpected, preferably advantageous synergetic effect has to be examined without reference to the problem of improving the alignment of the constituent parts of an integrated FET.

4.4.1 The gate region of a FET integrated in a semiconductor substrate separates the source and drain regions of the FET and, in one mode of operation of the FET, blocks the passage of charge carriers between said source and drain regions. However, it is a matter of obviousness that a minimal concentration of dopant is required to allow the passage of a current, whereas no blocking effect could be achieved if said concentration were excessive, hence, that the gate region of a FET has to be "lightly doped". As a matter of fact, neither during the proceedings before the Examining Division nor during the proceedings of appeal did the Appellant contend that there would exist integrated FETs in which the gate region of the substrate would be more than lightly doped.

Therefore, no exercise of inventive ingenuity was necessary to provide a light doping in the gate region of a FET formed on a GaAs substrate - feature (a).

4.4.2 Document (D5) teaches that, if the concentration of dopant in the surface layer of a GaAs substrate is at least $1 \times 10^{19}$, almost any metal placed in intimate contact with the surface will result in an ohmic contact without having to be alloyed - see page 234, first ten lines of section 11.3.1 "Ohmic Metallization". Bearing in mind that implantation depths are of the order of 1 µm or less, however, it is furthermore clear that the impurity's concentration mentioned in the cited passage of document (D5) cannot be in atoms per square centimetre but, instead, is in atoms per cubic centimetre.

Document (D5) admittedly acknowledges that such doping levels are not easily achieved, but hot ion implantation is not mentioned there. Besides, it is known in the art that implanting ions of a dopant into GaAs substrates while heating the latter to temperatures comprised in the range from about 200°C to about 400°C produces, after an appropriate annealing, good electrical characteristics. As a matter of fact, this teaching can be inferred from document (D4) and, moreover, in the case where the implant is selenium - see the summary and, in the sentence bridging the columns of page 806, the explicit reference to hot implantation. From document (D4), the reader also learns that Se concentrations as high as $3 \times 10^{19}$ $cm^{-3}$ or more can be achieved in the surface layer of a GaAs substrate - see page 806, lines 8 to 13 of the right hand column.

Therefore, even if the annealing operation is carried out according to the method disclosed in document (D4), an incentive to realise the source/drain regions of a FET comprising a GaAs substrate by hot implantation of Se ions with a concentration of at least $3 \times 10^{19}$ $cm^{-3}$ is anyway given to the skilled person - features (d) and (f).

4.4.3 Document (D4) reveals that furnace annealing as well as transient annealing by means of laser or electron beams have been envisaged to remove implantation damage in GaAs and to activate the implanted dopants - see the left hand column of page 805, lines 3 to 7 of the second paragraph. Shortcomings of these methods are mentioned and a presumably better method of annealing is accordingly proposed.

As already pointed out in the sections 4.2 and 4.3 of the present decision, however, the skilled person to be referred to here is a highly educated physicist and,

moreover, the economical interest of miniaturising integrated circuits is capital. Therefore, it is out of the question that such a person having read documents (D4) and (D5) would be deterred from investigating further annealing methods if he is not yet satisfied. As a consequence thereof, no inventive step can be perceived in the fact that the inventors selected lamp annealing - feature (e).

4.4.4 Document (D5) teaches that aluminium and titanium placed on GaAs exhibit good adhesion and thermal stability, and that multilayered metallisation are commonly used, in particular when the contacting metal is titanium. In the latter case, an overlay metal enhancing conductivity is indeed required - see section 12.3.1 on pages 271 and 272. Therefore, a skilled person seeking how to realise a FET on a GaAs substrate does not have to display inventive talent to envisage the provision of ohmic contacts in the form of a single layer of Al or Ti/Al, or in the form of a multilayered structure in which Al or Ti/Al is the contacting metal - feature (g) according to the main request.

4.4.5 Removing the side walls material is not envisaged in document (D2). Nevertheless, document (D2) teaches to make the side walls of silicon dioxide, i.e. the material of which dummy gates are usually made, as acknowledged in column 1 of the published patent application, lines 24 to 32. This material, however, is known to have a lower dielectric constant and to be a better insulator than silicon nitride, i.e. the material which is the most commonly used as alternative to silicon dioxide and, consequently, the most advisable one for making the side wall films (33) when carrying out the claimed method. The skilled person thus readily

understands that, if said films (33) are not removed after the gate and extraction electrodes have been made, excessive capacitive coupling and leakage currents between the latter might be expected.

Therefore, no inventive step either can be perceived in the removal of the side wall films (33) - feature (h).

4.5 Document (D5) is a technical handbook drafted by an author of acknowledged competence in the field of semiconductor devices formed on GaAs substrates. Consistent with the jurisprudence of the earlier decision T 0766/91 (not published), paragraph 8.2 of the Reasons for the decision, therefore, the information appearing in that document is common general knowledge of the skilled person working in said technical field. This also applies to the content of document (D4), which document is an article published in a scientific periodical essentially addressing to qualified professional and enjoying a worldwide reputation of seriousness.

Any skilled person attempting to solve a particular problem while designing a device, however, is supposed to bear in mind the elements of the common general knowledge in his field of professional activity. Therefore, if the design of a device involves any other technical problem which, together with at least one solution thereto, is part of said common general knowledge, the skilled person is ipso facto supposed to keep aware of the existence of said other technical problem and of the availability of said solution. In the present case, the provision of the features (d, e, f, g) of the claimed method represent, in view of the teachings disclosed in documents (D4) and (D5), such solutions to such problems forming part of the skilled person's common general knowledge. Having regard

thereto, the argument that the skilled person would have selected these documents rather than other ones among the available relevant literature might only be taken into consideration if, in combination with at least one other feature of the claimed method, one of said features (d, e, f, g) achieved an unexpected synergetic effect. However, no reason why such an effect would be produced can be perceived and, as a matter of fact, the Appellant neither contended that nor contested the relevance of the argumentation set forth in sections 4.1 to 4.4 of the present decision.

Therefore, in the Board's judgement, Claim 2 according to the main request lacks an inventive step within the meaning of Article 56 EPC. The same applies to the jointly filed Claim 1 for its subject-matter is the semiconductor device produced when carrying out the method of Claim 2.

4.6 Claims 3 to 5 of the main request fall because of their dependency on an unallowable Claim 2.

5. *Auxiliary request*

5.1 Document (D5) teaches that, contrary to aluminium and titanium - i.e. the other two metals mentioned in the patent application as envisaged for making the gate and extraction electrodes - gold exhibits poor adhesion to gallium arsenide and is highly susceptible of diffusing into that material - see page 271, lines 7 to 10 of the section headed "Choice of Metallization". Furthermore, said document is a technical handbook drafted by a person enjoying acknowledged authority in the field of semiconductor devices formed on GaAs substrates and, between the date of its publication and the priority date claimed in the present patent application, hardly more than two years can have elapsed. The Board,

therefore, has strong reasons to believe that, at said priority date, the skilled person involved in the design and production of semiconductor devices formed on GaAs substrates might have been deterred by a technical prejudice from using gold for making the gate and extraction electrodes of, inter alia, a FET integrated in such a substrate.

5.2 In the Board's judgement, therefore, Claim 2 according to the Appellant's auxiliary request involves an inventive step and is consequently allowable under Article 52(1) EPC. The same applies to Claim 1, since its subject-matter is the semiconductor device produced when carrying out the method of Claim 2.

6. The Board thus considers that the Appellant's request of oral proceedings is inapplicable.

7. The Board nonetheless observes that, on pages 8 and 10 as originally filed, references to electrodes formed in a single structure of Al or Ti/Al or in a multi-layer structure still appear - see lines 31 to 34 of page 8 and lines 13 to 18 of page 10. The responsibility for appropriate amendments as required by Rule 34(1)(c) EPC is left to the first instance.

**Order**

**For these reasons it is decided that:**

1. The decision under appeal is set aside.

2. The case is remitted to the first instance with the order to grant a European patent on the basis of the Appellant's auxiliary request with correction of the deficiencies mentioned in Sections 1 and 7 of the decision.

The Registrar: The Chairman:

M. Beer G. D. Paterson