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D E C I S I O N
of 9 February 1995

Case Number: T 0318/93 - 3.5.2

Application Number: 89201053.9

Publication Number: 0339737

IPC: H03K 19/096

Language of the proceedings: EN

Title of invention:
Integrated circuit having combinatorial logic functionality and provided with transmission gates having a low threshold voltage

Applicant:
Philips Electronics N.V.

Opponent:
-

Headword:
-

Relevant legal provisions:
EPC Art. 56

Keyword:
"Inventive step - no"

Decisions cited:
T 0128/87

Catchword:
-

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Case Number: T 0318/93 - 3.5.2

D E C I S I O N
of the Technical Board of Appeal 3.5.2
of 9 February 1995

Appellant: Philips Electronic N.V.
Groenewoudseweg 1
NL-5621 BA Eindhoven (NL)

Representative: Strijland, Wilfred
INTERNATIONAAL OCTROOIBUREAU B.V.
Prof. Holstlaan 6
NL-5656 AA Eindhoven (NL)

Decision under appeal: **Decision of the Examining Division of the European Patent Office dated 20 November 1992 refusing European patent application No. 89 201 053.9 pursuant to Article 97(1) EPC.**

Composition of the Board:

Chairman: A. G. Hagenbucher
Members: M. R. J. Villemin
C. Holtz

Summary of Facts and Submissions

I. The Appellant contests the decision of the Examining Division refusing European patent application No. 89 201 053.9 (publication No. 339 737) on the ground that the subject-matter of Claims 1 to 4 filed on 24 April 1992 did not involve an inventive step in view of prior art documents

D1: US-A-4 250 406,

D2: Patent Abstracts of Japan, Vol. 10, No. 95 (E-395)[2152], 12th April 1986 & JP-A-60-236322 and

general knowledge.

II. Introducing the subdivision (a) to (e) by the Board this Claim 1 reads as follows:

"1. An MOS integrated circuit comprising a plurality of transmission gates each having a single first transistor with a low threshold voltage and said gates being arranged for each feeding an associated further CMOS subcircuitry stage comprising exclusively second transistors having a threshold voltage that is substantially higher than said low threshold voltage, characterized in that

(a) multiple said gates in parallel feed a single input of said further subcircuitry stage,

(b) all of said first transistors are NMOS transistors,

(c) said circuit being arranged for operability at a supply voltage level of 2 Volts,

(d) in that said first threshold effectively lies between 0.1 Volts and 0.3 Volts and

(e) said higher threshold voltage is arranged for limiting off-state current in said further subcircuitry stage."

Claims 2 to 4 are dependent on Claim 1.

III. In a communication of the Board dated 18 May 1994 prior to oral proceedings the preliminary opinion was expressed that the subject-matter of this Claim 1 possibly lacked an inventive step in view of D1, the JEDEC standard No. 8 mentioned in the patent application and D3: US-A-4 595 845. Attention was also drawn to the reference IEEE Transactions on Electron Devices, Vol. ED-21, No. 6, June 1974, pages 324 to 331 referred to at column 3, line 24 to 26 of D1.

IV. At the oral proceedings, held on 9 February 1995, the Appellant requested the grant of a patent on the basis of Claims 1 to 4 (submitted 24 April 1992) as considered by the Examining Division (main request), or with amended Claim 1 according to a first or second auxiliary request.

Claim 1 of the first auxiliary request does not start in its preamble from D1 but from other prior art (EP-A-0 164 450, US-A-4 498 135), cited in the application. Claim 1 of the second auxiliary request starts from D1 as does Claim 1 of the main request.

The subject-matter of the independent claims according to both auxiliary requests is substantially distinguished from that of Claim 1 of the main request in that

(A) the integrated circuit of Claim 1 of the main request should comprise a combinatorial logic functionality with respective or specific multiples of transmission gates being connected in parallel to the input of a specific one of further subcircuitry stages,

(B) the voltage level "2 V" in feature (c) of Claim 1 of the main request is replaced by the range "2 to 3.6 V",

(C) the threshold level indicated in feature (e) of Claim 1 of the main request is defined as being "substantially 1 V".

V. The Appellant's arguments can be summarised as follows:

D1 relied on by the Examining Division as the most relevant prior art was concerned with the design of shift registers or sequential logic having a cascaded arrangement of alternating MOS transmission gates of P- and N-channel type and CMOS inverters. The object of this known circuit was, starting from a solution with two transistors per transmission gate, to minimise the number of transistors. The use of only one transistor per transmission gate was possible by adjusting the P-channel threshold voltages downwards in pre-selected transistors and by adjusting the N-channel threshold voltages upwards in other transistors. A further object was to attain reduced complexity due to the use of only one clock line instead of two lines. In contrast thereto the object of the present subject-matter was to provide an integrated circuit having combinatorial logic functionality and high integration density with low power dissipation. The circuit should operate with a high degree of reliability at a high switching frequency. To this end the present subject-matter envisaged operability of the MOS circuits at lower supply voltages. Contrary to D1 the transfer gates consisted only of N-MOS transistors. The presence of multiple clock signals was therefore accepted for the present subject-matter. A person skilled in the art confronted with the problem of reducing power dissipation for a circuit as known from D1 would not only reduce the power voltage but linearly downscale the

threshold voltages of transmission gates and subcircuitry stages. Instead, the technical features of the claimed subject-matter mainly diminished the threshold voltage value of the transmission gates.

Reasons for the Decision

1. Admissibility of appeal.

The Notice of Appeal/Statement of Grounds was filed one month before the end of the time limit for filing an appeal. A voucher for the appeal fee was mentioned in the Notice of Appeal but could not be found in the EPO. The EPO did not inform the Appellant about the missing voucher within the one month left before the end of the time limit. In view of this delay, the EPO shares some of the responsibility for the late payment of the fee. The Appellant was informed by the letter dated 5 August 1993 that the appeal fee is considered to have been paid in due time; cf. Rule 69(2) EPC and T 128/87 (OJ EPO 1989, 406), especially paragraph 9.

The present appeal is admissible.

2. The amendments comply with the requirements of Article 123(2) EPC. The subject-matter of the claims according to the main, first and second auxiliary requests can be derived from the claims as originally filed in conjunction with the Figure and original description, page 1, line 28, 29 and page 4, lines 15 to 18, 21 and 22. The term "combinatorial logic functionality" is defined on original page 1, lines 7 to 9.

3. *Main request*

3.1 As agreed by the Appellant in the Notice of Appeal/Statement of Grounds, an MOS integrated circuit comprising the features in the preamble of Claim 1 is known from D1. The circuit shown in Figure 4 of D1 also has features (a) and (e) recited in Claim 1 (cf. para. II. above). Gates 31 and 26 in parallel feed a single input (O) of the subcircuitry stage 42 (feature (a)). According to column 4, lines 17 to 24 in conjunction with column 3, lines 1 to 17 and 27 to 38 of D1, the bottom of the higher threshold voltage range (1.1 to 1.5 V) is kept higher than the top of the low threshold voltage range (0.4 to 0.8 V) in order to avoid high current leakages in the CMOS subcircuitry.

3.2 The subject-matter of Claim 1 differs from the circuit shown in Figure 4 of D1 by features (b), (c) and (d) (cf. para. II. above). It is novel, but not inventive for the following reasons:

3.3 The increasing demand for implementing more complex functions leads to higher integration and consequently to lower supply voltages in order to reduce energy dissipation per substrate area unit. JEDEC standard No. 8 of the Electronic Industry Association, which as a standard is considered as prior art, suggests a supply voltage range between 2 and 3.6 V. EP-A-339 737, column 1, lines 31 to 53 makes it clear that prior art integrated circuits with high treshold voltages of approximately 1 V would not function or have high static power dissipation and sensitivity to noise if they were operated at the supply voltages suggested by JEDEC standard Nr. 8. The threshold voltage ranges indicated in D1 (cf. para. 3.1 above) reveal that the known circuit is not specifically designed for supply voltages as low as those proposed by the JEDEC standard No. 8.

A person skilled in the art who is driven by the circumstances to highly integrate the circuit shown in Figure 4 of D1 would therefore try to modify this circuit so that it operates in the voltage range defined in JEDEC standard No. 8 without sacrificing the high degree of reliability at high switching speed. A high integration requires a low supply voltage so that the choice of a supply voltage as low as the lowest level of 2 V of the JEDEC standard (cf. feature (c) of Claim 1 as defined in para. II. above) would be envisaged by the skilled person without the need of inventive step.

3.4 It follows from the choice of the low supply voltage (2 V) that the threshold voltages of the transmission gates and of the CMOS subcircuitry stage of the circuit shown in Figure 4 of D1 have to be scaled down appropriately. It is clear from Figure 1 of D1 that the same transfer operation can be carried out by a N-MOS transistor triggered by means of a clock signal line $\overline{C}$ or a P-MOS transistor triggered by means of a complementary clock signal line C. The inherent P-channel threshold voltage is higher than the inherent N-channel voltage; cf. column 2, lines 26 to 29 of D1. It is known (cf. e.g. the reference cited in column 3, lines 24 to 26 of D1) that the threshold voltage of N-MOS transistors can be lowered more easily than that of P-MOS transistors. This reference (cf. Figures 12 and 15) shows that the treshold voltage of N-MOS transistors can approach about 0.1 V. It is furthermore clear from column 3, line 11 to 17 of D1 that the advantage of saving one clock signal line in the circuits according to Figures 2 and 4 entails the disadvantage of a higher-compromise-threshold voltage for the transmission gates because N-MOS and P-MOS transmission gates should have equal threshold voltages in order to avoid leakage currents in the following CMOS subcircuitry. In order to scale down the threshold voltage of the transmission

gates as a consequence of reducing the supply voltage a person skilled in the art will therefore accept the disadvantage of having two complementary clock signal lines and use only N-MOS transistors for the transmission gates in view of their low threshold voltage as already known from Figure 3 of D3. Hence, feature (b) of Claim 1 (cf. para. II. above) is just an obvious design consequence of reducing the supply voltage level.

3.5 It is known that a signal supplied through the input of a N-MOS transmission gate normally has at the output an amplitude loss in the order of magnitude of the effective threshold voltage of this transmission gate (cf. also D1, column 3, lines 2 to 8). If the supply voltage should be 2 V it is necessary to keep this amplitude loss as small as possible in order to obtain a sufficiently high signal for quickly switching the further CMOS subcircuitry stage. It is therefore normal design work to choose the threshold voltage of the transmission transistor in the range between the lowest N-MOS threshold voltage (about 0.1 V) and below the lowest threshold voltage (0.4 V) known from D1.

Hence, a voltage within the range defined in feature (d) of Claim 1 will readily be chosen by a skilled person if circumstances makes this desirable.

3.6 For the above reasons the Board finds that the subject-matter of Claim 1 according to the main request lacks an inventive step (Art. 52(1) and 56 EPC).

4. *Auxiliary requests*

4.1 The technical differences (A), (B), (C) (cf. para. IV. above) of the subject-matter of Claims 1 of both auxiliary requests over that of Claim 1 of the main

request do not add anything inventive for the following reasons:

4.2 Regarding (A): According to the patent application, page 1, lines 7 to 9, as originally filed the term "combinatorial logic functionality" means that the integrated circuit function is not limited to that of a memory function in isolation. This definition applies also to sequential logic circuits, for which the basic logic static storage element of Figure 4 of D1 is useful according to D1 (cf. column 4, lines 14 to 17). It is known that in sequential logic circuits specific multiples of transmission gates are connected in parallel to the input of a specific one of further subcircuitry stages in accordance with the desired functions. Referring to the narrower definition of "combinatoral logic functionality" in the applicant's letter dated 20 December 1991 attention is drawn to the fact that similar to the sole embodiment of the present application also according to Figure 4 of D1 co-existent input signals are not combined to an output signal necessarily co-existent therewith but are switched in a serial manner because the transfer transistors are controlled by complementary clock signals. Apart from this, D1 points in column 3, lines 64 to 68 also to the application for logic gates, e.g. NOR gates.

4.3 Regarding (B): The use of the full supply voltage range defined in JEDEC standard No. 8 instead of its lower voltage 2 V is not inventive, because the respective supply voltage depends only on the desired degree of energy reduction.

4.4 Regarding (C): Setting the threshold voltage of the CMOS subcircuitry to "substantially 1 V" means that it is set about 0.1 V lower than the corresponding lower limit (1.1 V) in D1. According to D1 (cf. column 4, lines 20

to 22) both transistors in inverters 41 and 42 of Figure 4 have a high threshold value in the range of 1.1 to 1.5 V which is higher than that of the transmission gates in order to avoid leakage currents. Since in CMOS processes the inherent P-channel threshold voltage is higher than the inherent N-channel threshold voltage and CMOS subcircuitry has P- and N-channels it is clear that due to the necessary compromise the threshold voltage cannot be reduced to an extent which is possible for NMOS transmission gates. Hence, setting the threshold voltage of a CMOS subcircuitry "substantially 1 V" is just normal design work of a skilled practitioner.

5. It follows from the above considerations that the subject-matter of Claims 1 according to the main and auxiliary requests lacks an inventive step in the sense of Article 56 EPC. These claims are therefore not acceptable under Article 52(1) EPC.

Order

For these reasons it is decided that:

The appeal is dismissied.

The Registrar: The Chairman:

M. Kiehl A. Hagenbucher

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