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D E C I S I O N
of 29 August 1996

Case Number: T 1037/92 - 3.4.1

Application Number: 86308245.9

Publication Number: 0228161

IPC: H01L 23/52

Language of the proceedings: EN

Title of invention:
Improved metal silicide fuse for integrated circuit structure and method of making same

Applicant:
ADVANCED MICRO DEVICES, INC.

Opponent:
-

Headword:
Fuse links/ADVANCED MICRO DEVICES

Relevant legal provisions:
EPC Art. 56, 78(1)(c)

Keyword:
"Inventive step (main and first auxiliary request: no)"
"Missing claims (second auxiliary request)"

Decisions cited:
T 0109/82, T 0176/84

Catchword:
-

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Case Number: T 1037/92 - 3.4.1

D E C I S I O N
of the Technical Board of Appeal 3.4.1
of 29 August 1996

Appellant: ADVANCED MICRO DEVICES, INC
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Decision under appeal: **Decision of the Examining Division of the European Patent Office dated 31 July 1992 refusing European patent application No. 86 308 245.9 pursuant to Article 97(1) EPC.**

Composition of the Board:

Chairman: H. J. Reich
Members: Y. J. F. Van Henden
M. Lewenton

Summary of Facts and Submissions

I. In response to a communication of the Examining Division, the proprietor of European patent application No. 86 308 245.9 (publication No. 0 228 161) filed with letter of 4 November 1991 an amended claim 1 reading

"A method of forming a metal silicide fuse for an integrated circuit structure having a controlled thickness which comprises:

(a) forming a layer of an insulating material (10) on an underlying structure (2);

(b) forming on said insulating layer (10) a layer of a predetermined amount of a metal (20) capable of reacting with silicon to form a silicide;

(c) forming over said metal a layer of silicon (30) in excess of the amount needed to react with all of said underlying metal (20);

(d) patterning said silicon (30) to form the desired fuse width and length prior to formation of the silicide;

(e) heating said structure to a temperature sufficient to cause said metal (20) and said silicon (30) to react to form the desired metal silicide (40); and

(f) removing unreacted portions of said silicon (30) and said metal (20) from said structure"

and further claims numbered 2 to 11, which were appended to that new independent claim.

II. The Examining Division refused the application on the ground that, having regard to the state of the art disclosed in documents

D3: D.C. Chen et al. "A new device interconnect scheme for sub-micron VLSI", IEDM 1984, pages 118 to 121, and

D4: US-A-4 135 295,

the subject-matter of the amended claim 1 lacked an inventive step.

III. The applicant lodged an appeal against the decision of the Examining Division.

IV. With its statement of grounds of appeal, the appellant filed an auxiliary set comprising nine claims.

Claim 1 of that auxiliary set differs from claim 1 as filed with letter of 4 November 1991 in that clause (b) reads "forming on said insulating layer (10) a layer of a metal (20) capable of reacting with silicon to form a silicide, said layer having a thickness of from about 25 to 1000 Angstroms (25 to 1000 x 10^{-10} m);", the spelling of "Angstrom" being here corrected, and in that "amorphous" has been inserted between "a layer of" and "silicon" in clause (c). The remaining claims of the auxiliary set are appended to the first claim.

V. The appellant requested that the decision of the Examining Division be set aside and that a European patent be granted to it on the basis of claims 1 to 11 as filed with letter of 4 November 1991, or on the basis of the auxiliary set filed with its statement of

grounds of appeal or a second auxiliary set, which set is mentioned in the latter document but was not filed. Subsidiarily, the appellant requested that oral proceedings be held if the Board were minded to uphold the impugned decision.

VI. The Board summoned the appellant to oral proceedings to be held on 29 August 1996. In an annex to the summons, the Board took the preliminary view that the state of the art disclosed in documents (D3) and (D4) does indeed form a bar to the allowability of claim 1 according to any of the appellant's main and first auxiliary request. The Board furthermore informed the appellant that no claims forming the basis of a second auxiliary request had been filed.

VII. The appellant neither filed written comments on the Board's communication, nor appeared at the oral proceedings. Being contacted by telephone, its representative informed the Board of the appellant's intention not to attend said oral proceedings.

As a matter of fact, by letter dated 5 August 1996, the appellant's representative had informed the Board that he would not attend the oral proceedings and looked forward to receive a written decision. This letter, which was transmitted to the Board after the date appointed for the oral proceedings, confirms the representative's declaration at telephone.

VIII. In support of its requests, the appellant argued in its written submissions substantially as follows:

The Examining Division was right when assessing novelty with respect to the disclosure in document (D4). However, its contention that, in a process of making fuses, it would be known from document (D3) to form the

metal layer and then to deposit silicon over the metal may not be accepted. Document (D3) refers indeed only to interconnects, i.e. (permanent) connections of circuits, and is in particular addressed to the use of metal silicide for making source/drain contacts. Since ohmic contacts are desired there, the presence of unreacted metal or silicon, either below or above the silicide, is immaterial, for the unreacted material enhances such a contact rather than interfering with it. In the case of a fuse, however, the latter's resistance would be affected by the presence of unreacted silicon, so that the fuse could not be reliably blown and, anyway, there would be some residual conductivity.

The applicant has discovered that, because the amount of unreacted silicon below the silicide of a fuse according to document (D4) cannot be easily controlled, an unknown further resistance acts in parallel with the fuse. Furthermore, some of the metal diffuses into the silicon in excess and lowers the value of this unknown resistance. Depending upon the amount of silicon under the fuse, a given current could thus be inadequate with one fuse and excessive with another. The same should also be expected when having followed the teachings of document (D3), for it is stated in the latter that there was no excess of silicon, so that it is reasonable to assume that an unremovable excess of metal will be left beneath the silicide.

The applicant furthermore contests that undoped silicon would have a negligible conductivity. Therefore, a bridge or path having a finite resistance could be left when blowing a fuse, whereby no total disconnection would be achieved. Since many circuits comprising blown fuses may be arranged in parallel, the resulting resistance could eventually be quite low, thus

affecting the operation of the circuits. Because of this, a person skilled in the art would not look to reference (D3) when building fuses. Besides, this also shows that the technical problem underlying the invention was not so obvious as the Examining Division thought.

IX. After deliberation by the Board, the Chairman gave the decision that the appeal is dismissed.

Reasons for the Decision

1. Document (D4) pertains to a method of forming platinum silicide fuse links for integrated circuit structures - see the title. Said method comprises the steps of

(a) forming a layer (57) of oxide on a silicon substrate (13) including a base (53) formed by diffusion into said substrate, i.e. "a layer of insulating material on an underlying structure", since silicon oxide is not conductive - see column 2, lines 40 to 45;

(c) forming on said insulating layer (57) a layer (59) of polycrystalline silicon in excess of the amount needed to react with all the platinum to be deposited thereon - see column 2, lines 45 to 48 and paragraph bridging columns 2 and 3;

(d) patterning said polycrystalline silicon (59) to form the desired fuse width and length, i.e. 2 µm and 8 µm, prior to the formation of the silicide - see column 2, lines 52 to 59;

(b) forming on the patterned polycrystalline silicon (59) a layer of platinum having a thickness of between 20 nm and 100 nm (200 to 1000 Angstroms) - see column 3, lines 26 to 28;

(e) heating the structure to a temperature of 560°C for approximately 20 mn, whereby a platinum silicide fuse (59') is formed - see column 3, lines 28 to 36 - and

(f) removing from the structure the unreacted portions of platinum - see column 3, lines 38 to 40.

2. The subject-matter of claim 1 according to the appellant's first auxiliary request is thus distinguished over the method disclosed in document (D4) in that:

- amorphous silicon is used instead of polycrystalline silicon;

- the order of deposition of silicon and the metal capable of reacting therewith to form a silicide is reversed, and in that

- also the silicon in excess is removed from the structure.

3. The shortcomings of fuses made in accordance with the teachings of document (D4) are of the kind which is revealed by use. This is actually the less questionable as the appellant itself contested that undoped silicon would have a negligible conductivity. Furthermore, programmable ROMs are normally produced in very big quantities and, before deciding to sell them to the public, fabricants submit them to numerous tests and controls in order to perfect their design and to

improve their reliability. In particular, the cause of the observed failures mentioned in the application is not liable to escape the attention of a skilled person examining fuses with, for instance, a scanning electron microscope after having submitted them to blowing tests.

The Board therefore takes the view that, contrary to the appellant's submission, identifying the drawbacks of the method disclosed in document (D4) does not require from a skilled person the exercise of inventive ingenuity - cf. decision T 109/82 (OJ EPO 1984, page 473), point 5.1 of the Reasons stating that a problem which could readily have been posed by any skilled person when and if the need had arisen must be regarded as obvious to the skilled person and, therefore, is unable to make a contribution towards the inventive merit of its solution.

4. Fuses are usually so designed as to withstand the current intensity needed for the normal operation of a device, and to be blown when the intensity of the current increases and nears values at which said device and/or connections thereto are liable to be damaged. In such programmable ROMs, where fuses and part of the other connections between components of the ROM are made at the same time, fuses are distinguished over said other connections in that their cross-section is smaller. Nevertheless, only part of the fuses of a programmed ROM have been blown and, when the programmed ROM is in use, the fuses having not been blown play the same part as all other connections of that integrated circuit.

Therefore, the Board does not accept the appellant's submission that fuses and other connections of a

programmable ROM would be intrinsically different kinds of conductors.

5. Pursuant to the jurisprudence of the earlier decision T 176/84 (OJ EPO 1986, page 50), paragraph 5.3.1 of the Reasons, a person skilled in the art of making fuse links for programmable ROMs and seeking how to preclude failures of such links is, in the absence of useful suggestions in the relevant technical field, expected to look for suitable parallels in neighbouring fields, i.e. fields in which problems similar to those in the field of fuse links arise and of which said person must be expected to be aware. Since fuse links are connections of reduced cross-section, the Board consequently takes the view that, starting form the teachings of document (D4) and seeking how to produce fuse links made of a metal silicide without leaving unreacted silicon in excess after completion of the manufacturing process, a skilled person would also have consulted the documentation available in the field of ultra miniaturised integrated circuits, whereby he would have taken document (D3) into consideration.

6. The latter document discloses a method of making interconnects for sub-micron VLSI by depositing sequentially, on the surface of a semiconductor substrate in which elements of an integrated circuit have already been formed, a thin layer of a refractory metal and a layer of amorphous silicon; photo-lithographically patterning the layer of amorphous silicon; annealing the wafer in order that the refractory metal reacts with the silicon; etching the metal in excess and performing oxide contact etching in a plasma having high selectivity to the silicide - see Figure 1 and section headed "Device concept and fabrication". The appellant's argument that no silicon in excess would be provided thus appears not to be

grounded and, furthermore, the result achieved by carrying out the method is not dependent on whether a source, a drain or nothing but the substrate underlies the interconnect.

As a matter of fact, the essential teaching given by document (D3) to the skilled person seeking how to produce better fuse links than can be made by carrying out the method disclosed in document (D4) is that the layers of refractory metal and silicon may be deposited in a reversed order, whereby the advantageous possibility of exclusively leaving metal silicide on the wafer is obviously provided.

7. In the Board's judgement, therefore, claim 1 according to the appellants's first auxiliary request lacks an inventive step.

8. Therefore, claim 1 of the first auxiliary request is not allowable - Article 52(1) EPC in conjunction with Article 56 EPC.

The remaining claims 2 to 9 of the first auxiliary request fall with claim 1 since they all are appended to the latter.

9. Claim 1 according to the appellant's main request does not exclude the use of amorphous silicon in the process of making fuse links and, as regards the layer (20) of metal capable of reacting with silicon, sets as implicit condition that the thickness of said layer is "predetermined". This latter feature, however, only makes sense if the remaining dimensions - width and length - of the fuse links to be produced are also predetermined, this ensuring that the same voltage shall be applied to blow said links. Nevertheless,

providing it does not require from the skilled person the exercise of inventive ingenuity.

In the Board's judgement, therefore, claim 1 according to the appellant's main request also lacks an inventive step.

10. Therefore, claim 1 according to the appellant's main request is not allowable either and with it fall the remaining claims 2 to 11 of that request for they all are appended to it.

11. No second auxiliary request has been filed during the delay imparted for that purpose. Therefore, the appellant's second auxiliary request does not comply with the requirements of Article 78(1)(c) EPC and no European patent may be granted on this basis.

Order

For these reasons it is decided that:

The appeal is dismissed.

The Registrar: The Chairman:

M. Beer H. Reich