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D E C I S I O N
of

25 April 1994

Case Number: T 0599/92 - 3.4.1

Application Number: 85400912.3

Publication Number: 0162774

IPC:

Language of the proceedings: EN

Title of invention:
Improvements in integrated circuit chip processing techniques and integrated circuit chip produced thereby

Applicant:
Digital Equipment Corporation

Opponent:
-

Headword:
-

Relevant legal norms:
EPC Art. 111(1)
EPC R. 86(3)

Keyword:
"Substantially modified claims filed with the Statement of Grounds of Appeal"
"Remittal to the Examining Division"

Decisions cited:
T 0063/86, T 0300/89

Catchword:
-

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Beschwerdekammern | Boards of Appeal | Chambres de recours

Case Number: T 0599/92

D E C I S I O N
of the Technical Board of Appeal 3.4.1
of
25 April 1994

Appellant: Digital Equipment Corporation
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Maynard, MA 01754 (US)

Representative: Mongrédien A.
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Decision under appeal: **Decision of the Examining Division 048 of the European Patent Office dated 26 February 1992 refusing European patent application No. 85 400 912.3 pursuant to Article 97(1) EPC.**

Composition of the Board:

Chairman: G.D. Paterson
Members: Y. van Henden
R. Shukla

Summary of Facts and Submissions

I. European patent application No. 85 400 912.3 (publication No. 0 162 774) was refused by the Examining Division on the sole ground that, taking into consideration the state of the art which can be derived from documents

D1: US-A-4 441 941 and
D2: EP-A-0 090 318,

the independent Claim 7 of a new set filed on 21 April 1990 did not involve an inventive step within the meaning of Article 56 EPC. The Examining Division nonetheless considered Claims 1 to 6 of said set to be allowable.

The claim refused by the Examining Division reads

"A method of forming an integrated circuit chip on a substrate (10) of a first conductivity type comprising the steps of:

A. providing active devices in active device regions (26) defined by openings in a field insulation layer, the gate electrodes (32) of the active devices having upper surfaces (33) and side surfaces (32), the upper surfaces of the gate electrodes (32) of the active devices being at the level of the upper surface (35) of the field insulation layer;

B. providing a sidewall insulation layer (44) on the sidesurface of the gate electrodes (32), the sidesurface insulation layer and the sidewalls of the field insulation layer defining windows (46); and

C. depositing conductive material (48, 50) in the windows (46), the upper surfaces of the conductive material in the windows (46) being at the level of the upper surface of the field insulation layer".

a minor spelling mistake being corrected here.

II. The Applicant lodged an appeal against the decision of the Examining Division.

With its Statement of Grounds of Appeal, the Appellant filed two sets of claims forming, respectively, the basis of a main and an auxiliary request. Claims 1 to 6 according to any of the Appellant's requests are identical to Claims 1 to 6 of the set received on 21 April 1990. Claim 7 according to the main request is still an independent claim and reads as follows:

"A method of forming an integrated circuit chip on a substrate (10) of a first conductivity type comprising the steps of providing active devices (32, 38, 40) in active device regions (26) defined by openings in a field insulation layer (12), the gate electrodes (32) of the active devices having upper surfaces (33) and side surfaces; providing a sidewall insulation layer (44) on the side surfaces of the gate electrodes (32), the sidewall insulation layer and the sidewalls of the field insulation layer (12) defining windows (46); and filling the windows (46) with a conductive material (48, 50); and further characterized by:

A. said sidewall insulation-layer-providing step comprising the steps of covering the upper surfaces of the active devices (32, 38, 40) and the field insulation layer (12) with an insulation layer (42), and reactive-ion etching the insulation layer (42) sufficiently to expose the upper surfaces of the active device (32, 38, 40) and the field insulation layer (12), the upper surfaces of the gate electrodes (32) of the active devices (32, 38, 40) being at the level of the upper surface (35) of the field insulation layer (12); and

B. said conductive-material-filling step comprising the step of depositing a layer of conductive material

(48, 50) in the windows (46) to the height of the field insulation layer (12) and the gate electrode (32), said conductive-material-depositing step including the steps of depositing a layer of conductive material (48, 50) over the upper surfaces of the active devices (32, 38, 40) and the field insulation layer (12); and etching the layer of conductive material (48, 50) so that the conductive material is only disposed in said windows (46), whereby the upper surfaces of the layer of conductive material (48, 50) in the windows (46) is at the level of the upper surfaces of the gate electrodes (32) and the field insulation layer (12)."

To this claim are appended seven claims numbered 8 to 14.

Claim 7 of the Appellant's auxiliary request is appended to Claim 1, and the remaining Claims 8 to 16 are appended to Claim 7.

Reasons for the Decision

1. With respect to the method of forming an integrated circuit chip covered by Claim 7 as filed on 21 April 1990, the subject-matter of Claim 7 according to the Appellant's main request is distinguished in that it comprises the steps of:

(a) covering the upper surfaces of the active devices (32, 38, 40) and the field insulation layer (12) with an insulation layer (42);

(b) reactive-ion etching the insulation layer (42) sufficiently to expose the upper surfaces of the active devices (32, 38, 40) and the field insulation layer (12);

(c) depositing a layer of conductive material in the windows (46) to the height of the field insulation layer (12) and the gate electrodes (32), over the upper surface of the active devices (32, 38, 40) and over the field insulation layer (12), and of

(d) etching the layer of conductive material so that the conductive material is only disposed in said windows (46), whereby the upper surfaces of the layer of conductive material (48, 50) in the windows (46) is at the level of the upper surfaces of the gate electrodes (32) and the field insulation layer (12).

Steps (a) and (b) are in substance equivalent to the steps (A) and (B) respectively, of Claim 15 of the set the Examining Division took into consideration while drafting its first communication, i.e. a set the Appellant had filed on 24 May 1988 pursuant to Rule 86(2) EPC. Likewise, steps (c) and (d) are respectively equivalent in substance to the steps (A) and (B) of Claim 18 of the latter set. The features recited in the above-mentioned Claims 15 and 18 are substantially equivalent to those recited in Claims 13 and 16, respectively, of the set filed on 21 April 1990 forming the basis of the decision under appeal.

2. In its first communication, issued on 28 December 1989, the Examining Division merely, and under the circumstances, justifiably, wrote that "Claims 10-18 add standard features that are either described in (D2) or are within the routine competence of a skilled person" - cf. paragraph 8 of the communication. With consideration to the amended set of claims filed on 21 April 1990, the decision under appeal asserts that the subject-matter of the Claims 8 to 16 does not involve an inventive step - see paragraph 5.2.

3. The Examining Division having not otherwise reasoned its judgment as regards the method steps (a), (b), (c) and (d) mentioned in paragraph 1 above, the amendments to independent Claim 7 which the Appellant has proposed in the appeal proceedings require a substantial further examination in relation to both the formal and substantive requirements of the EPC. As stated in Decision T 63/86 (OJ EPO 1988, 224), such further examination should be carried out by the Examining Division as the first instance after the Examining Division has itself exercised its discretion under Rule 86(3) EPC. The reasons for this are discussed fully in paragraph 2 of the Decision.

4. In the present case, since the Appellant no longer seeks grant of a patent including Claim 7 with text and subject-matter as rejected by the Examining Division, but has filed a main request containing a substantially amended text for Claim 7, it is clearly appropriate that the case should be remitted to the Examining Division in accordance with Decision T 63/86.

The Board also refers to Decision T 300/89 (OJ EPO 1990, 9), where it was stated in particular that "the burden lies upon an applicant (if he so wishes) to propose amendments (including by way of auxiliary requests) which overcome the objections raised by the Examining Division, in his observations in reply to the first communication in which such objections are raised". Clearly, the filing of a new set of requests for the first time in the Statement of Grounds of Appeal, as in the present case, inevitably leads to undesirable procedural delay.

Order

For these reasons, it is decided that:

1. The contested decision is set aside.

2. The case is remitted to the first instance for further examination of the application having regard to the requests set out in the Statement of Grounds of Appeal.

The Registrar:

M. Kiehl

The Chairman:

G.D. Paterson