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D E C I S I O N
of 7 December 1993

Case Number: T 0598/92 - 3.4.1

Application Number: 86905487.4

Publication Number: 0235248

IPC: H01L 29/90

Language of the proceedings: EN

Title of invention:
Detector and mixer diode operative at zero bias voltage and fabrication process therefor

Applicant:
Hewlett-Packard Company

Opponent:
-

Headword:
-

Relevant legal norms:
EPC Art. 56

Keyword:
"Inventive step (yes, after amendment)"

Decisions cited:
-

Catchword:
-

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Beschwerdekammern | Boards of Appeal | Chambres de recours

Case Number: T 0598/92 - 3.4.1

DECISION
of the Technical Board of Appeal 3.4.1
of 7 December 1993

Appellant: Hewlett-Packard Company
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California 94304 (US)

Representative: Colgan, Stephen James and
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Decision under appeal: **Decision of the Examining Division of the European Patent Office dated 19 February 1992 refusing European patent application No. 86 905 487.4 pursuant to Article 97(1) EPC.**

Composition of the Board:

Chairman: G.D. Paterson
Members: H.J. Reich
R.K. Shukla

Summary of Facts and Submissions

I. European patent application 86 905 487.4 (publication number WO 87/00693) was refused by a decision of the Examining Division.

II. The reason given for the refusal was that the subject-matter of independent Claims 1, 8, 9, 10 and 18 filed on 26 February 1991 and 17 May 1991 did not satisfy the requirements of Articles 52 and 56 EPC having regard to documents:

D1: US-A-3 398 334
D3: US-A-4 410 902, and

the general knowledge of a skilled person. On the basis of theoretical considerations the Examining Division took in particular the view that the diode claimed in Claim 1 differs from the nearest prior art disclosed in document D1 in that document D1 does not explicitly mention that the layer of opposite conductivity type semiconductor material has a thickness sufficient to shield metal impurities in the first ohmic contact from the critical thin layer and that the diode is operative at zero volts DC bias for both diode detector applications and anti-parallel mixer diode applications. Since it has been established that the claimed and the known diode structures are the same, it must therefore be assumed that the device of document D1 is also suitable for operation at zero volts DC bias for the applications mentioned. Moreover, since it can readily be foreseen that the impurities would cause deterioration of the performance of the device, it would be a normal design procedure implicit to the average practitioner to make the layer of opposite conductivity type semiconductor material thick enough so that

impurities from the ohmic contact do not reach the critical thin layer. The design requirements of document D1 are stated in a form which is independent of explicit values of doping densities, thickness of layers, etc., so that their calculation can readily be done by using textbook formulae relating to the depletion widths and the doping levels at the pn-junction. The thickness chosen for instance in the NIPIN structure of document D3 for the critical P-layer could be used for guidance to a suitable thickness.

III. The Appellant lodged an appeal against this decision. In the Statement of Grounds of appeal the main request was to maintain the claimed subject-matter unamended, and an auxiliary request was also filed. The Appellant argued *inter alia* that the diodes of document D1 have a non-depleted critical P-layer with a thickness and concentration which would provide such a high barrier height to be unacceptable for use at zero bias DC voltage. Document D3 being based on a different layer structure, (NIPIN instead of NPIN) would give no guidance regarding how to tailor the critical thin layer for producing the claimed functions within an NPIN structure.

IV. In a communication accompanying a summons to oral proceedings, the Board expressed its preliminary view that the subject-matter of Claim 1 as maintained unamended was obvious having regard to the prior art disclosed in documents D1,

D4: Electronics Letters, 3 March 1983, vol. 19, No. 5, pages 181-183, and

D6: R.K. Willardson et al.: "Semiconductors and Semimetals", vol. 15, Contacts, Junctions, Emitters, Academic Press, 1981, pages 30 and 31.

In reply, the Appellant withdrew his previous requests and filed new Claims 1 to 16 as a new request.

V. Oral proceedings were held on 7 December 1993, at the end of which the Appellant requested that the decision under appeal be set aside and that a patent be granted on the basis of a new main request consisting of Claims 1 to 6, including an amended Claim 1 in which, *inter alia*, the former general functional definitions of thickness and impurity concentration of the intrinsic or substantially intrinsic layer enabling operation at zero volts DC bias, were replaced by the specific values of these parameters which are disclosed as essential for realising such an operation. Thus, it was requested that a patent be granted on the basis of the following main request:

Claims:	1 to 6, filed during the oral proceedings;
Description:	pages 7 and 12 as originally filed, pages 1, 2, 8 and 9 as filed on 26 February 1991, pages 3, 4, 5, 6, 10 and 11 as filed during the oral proceedings;
Drawings:	sheets 1/4 to 4/4 as originally filed, but with amendment to Figure 4B.

VI. Claim 1 of the main request reads as follows:

"1. Circuitry including a diode structure (10) having:

a) a single intrinsic or substantially intrinsic semiconductor layer (16) having a thickness and impurity concentration such that it is substantially depleted of majority carriers;

b) a critical thin semiconductor layer (18) of either N or P type disposed on a surface of said intrinsic layer (16);

c) a layer (20) of opposite conductivity type (P or N) semiconductor material disposed on the other surface of said critical thin layer (18), to form a PN junction;

d) a further semiconductor layer (14) of said opposite conductivity type, or a conductive substrate (12), disposed on the other surface of said intrinsic layer (16);

e) a first ohmic contact (22) disposed on the other surface of said layer (20) of said opposite conductivity type semiconductor material;

f) a second ohmic contact (24) disposed either on said conductive substrate (12) or on said further semiconductor layer (14) of said opposite conductivity type,

characterised in that:

the diode structure (10) is operating at zero volts DC bias at microwave or millimetre wave frequencies;

said layer (20) of opposite conductivity type is thick enough so as not to be fully depleted of majority carriers during operation of the diode structure and so as to shield metal impurities between the first ohmic contact (22) and the critical thin layer (18);

said critical thin layer (18) is between 2.5 and 14 nm (25 and 140 Angstroms) in thickness, and is fully depleted of majority carriers;

said intrinsic layer (16) is between 50 and 150 nm (500 and 15,000 Angstroms) in thickness; and

the doping level in said intrinsic layer (16) is of the order of 10^{14} atoms/cc, the doping level in said critical thin layer (18) is of the order of $8x10^{18}$ atoms/cc, and the doping level in said opposite conductivity type layer (20) is of the order of $5x10^{18}$ atoms/cc."

Claims 2 to 6 of the main request are dependent on the above Claim 1.

VII. In support of this main request the Appellant argued essentially as follows:

(a) As indicated in the description of the present application, the prior art realises an operation at zero volts DC bias only in a metal-silicide-silicon Schottky barrier diode; see US-A-3 968 272 (D7), which has a completely different structure.

(b) The wording of document D4, page 182, left column, lines 2 and 3: "the buried layer remains fully depleted at **all** applied bias" will not be interpreted by a skilled person as a depletion at **zero** volts DC bias. The depletion widths of Figure 1 are theoretical values. Moreover, the wording of document D4, page 182, left column, last two lines to right column, line 1 and page 183, left column, lines 1 to 7 clearly shows that a zero bias voltage was used in document D4 only as an assumed boundary value for calculating **theoretical** barrier heights. Table 1 on page 182, therefore, gives no information with regard to barrier heights allowing a diode to be in practice operated at zero volts DC bias.

(c) The calculations of document D4 are based on an NPN structure and not on the claimed NPIN structure. Moreover, the use of an n-layer instead of an intrinsic one would lead to only a small depletion in the critical thin layer and to changes in capacitance, so that the degradation of the response at high frequencies would be pronounced. Thus, a combination of documents D4 and D1 would not be obvious.

(d) A combination of documents D1 and D3 does not lead to the invention in an obvious manner, since both documents relate to using a DC bias voltage across the diode structure.

(e) Showing theoretically how the invention may be derived from the cited prior art after considering the disclosure of the application, represents an unallowed *ex post facto* analysis. Moreover, the early publication of D1 and the subsequent attempts according to document D7, leading in practice to unsatisfactory results, show that the claimed solution for realising zero volts DC bias operation of a detector diode at high frequencies was not at all obvious. In particular, there is no evidence that there was an incentive to reduce the critical layer thickness in the diode of document D1 in order to enable detector operation at zero volts DC bias.

VIII. At the conclusion of the oral proceedings, the decision was announced that the decision of the Examining Division is set aside and that the case is remitted to the first instance with the order to grant a patent on the basis of the main request set out in paragraph V above.

IX. On 8 December 1993, the day following the oral proceedings, the Appellant filed a letter questioning whether Claim 1 as filed during the oral proceedings literally read on to Figures 3A and 3D of the description, and requesting correction of an error in Claim 1 in this connection, by replacing the words "on the other surface of said layer (20)" in Claim 1 with the words "on a surface of said layer (20)".

Reasons for the Decision

1. The subject-matter of Claim 1 of the main request comprises the characteristics of original Claims 1, 3, 4 and 6 and features disclosed in the original description, page 7, lines 13 to 18. The features of dependent Claims 2 to 6 are disclosed in the following original text: page 10, lines 15 to 18; page 10, line 18 to page 11, line 6; Claim 2 and page 6, line 1; page 9, lines 21-24; and Claim 5. The amendments of the description are in line with Rules 27(1)(b),(c) EPC. There is therefore no objection under Article 123(2) EPC to the current set of application documents.

2. *Novelty*

2.1 Document D1 describes circuitry including a diode structure which comprises the features defined by the wording of the precharacterising part of Claim 1. The diode of this prior art has a "critical thin layer" which should be desirably less than 7.3×10^5 nm thick when doped at 10^{13} atoms/cc and less than 2.3×10^4 nm thick when doped at 10^{16} atoms/cc. In the diode claimed in Claim 1 on the other hand the "critical thin layer" is about four orders of magnitude thinner and has a

higher doping concentration by about two orders of magnitude.

2.2 The diodes disclosed in the other documents of the European Search Report have layer structures which are different from the NPIN or PNIP structures claimed.

2.3 Thus, the subject-matter of Claim 1 is considered novel in the sense of Article 54 EPC.

3. *Inventive step*

3.1 Starting from the closest prior art circuitry according to document D1, the objective problem underlying the present invention is to provide a new and improved circuitry including a diode structure which is operative at zero volts DC bias with a high detection efficiency; see the description, page 3, lines 8 to 10.

3.2 This problem is solved by the features claimed in the characterising part of Claim 1 comprising in particular the features that "said critical thin layer is between 2.5 and 14 nn in thickness and the doping level in said critical thin layer is of the order of $8x10^{15}$ atoms/cc". These values of the thickness and impurity concentration of the critical thin layer, in the Board's view, are the decisive parameters, which enable the conventional diode structure of document D1 to be operated without DC bias. In the Board's view, a skilled person would clearly conclude from the presence of DC bias 31 between electrodes 22 and 21 in the circuitry of Figure 9 of document D1 that a bias source should not only be present in the anti-parallel diode combination but is indispensable also in a practical detector application of one diode element only. There is no statement to the contrary in document D1. Hence, the examination of an inventive step underlying the subject-matter of Claim 1

reduces to the question whether it is obvious for a skilled person, that a thickness reduction of about four orders of magnitude combined with an increase of the dopant concentration by two orders of magnitude would allow to dispense with the conventionally necessary DC bias source in the use of the conventional diode structure of document D1 for detection purposes.

3.3 Though document D7 teaches clearly that a barrier height in the region of 0.15 volts makes a Schottky diode suitable for use without DC bias as a detector at microwave frequencies, it appears doubtful to the Board that a skilled person would generalise such statement and come to the conclusion that such barrier height creates sufficient non-linearity of the current-voltage characteristics such as necessary for high detection efficiency in both, in a rectifying junction caused by diverging work functions in the metal-semiconductor interface of a Schottky diode (D7), and in the rectifying junction caused by a depleted semiconductor area in the vicinity of a pn-junction (D1).

3.4 In the NIPIN structure of document D3, the thickness of the critical p^+ layer 12 (d_3) is disclosed to have no *prima facie* influence on the resulting barrier height. Document D3 in formula (1) of column 3 offers a skilled person a theoretical expression of the built-in potential $\varnothing_{B0}$, which is only dependent on the thicknesses d_1 and d_2 of the adjacent intrinsic layers and proposes the skilled person to design the zero barrier height $\varnothing_{B0}$ for a particular device application through appropriate choices of the space charge density in the critical thin layer and appropriate choices of the thicknesses of the two intrinsic layers adjacent to the critical thin one; see in particular D3, column 4, lines 39 to 42. Above all, document D3 gives a skilled person no hint at all that via such $\varnothing_{B0}$ tailoring a bias may be omitted.

3.5 Also document D4 is silent about the fact that in a n^+p^-n mesa diode an appropriate tailoring of the critical thin p^+ layer would allow to create an efficient detector means which operates without DC bias. Hence, a skilled person is regarded to have no realistic motive to extrapolate the theoretical values of the barrier of zero bias in Table 1 to lower values. In the Board's view the teaching of Table 1 of document D4 is limited to the theoretical information that in this diode the barrier height decreases with decreasing thickness of the critical thin p^+ layer. The only experimental values of this conventional n^+p^+n-diode have been measured at -20V bias, see Table 1. The technically applicable teaching of document D4 concerns the fact that such diodes produced with barrier heights from 0.55 eV to 0.94 eV have a high quality as demonstrated by the low ideality factor $(1-(\partial Ø/\partial V)]^{-1}$ measured, see page 183, left column, last two lines. In the Board's view, parameters of a special thickness region (2.5 to 14 nm) and a particular dopant concentration (4.10^{18} atoms/cc) of a p^+layer in an n^+p^-n structure, being known for an advantageous dependence of the barrier height from the applied voltage, give no hint to a skilled person that a use of further modified values as parameters for the critical thin layer in an NPIN or PNIP structure creates a detector diode which is operable at zero volts DC bias.

3.6 The remaining documents cited in the European Search Report are less relevant.

3.7 For the reasons set out above in paragraphs 3.1 to 3.5, the subject-matter of Claim 1 is considered to involve an inventive step in the sense of Article 56 EPC.

4. Thus, Claim 1 is allowable under Article 52(1) EPC. Dependent Claims 2 to 6 concern particular embodiments

of the device claimed in Claim 1 and are, therefore, likewise allowable.

5. With reference to the letter filed on 8 December 1993 which is referred to in paragraph IX above, the decision which was announced at the oral hearing on 7 December 1993 settled the text of Claim 1 of the application, subject to application of the provision in Rule 89 EPC. In the present case, the Board agrees that there is a linguistic error in Claim 1 as filed during the oral proceedings which should be corrected pursuant to Rule 89 EPC by replacing the words "on the other surface" in sub-paragraph (e) of Claim 1 (see paragraph VI above, by the words "on a surface".

Consequently feature (e) as set out in paragraph VI shall read as follows:

"e) a first ohmic contact (22) disposed on a surface of said layer (20) of said opposite conductivity type semiconductor material;"

Order

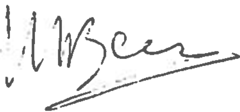
For these reasons, it is decided that:

1. The decision of the Examining Division is set aside.

2. The case is remitted to the first instance with the order to grant a patent on the basis of the following text:

Claims:	1 to 6, filed during the oral proceedings on 7 December 1993, wherein Claim 1 is amended as stated in paragraph 5 above;
Description:	pages 7 and 12 as originally filed, pages 1, 2, 8 and 9 as filed on 26 February 1991, pages 3, 4, 5, 6, 10 and 11 filed during the oral proceedings on 7 December 1993;
Drawings:	sheets 1/4 to 4/4 as originally filed, but with amendment to Figure 4B.

The Registrar:



M. Beer

The Chairman:

G.D. Paterson