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DECISION
of 17 March 1995

Case Number: T0574/92 - 3.4.1

Application Number: 86106981.3

Publication Number: 0208877

IPC: H01L21/00

Language of the proceedings: EN

Title of invention:

Method of manufacturing semiconductor devices having connecting areas

Applicant:

SONY CORPORATION

Opponent:

-

Headword:

-

Relevant legal provisions:

EPC Art. 56

Keyword:

"Inventive step (no), obvious combination of method steps"

Decisions cited:

T 37/82, OJ EPO 84,71

Headnote/Catchword:

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Case Number: T 0574/92 - 3.4.1

D E C I S I O N
of the Technical Board of Appeal 341
of 17 March 1995

Appellant:

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Decision under appeal:

Decision of the Examining Division of the European
Patent Office dated 14 February 1992 refusing
European patent application No. 86106981.3
pursuant to Article 97(1) EPC.

Composition of the Board:

Chairman: G. D. Paterson
Members: H. J. Reich
Y. J. F. Van Henden

Summary of Facts and Submissions

I. European patent application No. 86 106 981.3 (publication number 0 208 877) was refused by a decision of the Examining Division in respect of Claim 1 filed on 7 January 1991, and Claims 2 to 20 as originally filed.

II. The reason given for the refusal was that Claim 1 did not satisfy Articles 52(1) and 56 EPC with regard to documents:

D1: EP-A-0 010 624 and

D2: EP-A 0 144 762.

In its decision the Examining Division furthermore established in paragraph 11 that dependent Claims 2 to 20 did not contain any additional features which, in combination with the features of any claim to which they refer, involved an inventive step for the reasons set out in paragraph 5.2 of its communication dated 27 June 1990 (the appealed decision reads "27.06.91" which is an obvious clerical error). In this paragraph, the Examining Division stated that it can be derived from document D2, page 5, line 27 to page 7, line 3; page 15, line 29 to page 17, line 5 and figures 11 to 13, that inter alia the features of Claim 2 have already been employed for the same purpose in the similar method disclosed in document 2.

III. The Examining Division based its above view essentially on the following grounds and evidence: Document D1 which is considered to be the closest prior art, discloses in Figures 1A to 1E and pages 5 and 6 a method of forming minute gaps for the fabrication of semiconductor devices which comprises steps (a) and (e) to (i) claimed in Claim 1; see also below paragraph VI. Formulating the

problem underlying the application - providing electrical connections from a relatively large external electrode to a small active region for high speed operation - does not contribute to inventive step. It is well known in the art that the operating speed of a transistor can be improved by reducing the size of the active regions and by contacting them via an external connection; see for instance the background art in the application according to figure 1A and figure 1B and the description on page 1, line 30 to page 2, line 19 or document D2, page 1 to page 4, line 15. Since document D2, page 5, line 27 to page 7, line 3 discloses to solve the same problem as in the present application by steps (b) to (d) of Claim 1, a skilled person would regard it as a normal design option to implement into the method disclosed in document D1 steps (b) to (d) disclosed in document D2 and thereby produce the windows according to figure 10 of document D2 by means of the measures described in document D1. Applying additionally the features of Claim 2 - i.e. measures (j) to (m) (see below paragraph VI) - and thus arriving at the method claimed in Claim 2 would be obvious, since these measures have already been employed for the same purpose in the similar method according to document D2; see in particular vertical conductive layer 62 in figure 12, which connects narrow active device region 56 to patterned horizontal conductive layer 22. Where it is desirable to form a minute gap on the surface of an active area for connecting the active area to a conductive layer in alignment with the active area in order to eliminate the mask fitting space or to reduce the parasitic capacitance, the skilled person would routinely use the method steps of document D2 in a semiconductor process according to Claim 2.

IV. The Appellant filed an appeal against this decision. With his Statement of Grounds of Appeal he filed an amended Claim 1, which combines the features of Claims 1 and 2 underlying the appealed decision - i.e. steps (a) to (m) mentioned in paragraph III above in their identical wording - and renumbered the dependant Claims 3 to 20 underlying the appealed decision into Claims 2 to 19.

V. The Appellant requests that a patent be granted on the basis of Claims 1 to 19 filed with the grounds of appeal on 12 June 1992.

VI. Claim 1 filed on 12 June 1992 reads as follows:

"1. A method of manufacturing a semiconductor device, comprising the following steps of:

(a) forming a first insulating layer (5) on a semiconductor substrate including at least one active area (6, 6A);

(b) selectively forming a first conductive layer (9) on said first insulating layer (5);

(c) forming a second insulating layer (16) on said first conductive layer (9);

(d) forming at least one window (25, 26) through said first and second insulating layers (5, 16) and said first conductive layer (9) on said active area (6, 6A) the sidewall of said window (25, 26) being perpendicular to a surface of said semiconductor substrate;

(e) forming a third insulating layer (17) on said active area exposed through said active area window;

(f) forming an oxide resistant layer (18) all over said semiconductor substrate;

(g) anisotropically etching said oxide resistant layer (18) so as to leave said oxide resistant layer (18) only at a side wall portion of said window (25);

(h) oxidizing said semiconductor substrate with said remaining oxide resistant layer (18) as a mask to change said third insulating layer (17) to a fourth insulating layer (19); and

(i) selectively etching said remaining oxide resistant layer (18) and said third insulating layer (17) just under said remaining oxide resistant layer (18) to form a minute gap (18g) on the surface of said active area for connecting said active area (6) to said first conductive layer (9) to be connected to an electrode of said semiconductor device.

(j) forming a second conductive layer (20) all over the semiconductor substrate so as to connect said first conductive layer (9) and the exposed surface of said active area through said formed minute gap (18g);

(k) injecting an impurity to said second conductive layer (20) selectively to diffuse said impurity to said semiconductor substrate so as to form a graft active area (18w);

(l) etching said second conductive layer (20) so as to leave said second conductive layer (20) only at said side wall portion of said windows (25, 26); and

(m) injecting an impurity into inside of said graft active area on said semiconductor substrate to form an intrinsic active area".

Claims 2 to 19 are dependent on Claim 1.

VII. In support of his request the Appellant argued essentially as follows:

(a) The technique suggested by the invention is used to produce the graft **base** area and does not make use of the method described in document D1 for forming small structures wherein a stepped film is etched away such that it is only left in the relatively

small step area where it serves as a mask. Moreover, document D1 only shows how to produce a very narrow emitter area (56 in figure 3E).

- (b) The invention uses the opening obtained in the silicon dioxide neither as a window for thermodiffusion from the gas phase as in document D1 nor as a mask opening for ion implantation as in document D2 but for selectively diffusing into the semiconductor substrate an impurity which was injected into the contacting second conductive layer as claimed in step (k).
- (c) Document D2 describes the fabrication of a lateral bipolar transistor, whereas the subject-matter of the application refers to the fabrication of a bipolar transistor with a buried collector layer (subcollector).
- (d) Document D2 does not provide any clue how it can be avoided that, when the width of the emitter is reduced, the width of the graft base increases by the same magnitude.

Reasons for the Decision

1. Inventive Step

- 1.1 The Board follows the technical interpretation of document D1 by the Examining Division as set out in paragraph III above in that document D1 discloses in accordance with the wording of Claim 1:

"A method of manufacturing a semiconductor device comprising the following steps of:

- (a) forming a first insulating layer (see D1, 12 in fig. 1A) on a semiconductor substrate (10) including at least one active area (implicitly present in view of the "channel" mentioned in line 31 of page 6 for which "stop" region 20 is produced)...
- (d) forming at least one window (beginning at the border between layers 12 and 15 in fig. 1B; see also page 5, lines 13 to 17) through said first... insulating layer...on said active area, the sidewall (see the lefthand border of layer 12 in fig. 1B) of said window being perpendicular to a surface of said semiconductor substrate;
- (e) forming a third insulating layer (15 in fig. 1B) on said active area exposed through said active area window;
- (f) forming an oxide resistant layer (14 in fig. 1B, consisting of Si₃N₄ according to D1, page 5, line 27 as in the embodiment of Claim 1 disclosed in the description of the present application page 10, line 3) all over said semiconductor substrate;
- (g) anisotropically etching said oxide resistant layer (D1, page 6, lines 2 to 9) so as to leave said oxide resistant layer (14 in fig. 1C) only at a side wall portion of said window;
- (h) oxidising (page 6, lines 9 to 15) said semiconductor substrate with said remaining oxide resistant layer (10) as a mask to change said third insulating layer to a fourth insulating layer (16 in fig. 1D)
- (i) selectively etching said remaining oxide resistant layer (page 6, lines 15 to 18) and said third insulating layer (page 6, lines 18 to 21) just

under said remaining oxide resistant layer to form a minute (see the embodied width of 100nm in the description of the present application, page 8, line 31 and the lower limit of 100nm disclosed in D1, page 6, line 26) gap (18 in fig. 1E) on the surface of said active area."

1.2 The Appellant's arguments in paragraph VII-(a) above are regarded as not relevant since the Examining Division and the Board do not start from the method disclosed in Figures 3A to 3F but in Figures 1A to 1E of document D1. Furthermore, Claim 1 is not limited to any specific active area, (see in particular the wording of steps (k) and (m) of Claim 1), so that the Appellant's arguments based on a specific active area such as a base or a graft base area, cannot support an inventive step underlying the subject-matter of Claim 1. Hence, the Appellant's argument stated in paragraph VII-(d) above cannot be taken into consideration by the Board. Contrary to the Appellant's view in paragraph VII-(a), the etching of a stepped film leaving only a mask part follows clearly from Figures 1D and 1E of document D1; see the stepped film 16, 15 in Figure 1D and the remaining mask part 16 in Figure 1E.

1.3 Starting from the conventional method disclosed in Figures 1A to 1E of document D1 as closest prior art, the objective problem underlying the subject-matter of Claim 1 has to be seen in the provision of a method for manufacturing a semiconductor device wherein the contacting steps of an active device area in the semiconductor substrate allow to eliminate mask fitting space and to reduce the parasitic capacitance of the contacting non-active device areas in order to manufacture high speed and large scale integrated (LSI) devices; see the description of the present application, page 2, line 25 to page 3, line 1. The Board follows the

Examining Division in that this objective problem is known from the background art of the present application according to Figure 1A and Figure 1B and the corresponding description, page 1, line 30 to page 2, line 19 and that, for this reason, the objective problem does not contribute to an inventive step underlying the subject-matter of Claim 1; see also paragraph III above.

1.4 The above problem is solved by combining the method steps set out in paragraph 2.1 above with steps (b), (c), the features defined by the remaining wording of steps (d) and (i), step (j), partially step (k), and step (l) as claimed in Claim 1. The Board follows the Examining Division in that these steps are known from the similar method disclosed in document D2; see paragraph III above. The particular measures of these steps in their claimed wording can be derived from document D2 - in line with the grounds set out by the Examining Division and stated in paragraph III - as follows:

- "(b) selectively forming a first conductive layer (see D2, 22 in Fig. 10A) on said first insulating layer (20 in Fig. 10A);
- (c) forming a second insulating layer (24) on said first conductive layer (22);
- (d) forming at least one window (see the exposed surface of substrate 10 in Fig. 10A) through said first and second insulating layers (20, 24) and said conductive layer (22)... the sidewall of said window being perpendicular to a surface of said semiconductor device (see both borders of layer structure 20, 22, 24, in Fig. 10A);"
- (i) ...forming a gap (see the exposed surface of substrate 10 Fig. 10A)..." for connecting said active area (56 in Fig. 15A) to said first

conductive layer (22 in Fig. 15A) to be connected to an electrode (80 in Fig. 15A) of said semiconductor device;

- (j) forming a second conductive layer (60, 62 in Fig. 11) all over the semiconductor substrate so as to connect said first conductive layer (22) and the exposed surface of active layer (56 in Fig. 11) through said formed...gap (the fact that the gap is "minute" as claimed follows from its formation by steps (e) to (i) disclosed in document D1; see para. 2.1 above);
- (k) injecting an impurity (see D2, page 15, lines 22 to 26)... so as to form a graft active area (56 in Fig. 11);
- (l) etching said second conductive layer (60, 62) so as to leave said second conductive layer (62 in Fig. 11 and 12) only at said side wall portion of said windows;"

1.5 The remaining features claimed in step (k) of Claim 1, i.e. injecting an impurity "to said second conductive layer selectively to diffuse said impurity to said semiconductor substrate" represents only an alternative measure to the ion implantation step of document D2 (page 15, line 23) in order to produce the claimed "graft active area". Since prima facie the lateral dimensions of the graft active area are dependent on the width of gap and not on the particular measure by which the corresponding impurities are driven through said gap into the substrate-i.e. by outdiffusing from the second conductive layer as claimed or by implanting before deposition of the second conductive layer as disclosed in document D2 - the Board regards said remaining features claimed in step (k) as not contributing to the solution of the objective problem underlying Claim 1. According to the established case law of the Board of Appeal of the EPO, features which do not contribute to

the solution of the problem set in the description, are not to be considered in assessing the inventive step of a combination of features; see for instance T 37/82, OJ EPO 1984, 71. Being not part of the solution, the diverging technique for the impurity injection falls under the similarity aspect of the claimed and conventional methods as already stated by the Examining Division (see paragraph III above). Therefore, the Appellant's argument according to paragraph VII-(b) is held not to be able to support an inventive step underlying the subject-matter of Claim 1. Moreover, the production of a graft active area by outdiffusion from its contacting conductive layer is generally known; see the background art of the present application according to Figure 1B, in particular the description page 8, lines 5 to 7. In this text the Appellant explicitly admits that said outdiffusion technique is "usual" for forming a graft active area. The injection technique claimed in step (k) is thus at the free disposal of a skilled person and its use in step (k) has to be regarded as obvious.

- 1.6 Since the subject-matter of Claim 1 is not restricted to the fabrication of a bipolar transistor with a subcollector, the Appellant's argument set out in paragraph VII-(c) has to be regarded as not relevant.

- 1.7 Step (m) claimed in Claim 1 restricts the subject-matter of Claim 1 to a specific property (i.e "intrinsic") of the claimed active area which has no influence on the parasitic capacity of its connecting inactive parts and does not allow to eliminate mask fitting space. Being no element of the solution of the problem set in the description, step (m) of Claim 1 causes only a similarity between claimed and conventional method and

therefore has to be disregarded in the assessment of inventive step. Moreover step (m) is part of the background art disclosed in Figure 1B of the present application (see intrinsic base 7.)

- 1.8 A skilled person can easily derive from the metallization structure of the device in Fig 15A that the contact forming steps mentioned in paragraph 2.4 above and disclosed in document D2, would allow to solve the objective problem set out in paragraph 2.3 above. Thus, a skilled person has a clear motive to combine them with the manufacturing steps set out in paragraph 2.1 above and to make additionally use of the advantageous "minute" dimensions of the contact opening which are achievable by the method disclosed in document D1.
2. For the above reasons, in the Board's judgement, Claim 1 does not involve an inventive step and is not allowable pursuant to Articles 52 (1) and 56 EPC. Claims 2 to 19 fall because of their dependence on Claim 1.

Order

For these reasons it is decided that:

The appeal is dismissed.

The Registrar:

The Chairman:

M. Beer

G. D. Paterson

