BESCHWERDEKAMMERN DES EUROPÄISCHEN PATENTAMTS

BOARDS OF APPEAL OF THE EUROPEAN PATENT OFFICE

CHAMBRES DE RECOURS DE L'OFFICE EUROPEEN DES BREVETS

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File Number: T 69/92 - 3.5.2

Application No.: 84 307 563.1

Publication No.: 0 144 158

Title of invention: Integrated circuit timing apparatus

Classification: H03L 7/08

D E C I S I O N
of 14 January 1993

Applicant: INMOS LIMITED

Opponent: Deutsche ITT Industries GmbH, Frieburg

Headword:

EPC Articles 56, 114(2) and 123(2) and (3)

Keyword: "Inventive step - yes, after further amendment"
"Amendments appropriate and admissible"
"Documents produced in oral proceedings disregarded"

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Beschwerdekammern | Boards of Appeal | Chambres de recours

Case Number : T 69/92 - 3.5.2

D E C I S I O N
of the Technical Board of Appeal 3.5.2
of 14 January 1993

Appellant : (Opponent)
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Decision under appeal :
Interlocutory decision of the Opposition Division of the European Patent Office dated 22 November 1991 concerning maintenance of European patent No. 0 144 158 in amended form.

Composition of the Board :

Chairman : E. Persson
Members : W.J.L. Wheeler
M.R.J. Villemin

Summary of Facts and Submissions

I. The Appellant opposed European patent No. 0 144 158 and now contests the interlocutory decision of the Opposition Division that, account being taken of the amendments made during the opposition proceedings, the patent and the invention to which it relates meets the requirements of the EPC.

II. In the appeal proceedings, the Respondent made further amendments to the claims and description. There are now three independent claims, Claims 1, 21 and 23, worded as follows:

"1. An integrated circuit device comprising a timing apparatus (4) for a logic device (2) said timing apparatus having an output (5) connected to supply a high frequency output timing signal to said logic device, said timing apparatus (4) comprising a phase locked loop arranged to produce said output timing signal whose frequency is a multiple of the frequency of an input clock signal, wherein said phase locked loop comprises comparator means (7) having a first input to which said input clock signal is applied, a second input, and output means on which comparison signals are provided, a divider (8) having an input connected to receive said output timing signal and an output connected to said second input of the comparator means (7) said divider (8) being arranged to divide the frequency of said output timing signal by a predetermined integer, and a voltage controlled oscillator (12) arranged to be controlled in dependence upon said comparison signals to produce said output timing signal at its output, the output of said voltage controlled oscillator (12) being connected to the input of said divider (8) wherein said timing apparatus (4) has an input (6) connected to one input pin (3') for receiving said input

clock signal, said comparator means (7) has two outputs (9,10) on which said comparison signals are provided, one to increase the frequency and the other to decrease the frequency of the voltage controlled oscillator, said phase locked loop includes converter and filter means (11) connected to receive the comparison signals (9,10) and arranged to generate a voltage signal (27) whose magnitude is determined by the comparison signals, said voltage controlled oscillator (12) being controlled by said voltage signal (27), said converter and filter means (11) includes a first current source circuit (18,19,20,21) connected to receive one comparison signal (9) of the comparator means (7) and including a first current source transistor (19) operable in response to said one comparison signal (9) to vary said voltage signal (27) to increase the frequency of the oscillator (12), a second current source circuit (23,24,25,26) connected to receive the other comparison signal (10) of the comparator means (7) and including a second current source transistor (24) operable in response to said other comparison signal to vary said voltage signal (27) to decrease the frequency of the oscillator (12) and a current reference circuit (13), characterised in that said integrated circuit device further comprises a logic device (2) to which a plurality of input and output pins (3) are connected, both the said logic device (2) and said timing apparatus (4) being completely formed on a common single chip (1), and in that the current reference (13) has first and second current mirror circuits (30,31) (28,29) connected respectively between a power supply and ground, a first current mirror transistor (31) in the first current mirror circuit being coupled to said first current source transistor (19) and controlling the current value in said first current source transistor (19), and a second current mirror transistor (28) in the second current mirror circuit coupled to said second current source transistor (24) and controlling the

current value in said second current source transistor (24), and the output (5) of said voltage controlled oscillator (12) is directly connected to said logic device (2) to supply thereto high frequency output timing signals of at least 40MHz."

"21. A method of supplying timing signals to an integrated circuit logic device (2) comprising the steps of applying a low frequency clock signal to an input (6) of a timing apparatus, the timing apparatus being arranged to generate a high frequency timing signal at its output (5) having a frequency which is a multiple of that of said clock signal, dividing the frequency of said high frequency timing signal by a predetermined integer, comparing the divided frequency with the frequency of the clock signal, generating an increase or decrease comparison signal (9,10) where the clock signal frequency is respectively greater than or less than said divided frequency, using said increase and decrease comparison signals to switch respective current sources (19,24) and generate a D.C. voltage whose magnitude is determined by said increase and decrease comparison signals, and generating the high frequency timing signal at the output (5) of a voltage controlled oscillator (12) in dependence upon said comparison signals, characterised in that the timing apparatus employed is formed with the logic device (2) on a common single chip, and in that current flow through each of said current sources is controlled by a respective current mirror circuit (28,29,30,31) and in that the high frequency timing signal at the output of said voltage controlled oscillator is at least 40MHz and is connected directly to said logic device (2) to form the timing signal therefor."

"23. A method of supplying timing signals to an integrated circuit logic device (2) comprising the steps

of applying a low frequency clock signal to an input (6) of a timing apparatus, the timing apparatus being arranged to generate a high frequency timing signal at its output (5) having a frequency which is a multiple of that of said clock signal, dividing the frequency of said high frequency timing signal by a predetermined integer, comparing the divided frequency with the frequency of the clock signal, generating an increase or decrease comparison signal (9,10) where the clock signal frequency is respectively greater than or less than said divided frequency, using said increase and decrease comparison signals to switch respective current sources (19,24) and generate a D.C. voltage whose magnitude is determined by said increase and decrease comparison signals, and generating the high frequency timing signal at the output (5) of a voltage controlled oscillator (12) in dependence upon said comparison signals, characterised by controlling the current flow in each current source (19,24) by use of a programmable current reference circuit (13) including a current mirror circuit (28,29,30,31) for each of said current sources, determining the operating speed of the logic device (2) and programming the current reference circuit (13) to provide a high frequency output signal of at least 40MHz which matches said operating speed and supplying said high frequency output signal to the logic device (2) which is formed with the timing apparatus on a common single chip."

III. In the Statement of Grounds of Appeal, the Appellant argued essentially that the decision under appeal was based on an incorrect assessment of the closest prior art document EP-A-0 072 751 (D2). Contrary to paragraph 3(i) of the impugned decision, D2 disclosed the combination on a single chip of a codec and timing apparatus including a phase locked loop (see page 1, lines 24 and 25, page 1, line 34 to page 2, line 11, and "A single-chip codec with

switched-capacitor filters" cited in the search report of D2). Moreover, contrary to paragraph 3(ii) of the impugned decision, D2 disclosed a comparator (1, Figure 1) with two outputs (c, d), one to increase the frequency (when c = 0) and the other to decrease the frequency (when d = 0) of the voltage controlled oscillator (3), see D2, page 4, lines 5 to 26. The choice of positive instead of negative logic was not inventive. Thus, the Appellant argued that the subject-matter of Claim 1 in the form maintained by the Opposition Division did not involve an inventive step.

The Appellant also argued that the Opposition Division had committed a substantial procedural violation in not considering whether the requirements of Article 123(3) EPC had been met. The newly introduced Claim 22 (now Claim 20) extended the protection to cover combinations with analogue MOS circuits.

IV. The Respondent pointed out that Claim 22 objected to by the Appellant could not extend the protection because it was dependent on Claim 1. It merely specified that the integrated circuit device, which according to Claim 1 comprised a logic device, comprised a MOS device.

The Respondent accepted that D2 disclosed more features of the present invention than had been acknowledged in the proceedings before the Opposition Division and amended the claims to take account of this. Regarding inventive step, the Respondent argued essentially that although D2 disclosed a phase locked loop formed as an integrated circuit and mentioned that it may be used for a codec, it did not disclose a codec, or any other logic circuit, on the same chip as the phase locked loop. D2 was concerned with reducing the size of the necessary capacitors so that they could be integrated on the same chip as the phase

locked loop whose output frequency was 128 kHz. The present invention, subject-matter of the claims as amended during the appeal proceedings, used two reference current mirror circuits to solve the different problem of reducing phase jitter when timing signals of a frequency of at least 40 MHz were produced on chip. This was not disclosed in D2.

V. During oral proceedings held on 14 January 1993, the Appellant argued essentially that Claim 1 of the patent in suit had three characterising features:

(a) everything on one chip,
(b) current mirror circuits,
(c) frequency at least 40 MHz.

Regarding (a), it was already known from D2's search report to put a codec and its timing circuit on one chip. Regarding (b), D2 showed two current source transistors (Q10, Q11) in Figure 5A. Regarding (c), there was no disclosure in the application as originally filed that the frequency could be above 40 MHz with no upper limit, only the range 40 to 100 MHz was disclosed. A phase locked loop producing an output frequency of tens of MHz was known from DE-A-2 739 035 (D3), cited in the notice of opposition. To support the argument concerning feature (a) the Appellant sought to introduce into the appeal proceedings the paper "A single-chip codec with switched-capacitor filters" cited in the search report of D2 and four further references cited in that paper. The Board decided to disregard these new documents.

VI. The Respondent replied that integrated logic circuits produced noise on the substrate which affected the positions of the edges of clock signals when these were

generated on chip. With a clock frequency of 128 kHz, as in D2, clock edge jitter of 50 ns could be tolerated. But with a frequency of 40 MHz, jitter 2 or 3 ns would cause clock ambiguity. The present invention reduced the jitter to an acceptable level by using current mirror circuits to control the current in the current sources. In D2, the current flow through transistors Q10 and Q11 was set by a potential divider (Q7, Q8, Q9, Figure 5A, or Q7, R10, Q9, Figure 6A) which could not compensate for noise on the substrate. The application as originally filed contained an example where the frequency was 40 to 100 MHz, but there was no suggestion that 100 MHz was a necessary upper limit.

VII. The Appellant requests that the interlocutory decision of the Opposition Division be set aside and that the patent in suit be revoked in its entirety.

VIII. The Respondent requests that the patent be maintained on the basis of the following documents:

- Claims 1, 21 and 23 as presented in the oral proceedings.
- Claims 2 to 20 and 22 as filed on 10 September 1992.
- Description as printed in the patent specification, with the text from column 1, line 48, to column 2, line 54, inclusive, being replaced by pages 2a, 2b and 2c as presented in the oral proceedings.
- Drawings as printed in the patent specification.

Reasons for the Decision

1. The appeal is admissible.

2. Before coming to the question of inventive step, the Board will consider the Appellant's objections relating to the amendments made to the claims and the alleged procedural violation.

2.1 It is true that, as pointed out by the Appellant, there is no explicit reference to Article 123(3) EPC in the decision under appeal. Nevertheless, it is clear from paragraph 9 of the impugned decision that the Opposition Division was of the opinion that the amended patent and the invention to which it related met the requirements of the EPC. From this it may be inferred that they were of the opinion that the amendments complied with Article 123(3) EPC. The lack of an explicit reference to Article 123(3) EPC does not constitute a substantial procedural violation.

2.2 The Appellant objected to the introduction of the feature "at least 40MHz" into the independent claims. The Board notes that the claims as granted did not specify a lower or an upper frequency limit for the timing signal. The figure 40 MHz appears towards the end of the description as originally filed as the lower limit of the range 40 - 100 MHz, mentioned by way of example. The effect of the phrase "at least 40MHz" in the independent claims is to restrict the protection by disclaiming frequencies less than that. In the opinion of the Board, the disclaimer of frequencies below 40 MHz does not oblige the Respondent to disclaim frequencies above 100 MHz as well. Thus, the introduction of "at least 40MHz" into the claims does not infringe paragraph (2) or (3) of Article 123 EPC.

2.3 The Appellant objected to the introduction of Claim 22 (now Claim 20). As the Respondent has pointed out, this claim cannot extend the protection because it is properly dependent on Claim 1. It specifies a further, cumulative restriction, namely that the integrated circuit device comprises a MOS device. It does not free it from any of the features specified in Claim 1. It is clear from the originally filed description that the device may be a MOS device. Thus, Claim 20 does not infringe paragraph (2) or (3) of Article 123 EPC.

2.4 In the opinion of the Board, the amendments made to the claims may be regarded as an appropriate response to the opposition and appeal. The description has been amended only to the extent necessary to acknowledge the prior art cited by the Appellant and to adapt it to the present form of the independent claims. In the opinion of the Board, the amended form of the patent in suit complies with paragraphs (2) and (3) of Article 123 EPC.

3. Turning now to the question of inventive step, both the parties and the Board are in agreement that the closest prior art is disclosed in EP-A-0 072 751 (D2). There is also agreement that D2 discloses an integrated circuit device having all the features recited in the prior art portion of Claim 1 of the patent in suit.

3.1 However, there is disagreement as to whether D2 also discloses the feature of the logic device and the timing apparatus both being completely formed on a common single chip. As pointed out by the Appellant, D2 mentions that the phase locked loop (PLL) circuit is itself in the form of an integrated circuit and is used for a coder-decoder circuit. However, there is no disclosure in D2 of the PLL circuit being formed on the same chip as the codec. The citation of "A single-chip codec with switched capacitor

filters" in the search report of D2 is a separate piece of information which, although published in D2, is not disclosed as a feature of the circuits described in D2.

3.2 The Appellant sought to support the contention that it was already known to integrate a codec and a PLL on a single chip by introducing the citation "A single-chip codec with switched-capacitor filters" and four further documents into the proceedings. The Board considers that these documents, produced for the first time in the oral proceedings, were not submitted in due time and are not sufficiently relevant to have a substantive effect on the outcome of the appeal. The Board therefore exercises its discretion under Article 114(2) EPC to disregard them.

3.3 The subject-matter of the present independent claims differs from the prior art known from D2 in that the timing apparatus is formed with the logic device on a common single chip, current flow through each of the current sources is controlled by a respective current mirror circuit and the high frequency timing signal at the output of the voltage controlled oscillator is at least 40 MHz and is connected directly to said logic device to form the timing signal therefor.

3.4 The circuits disclosed in D2 produce timing pulses having a frequency of 128 kHz. As explained by the Respondent, the amount of imprecision in the edges of the timing signals, or clock edge jitter, which can be tolerated at 40 MHz is much less than at 128 kHz.

3.5 The present invention solves the problem of reducing the clock edge jitter to a level which is tolerable at clock frequencies of 40 MHz and higher by the use of respective current mirror circuits to control the current flowing through the current sources.

3.6 In the opinion of the Board, even if, for the sake of argument and to the advantage of the Appellant, it is assumed to have been known to integrate a logic device and a PLL providing 128 kHz timing signals therefor on a single common chip, and taking into account the fact that PLL circuits operating at tens of MHz were known per se (see D3 cited by the Appellant) and that current mirrors were also known per se, it would not have been obvious to the person of average skill in the art to modify any of the timing circuits known from D2 to operate at 40 MHz (that is, to increase its output frequency by a factor of more than 300) and to reduce the jitter in the output of the voltage controlled oscillator to a tolerable level by replacing the circuits for controlling the current flow through the current sources (Q10, Q11) of D2 (see Figures 5A, 6A and 6B) by respective current mirror circuits.

3.7 Thus, in the opinion of the Board, the integrated circuit device according to Claim 1 and the methods according to Claims 21 and 23 of the patent in suit are novel and involve an inventive step over the cited prior art. The patent may be maintained with these claims. The same applies to the dependent Claims 2 to 20 and 22.

4. In the result, the Board is of the opinion that the patent may be maintained in amended form as requested by the Respondent.

Order

For these reasons, it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the first instance to maintain the patent in amended form as requested by the Respondent (see paragraph VIII above).

The Registrar: The Chairman:

M. Kiehl E. Persson