BESCHWERDEKAMMERN DES EUROPÄISCHEN PATENTAMTS

BOARDS OF APPEAL OF THE EUROPEAN PATENT OFFICE

CHAMBRES DE RECOURS DE L'OFFICE EUROPEEN DES BREVETS

Publication in the Official Journal ~~Yes~~ / No

File Number: T 961/91 - 3.5.1

Application No.: 86 401 319.8

Publication No.: 0 206 928

Title of invention:

Classification: G11C 8/00

D E C I S I O N
of 28 April 1992

Applicant: SGS-Thomson Microelectronics, Inc.

Headword:

EPC Article 56

Keyword: "Inventive step (yes)"
"Late filed documents"

Headnote

Europäisches Patentamt | European Patent Office | Office européen des brevets

Beschwerdekammern | Boards of Appeal | Chambres de recours

Case Number : T 961/91 - 3.5.1

D E C I S I O N
of the Technical Board of Appeal 3.5.1
of 28 April 1992

Appellant : SGS-Thomson Microelectronics, Inc.
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Decision under appeal : Decision of the Examining Division of the European Patent Office dated 2 July 1991 refusing European patent application No. 86 401 319.8 pursuant to Article 97(1) EPC.

Composition of the Board :

Chairman : P.K.J. van den Berg
Members : A.S. Clelland
W.M. Schar

Summary of Facts and Submissions

I. European patent application 86 401 319.8 (publication No. 206 928) was refused by decision of the Examining Division at the end of oral proceedings held on 2 July 1991; the subsequent written decision was dated 15 July 1991.

II. The reason for the refusal was that the subject-matter of the claims considered at the oral proceedings lacked an inventive step having regard to the following documents (using the Examining Division's notation):

D1: EP-A-0 031 672
D3: US-A-3 859 637.

III. An appeal against this decision was received on 19 September 1991. The Appellant (applicant) requested cancellation of the decision and filed a revised set of claims. A Statement of Grounds of Appeal was received on 13 November 1991.

IV. The Appellant's request is based on the following documents:

Claims:	Claims 1 to 4 as filed on 19 September 1991;
Description:	Pages 1 and 3 to 9 as originally filed,
	Page 2b as filed on 16 November 1990
	Pages 2, 2a and 2aa as filed on 19 September 1991;
Drawings:	Sheets 1/2 and 2/2 as originally filed.

V. Oral proceedings were held at the Appellant's request on 28 April 1992.

VI. The claims received on 19 September 1991 include two independent claims, Claims 1 and 3, being respectively a method and an apparatus claim. Claim 1 reads as follows:

"A method of operating an input buffer circuit with low power operation, which method comprises inputting data to a latch circuit (62,64) through a controlled isolation circuit (20), switching said isolation circuit (20) between an active power drawing state when data may be input to the latch circuit (62,64) and an inactive state when power drawing is switched off and data is not input to the latch circuit, and supplying to said isolation circuit an enable signal to switch the isolation circuit to the active state in response to a signal indicative of valid data and later supplying to said isolation circuit (20) a disable signal to render the isolation circuit inactive, wherein said signal indicative of valid data is supplied to a delay circuit (50) which generates after a predetermined delay a latch enable signal to enable the latch circuit, characterised in that when said latch enable signal is generated it is used both to operate the latch circuit (62,64) to store in the latch circuit data which has been input to the latch circuit during the active power drawing state of said controlled isolation circuit (20), and to cause said disable signal to be supplied to the controlled isolation circuit to disable the controlled isolation circuit when the latch enable signal is generated, and in that said delay circuit is arranged to match the said predetermined delay with the time taken for the signal indicative of valid data to cause the enable signal to be supplied to the isolation circuit to switch the latch circuit to the active state and for the data to be input through the isolation circuit into the latch circuit."

VII. Claim 3 reads as follows:

"An input buffer circuit for low-power operation comprising:
controlled isolation means (20) having a first input (16) for receiving a data signal, a second input (46) for receiving an enable or disable signal and an isolation output (32), and further having an active power-drawing state and a normal inactive state dependent on the enable or disable signal;
latch means (62,64) connected to said isolation output for storing the voltage level on said isolation output in response to a latch enable signal on a latch enable node (54);
control means (45), having a control output connected to said second input (46), and having an enabling input (40) for receiving an enabling signal and a disabling input (42) for receiving a disabling signal, for selectively supplying an enable or disable signal to said second input (46); and
delay means (50) arranged to receive said enabling signal which is indicative of valid data being supplied to the circuit and to generate said latch enable signal a predetermined time after said enabling signal is received characterised in that the delay means (50) is arranged to generate said latch enable signal after a delay which is selected to match the propagation time of said enabling signal through the control means (45) and of a data signal through the controlled isolation means (20) and the latch means (62,64) said delay means (50) comprising circuit elements arranged to match the controlled isolation means (20), latch means (62,64) and control means (45) and in that the latch enable signal is used both to operate the latch means (62,64) to hold data input to the latch means and to provide said disabling signal to the control means (45) thereby to supply the disable signal and disable the

controlled isolation means (20) when the latch enable signal is generated."

VIII. The Appellant's representative argued at the oral proceedings that the delay provided by the invention - hereinafter referred to as the "tracking delay" - could not be compared with that used in D1. It was said that Figure 10 of D1 showed that the delay of D1 was not chosen to match a particular propagation time but to correspond to the time period for which a valid input signal was present at the input of the D1 circuit; this, it was said, could be seen from a comparison of the $\overline{\emptyset}_*$ and A_{in} timing signals in Figure 10. In absolute terms the period for which power was drawn was considerably longer than in the invention, being based on the period for which the input signal was valid; this understanding was said to be reinforced by the fact that the D1 circuit was based on a prior art arrangement disclosed in Figures 1 to 3, in which the reduction of power consumption was not an aim but which nevertheless caused latch operation after the same time period as in the preferred arrangement shown in Figures 6 to 9. Moreover, figure 10 also showed that the latch time, given by the cross-over point of the $\emptyset$ and $\overline{\emptyset}$ signals was approximately at the mid-point of the $\overline{\emptyset}_*$ signal. Since the isolation means could be switched off as soon as the input signal had been latched this showed that the D1 circuit drew current twice as long as was necessary. Thus, although D1 was concerned with reducing power consumption it did not achieve the object of minimising power consumption. The designers of the arrangement known from D1 had not appreciated that a further reduction was possible by matching the delay after which the latch means operated to the propagation time rather than operating the latch at some arbitrary time within the period of a valid input signal. The representative also argued that the nature of the delay

was of significance; in the preferred embodiment of the invention as shown in Figure 3 the delay was a tracking delay making use of components which were analogous to those of the actual circuit as shown in Figure 1. Variations in propagation time caused for example by temperature changes would thus be compensated since corresponding variations would take place in the delay.

Reasons for the Decision

1. The appeal is admissible.

2. Admissibility of amendments

At the oral proceedings the representative referred to a submission including amended claims filed by fax on 24 April 1992, i.e. less than two working days before the oral proceedings. This submission had not been received by the Board prior to the oral proceedings.

The filing of amendments, as pointed out in the "Guidance for Appellants and their Representatives", OJ EPO 1984, 376, at 2.2 "Submission of amendments", "should be done at the earliest possible moment...the Board concerned may, for example, disregard amendments which ... when a date for oral proceedings has been given, are not submitted in good time for the proceedings". T 95/83, OJ EPO 1985, 75, indicates that amendments not submitted in good time are only considered on their merits where there is some clear justification both for the amendment and for its late submission. In the present procedure, the amended claims were not received by the Board prior to the oral proceedings. No good reason was advanced at the oral proceedings as to why the amended claims were filed so late and accordingly they were declared inadmissible on

the basis of Art. 114(2) EPC. The oral proceedings were therefore based on the request set forth at point IV above.

3. Novelty

3.1 Although the following discussion of novelty is primarily based on the wording of Claim 3 it applies also, mutatis mutandis, to Claim 1.

3.2 The most relevant single document is D1. This discloses in connection with Figures 6 to 9 an input buffer circuit which in accordance with the paragraph bridging pages 4 and 5 of the description is for low power operation. This known buffer circuit provides controlled isolation means in the form of a NOR gate $Q_{11,12,14,16}$ having a first input A_{in} for receiving a data signal, a second input for receiving an enable or disable signal $\overline{\phi}_*$, and an isolation output, and further having an active power-drawing state and a normal inactive state dependent on the enable or disable signal. The known arrangement further discloses latch means (13) connected to the isolation output for storing the voltage level on the isolation output in response to a latch enable signal ϕ, $\overline{\phi}$ on a latch enable node, as well as control means in the form of a NAND gate Q_{45-48} having a control output connected to the second input, an enabling input N1 for receiving an enabling signal ($\overline{CE}$ by way of $Q_{31,32}$) and a disabling input for receiving a disabling signal, an enable or disable signal selectively being supplied to the second input. Delay means $Q_{33,34}$, $Q_{35,36}$ receive the enabling signal, which is indicative of valid data being supplied to the circuit, and generate the latch enable signal ϕ, $\overline{\phi}$ a predetermined time after the enabling signal is received.

3.3 Both independent Claims 1 and 3 further include - albeit with different wording - the following two features:

(a) The latch enable signal is used both to operate the latch means so as to store input data and to provide the disabling signal to disable the controlled isolation means when the latch enable signal is generated.

(b) The delay period of the delay means is arranged to match the combined propagation time of the enabling signal through the control means and a data signal through the controlled isolation means and into the latch means.

Neither of these features can be directly and unambiguously identified in the disclosure of D1; the subject-matter of each of independent Claims 1 and 3 is accordingly novel.

4. Inventive step

4.1 It is apparent that D1 does not use the latch enable signal to disable the controlled isolation means when the latch enable signal is generated. In accordance with Figure 6 of D1 the disable signal is generated by a "clock circuit" (15), shown in Figure 8 to comprise a delay circuit formed by CMOS inverters $Q_{41,42}$ and $Q_{43,44}$, together with a NAND gate formed by transistors Q_{45-48} as in the preferred embodiment of the application. From Figure 10 the disabling signal $\overline{\phi}_*$ can be seen to cause the isolation means to be disabled at a time period after operation of the latch means which is approximately as long again as the period between enabling of the isolation means and operation of the latch means, and which is determined by the two CMOS inverters referred to above. It

is not clear to the Board why the D1 arrangement requires an additional delay after latching has taken place before the isolation means are turned off; however, even if for the sake of argument the skilled man would find it obvious to modify D1 so as to remove this additional delay and thereby halve the period during which power is consumed, he would for the reasons given below still not arrive at the invention as claimed.

4.2 Two objectives which the skilled man in the CMOS art must constantly bear in mind in circuit design are the need to keep power consumption as low as possible and the need for fast operation. The D1 arrangement seeks to achieve these objectives by ensuring that latching can only take place within the period during which valid data is present on the circuit input, the time t during which the isolation means enable signal $\overline{\phi}_*$ is supplied being approximately equal in length to the valid input data signal as can be seen from Figure 10. Power consumption in the D1 circuit is accordingly restricted to the time during which a valid input data signal is present. It does not appear to the Board that the skilled man would go further than this without the exercise of invention; in order to arrive at the claimed arrangement it is necessary for the skilled man to appreciate firstly that power consumption can be reduced below the period during which valid data is present and secondly that it can be made dependent only on the overall propagation time needed to enable the isolation means and for the data thereafter to be received by the latch means. Neither appreciation is, in the Board's view, derivable from the teaching of D1 without the exercise of invention. Even if the skilled man were to appreciate that he could halve the time that the NAND gate remains open (see paragraph 4.1 above) the delay would still be based on the valid signal period and not the propagation time.

4.3 Although drafted in a differing language, both independent Claims 1 and 3 include the feature of matching the delay to the propagation time. The subject-matter of each of Claims 1 and 3 accordingly involves an inventive step.

5. Claims 2 and 4 are respectively appendant to Claims 1 and 3 and add further features to these claims, so that their subject-matter also involves an inventive step.

Order

For these reasons, it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the first instance with the order to grant a patent on the basis of the Appellant's request (paragraph IV above).

The Registrar: The Chairman:

M. Beer P.K.J. van den Berg