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Aktenzeichen / File Number / Numéro du dossier

T 453 / 91 - 3.5.1

In der Anlage erhalten Sie

- ☐ eine Kopie des Berichtigungsbeschlusses
- ☐ ein korrigiertes Vorblatt (Form 3030)
- ☐ einen Leitsatz / Orientierungsatz (Form 3030)
- ☐ _____

Please find enclosed

- ☒ a copy of the decision correcting errors
- ☐ a corrected covering page (Form 3030)
- ☐ a headnote / catchword (Form 3030)
- ☐ _____

Veuillez trouver en annexe

- ☐ une copie de la décision rectifiant des erreurs
- ☐ une page de garde (Form 3030) corrigée
- ☐ un sommaire / une phrase vedette (Form 3030)
- ☐ _____

Anmeldung Nr. / Patent Nr.: _____ (soweit nicht aus der Anlage ersichtlich)

Application No. / Patent No.: 90117520.4 (if not apparent from enclosure)

Demande n° / Brevet n°: _____ (si le n° n'apparaît pas sur l'annexe)

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Beschwerdekammern | Boards of Appeal | Chambres de recours

Case Number: T 0453/91 - 3.5.1

D E C I S I O N
of 27 July 1994 correcting errors in the decision of the Technical Board of Appeal 3.5.1 of 31 May 1994

Appellant: International Business Machines Corporation
Old Orchard Road
Armonk, N.Y. 10504 (US)

Representative: Schäfer, Wolfgang, Dipl.-Ing.
IBM Deutschland GmbH
Schönaicher Strasse 220
D-7030 Böblingen (DE)

Decision under appeal: **Decision of the Examining Division of the European Patent Office dated 17 December 1990 refusing European patent application No. 86 117 601.4 pursuant to Article 97(1) EPC.**

Composition of the Board:

Chairman: P. K. J. van den Berg
Members: W. B. Oettinger
F. Benussi

In application of Rule 89 EPC the front page of the decision in the appeal case T 0453/91 - 3.5.1 is corrected by substitution of the name of the representative "Schäfer, Wolfgang, Dipl.-Ing." instead of "Herzog, Friedrich Joachim, Dipl.-Ing.", page 14 is corrected by substitution of the paragraph

"Description:
pages 1, 2, 6 to 9 and 11 filed on 11 November 1993,
pages 3 to 5, 10 and 12 filed on 19 March 1994."

instead of

"Description:
pages 1, 2, 6 to 9 and 11 filed on 19 March 1994,
pages 3 to 5, 10 and 12 filed on 11 November 1993."

and on page 13, line 15 the word "divided" should read "directed".

The Registrar: The Chairman:

M. Kiehl P. K. J. van den Berg

BESCHWERDEKAMMERN DES EUROPÄISCHEN PATENTAMTS

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D E C I S I O N
of 31 May 1994

Case Number: T 0453/91 - 3.5.1

Application Number: 86117601.4

Publication Number: 0271596

IPC: G06F 15/60

Language of the proceedings: EN

Title of invention:
Method for physical VLSI-chip design

Applicant:
International Business Machines Corporation

Opponent:
-

Headword:
-

Relevant legal norms:
EPC Art. 52(1),(2),(3), 54, 56

Keyword:
"Methods for performing mental acts, as such (no)"
"Programs for computers, as such (no)"
"Invention (yes) - Product and manufacturing processes"
"Novelty (yes)"
"Inventive step (yes)"

Decisions cited:
T 0208/84, T 0175/84

Catchword:
The method claims rejected could be interpreted as merely delivering a "design"; i.e. the result would not necessarily be a "physical entity". In contrast, the method claims now on file are restricted to technical, viz. manufacturing, processes albeit including the designing method.

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Beschwerdekammern | Boards of Appeal | Chambres de recours

Case Number: T 0453/91 - 3.5.1

D E C I S I O N
of the Technical Board of Appeal 3.5.1
of 31 May 1994

Appellant: International Business Machines Corporation
Old Orchard Road
Armonk, N.Y. 10504 (US)

Representative: Herzog, Friedrich Joachim, Dipl.-Ing.
IBM Deutschland GmbH
Schönaicher Strasse 220
D-7030 Böblingen (DE)

Decision under appeal: **Decision of the Examining Division of the European Patent Office dated 17 December 1990 refusing European patent application No. 86117601.4 pursuant to Article 97(1) EPC.**

Composition of the Board:

Chairman: P. K. J. van den Berg
Members: W. B. Oettinger
F. Benussi

Summary of Facts and Submissions

I. The appeal contests the decision of the Examining Division to refuse the European patent application No. 86 117 601.4 filed on 17 December 1986 (publication number 0 271 596) for the reason that:

- Claim 1 of the Applicant's main request, filed on 4 October 1990, directed to a "method for carrying out a design ...", would relate to methods for performing mental acts (Art. 52(2)(c) EPC), it being not relevant that a step of the claimed method was specified as being carried out on a computer,

- the independent method Claim 6 as originally filed, directed at a "method for physical chip design", was unallowable for the same reason,

- the independent product Claim 14, filed originally, lacked clarity (Art. 84 EPC) and, possibly (cf. paragraph I.6 of the appealed decision referring to a preceding Communication), even novelty (Art. 54 EPC),

- Claim 1 of the auxiliary request, filed on 4 October 1990, directed at a "method for fixing the positions of electrical elements ... on a semiconductor chip ...", would have to be rejected for the same reason as that of the main request,

- if Claim 1 of the auxiliary request were understood as being intended to claim a method whose steps are all carried out by a computer, this variation would not be supported by the application as filed.

II. As to the independent Claim 14 of the auxiliary request, directed to a semiconductor chip, the Examining Division considered that this claim would have allowed the examination procedure to continue but that it must be rejected as part of the Applicant's unallowable auxiliary request.

In the preceding Communication, the Examiner had also stated that the subject-matter claimed, if it were not excluded from patentability by Article 52(2) EPC, would probably be novel (Art. 54) and inventive (Art. 56).

III. The decision, which was announced during the oral proceedings, was issued with a full reasoning on 17 December 1990.

The appeal was lodged, and the respective fee paid, on 31 January 1991 with a request that the appealed decision be set aside and a patent granted.

On 13 April 1991, the Appellant filed a Statement of Grounds arguing that the subject-matter claimed is not excluded from patenting.

IV. On 23 November 1992, in oral proceedings held following an auxiliary request, the Board decided to continue the procedure in writing on the basis of method claims for the physical design of a (semiconductor) chip filed as Auxiliary Request VI and a product claim for a semiconductor chip filed as Auxiliary Request X on 28 October 1992.

V. In response to Communications from the Board expressing remaining doubts about the patentability of the method claims, the Appellant filed on 19 March 1994 new Claims 1 to 4 and new pages 3 to 5, 10 and 12 for the description, requesting by implication that the grant of

a patent be based on these documents together with Claims 5 to 7 and the other pages of the description as filed on 11 November 1993 and with the original drawings.

The independent claims read as follows:

"1. A semiconductor chip having a chip area which is divided into partitions each partition being a functional block having a number of electrical elements, e.g. gates, pins, connections, etc., wherein

(a) said partitions are intimately attached to each other at their respective adjacent edges leaving no space in between;

(b) said partitions contain interconnect-contact points at their boundaries/edges that connect crossing interconnection lines from edge to edge with matching interconnect-points at the adjacent partition and emerging and ending interconnection lines in matching fashion as well as said electrical elements, said crossing interconnection lines being not connected with one of said elements within said respective crossed partition, and

(c) said partitions are of different porosity, i.e. one partition might be packed more densely than the other."

"3. A method of manufacturing a semicondutor chip according to claim 1 or 2, comprising

(a) designing the chip, including the steps of

logically dividing into partitions the circuits to be placed on said chip,

determining space requirements of said partitions and placing said partitions onto different areas of said chip,

determining logic as well as crossing, ending and emerging connection lines within a given partition by treating connection lines within said given partition in the same way as circuits therein, and repeating this step sequentially for adjacent partitions until all partitions have been processed, at least some of said processed partitions having circuit densities that differ from others of said processed partitions,

shaping the processed partitions into various shapes so that they fit to each other without leaving space in between the neighboring edges of adjacent partitions,

determining interconnect contact points at the boundaries of said partitions by starting in one specific area of the chip and propagating step-by-step in a given direction to form exit information and contact areas of one of said partitions as the input information or placement respectively for the successive adjacent partition or partitions respectively, and

abutting on said chip the appropriately shaped partitions so that each of said partitions is positioned seamlessly to another of said partitions;

and

(b) materially producing the chip so designed.

4. A method of manufacturing a semiconductor chip according to claim 1 or 2 comprising

(a) designing the chip, including the steps of

logically dividing in several partitions all circuits to be contained on the chip,

establishing a floor plan that reflects space requirements as well as locations of said partitions,

said partitions being completely processed independently and in parallel by treating the interconnection lines that cross, emerge or end in a given partition the same as the internal circuits,

physically defining said partitions so that at least one of said partitions have a shape that is different from that of the other of said partitions, such that on the spatial area of the chip said partitions fit together at adjacent edges without leaving space in between, and such that associated inter-connect-points match each other,

determining interconnect contact points at the boundaries of said partitions by starting in one specific area of said chip and propagating step-by-step in a given direction to form exit information and contact areas of one of said partitions as the input information or placement respectively for the successive adjacent partition or partitions respectively, and

adjusting and varying the density or porosity respectively of partitions or regions;

and

(b) materially producing the chip so designed."

VI. In support of his request for grant, the Appellant submitted, in essence, that

- the chip as defined in Claim 1 is new and would not be rendered obvious by the IBM Technical Disclosure Bulletin, Vol. 7 No. 8 (January 1985), p. 4648-4651, cited in the description (second paragraph) and subsequently referred to as "D", because from that prior art at the most feature (a) could be derived, and

- the methods defined in Claims 3 and 4 would clearly be of a technical nature and not merely mental acts or computer programs, because they had to do with working on a physical entity given by an electronic representation of the image of the layout of a real object to be manufactured.

Reasons for the Decision

1. The appeal (cf. point III) is admissible.

2. *Amendments*

2.1 Claim 1 is based on the original Claim 14.

2.2 Dependent Claim 2 is based on the original Claim 15.

2.3 Claim 3, although referring back to (product) Claim 1, is an independent claim insofar as it is of a different category (method).

The method claimed is a method of manufacturing a product (viz. the product claimed in Claim 1). In this respect, Claim 3 is based on, for instance, the reference to "production" in the original description (e.g. on page 6 line 12 and page 10 line 7).

That method comprises a partial method of designing the said product, namely the semiconductor chip claimed in Claim 1. As to this partial method, and the steps it includes, Claim 3 is based, in essence, although with different words, on the original Claims 1 to 5. More particularly, all of the steps of the said partial method in Claim 3 can either directly be refound or are implicit in features (a) to (h) of the original Claim 1 or in the features added by, for instance, Claims 2, 3 and 5.

The concluding step of the said manufacturing method is, again, based on the afore-mentioned reference in the description.

2.4 Similarly, Claim 4 is based,

- as to its category and the last step of the manufacturing method, on the description, and

- as to the partial method of designing the product (chip) and the steps it includes as defined, on the original Claim 6 and its dependent claims, particularly Claims 9 and 11.

2.5 Dependent Claims 5 to 7 are based on the original Claims 10, 12 and 13, respectively.

2.6 The amendments made to the description are, in essence, limited to corrections and modifications rendering the description allowable under Rule 27(1)(b) and (c) EPC.

They are, therefore, also admissible under Article 123(2) EPC.

3. *Novelty and Inventive Step - Product Claim*

3.1 From the piece of prior art (D) cited as coming nearest to the claimed invention (cf. point VI) a semiconductor chip divided as defined in the introductory passage of Claim 1 is known.

3.2 Feature (a) of Claim 1 is not expressly mentioned in the text of D. However, it is noted that, if the equations (1), for instance $y_{11}+y_{21}=y$, are taken to be exact, this would point to no gaps being provided between the partitions.

Furthermore, Fig. 1 and 2 of D would seem to give the impression, and thus confirm the view based on the equations (1), that the partitions are intimately attached to each other at their respective adjacent edges leaving no space in between, as claimed by way of feature (a).

3.3 Whereas any partition of a prior art chip would have emerging and ending interconnection lines as a matter of course, no crossing interconnection lines not connected with any of the electrical elements are either mentioned in the text or shown in the figures of D.

It could be argued that it follows from the appearance of feature (a) in Fig. 1 and 2 of D, that

- inevitably no interconnection lines can be placed in channels between the edges of adjacent partitions and

- therefore the partitions in the upper left corner and in the lower right corner (having the dimensions $x_{11}.y_{11}$ and $x_{22}.y_{22}$) can, in the absense of a common boundary, or edge, only be connected by interconnection lines drawn **either** through other partitions (such as that having the dimensions $x_{21}.y_{21}$ and/or that having the dimensions $x_{12}.y_{12}$) **or** around the outer edges of the chip.

However, nothing in D would point to a particular selection of one or the other of these two alternatives.

It is, thus, not possible to clearly and unambiguously derive feature (b) of Claim 1 from D. This feature is therefore to be regarded as new.

3.4 According to D, VLSI chips are designed so that they are "dense". Nothing in D would, however, point to the possibility of partitions being of different density, or porosity.

Thus, evidently, feature (c) cannot be derived from D.

3.5 Thus, the subject-matter of Claim 1, as a whole, is clearly novel.

3.6 As already said above (3.3), nothing in D would point to the selection of one or the other of the two alternatives mentioned.

From general considerations based on the skilled person's general knowledge, he would also not be led to consider choosing specifically the **former** one of these two alternatives and not the **latter** one. On the contrary: Given that hitherto such interconnection lines used to be placed in channels between partitions, the skilled person would, if no such intermediate channels exist, be led to look for, and use, channels around the outer edges of the chip.

In D, keeping at a minimum the interconnecting wire lengths between partition centers and bounding I/O's is mentioned as desirable. However, in the absence of any proposal in the prior art to draw an interconnection line through partitions none of whose electrical elements are to be connected to it, the skilled person would not consider attempting to solve the problem of minimizing wire lengths by such a deviation from the prior art.

Feature (b) does not, therefore, appear to be obvious from the prior art.

3.7 As already said (3.4), nothing in D would point to partitions being given different porosity.

In effect this means that feature (c) is not only new but also unobvious.

3.8 Therefore, even in the "worst" case, namely if feature (a) were regarded as being known from D, the subject-matter of Claim 1 is to be considered, in agreement with the Examining Division's apparent view (cf. point II), to involve an inventive step.

4. *Novelty and Inventive Step - Method Claims*

A process of manufacturing the product claimed in Claim 1 in a particular way so that it has the technical features defined in Claim 1, inevitably results in that particular product and not in one which does not have these features but differing ones. This is particularly so if the manufacturing process comprises a partial method of designing the said product, by respective steps, in such a particular way that it has the said technical features.

This being true in the present case for Claims 3 and 4, it follows already from the novelty and inventiveness of the subject-matter of Claim 1, based on the novelty and non-obviousness of at least some of its features, that the subject-matter of Claims 3 and 4, concerned with particular ways of achieving these features, is also novel and inventive.

5. *Non-Exclusion from Patentability - Method Claims*

5.1 Therefore, the only issue remaining to be decided in respect of these claims is, following the reasons given for the rejection of the design method claims in the decision under appeal, whether the subject-matter of Claims 3 and 4 is an invention within the meaning of Article 52(1) EPC or not (Art. 52(2) in conjunction with (3) EPC).

5.2 In the particular circumstances of the present case, it appears appropriate first to refer, for contrasting Claims 3 and 4 with the version of the method claims underlying the decision under appeal, to that earlier version, even though it has not been maintained.

As far as the kind of method is concerned for which protection was sought, the methods then claimed could be interpreted as delivering a mere "design" in form of an image of something which does not exist in the real world and which may or may not become a real object; i.e. the result of the claimed method would not necessarily be a "physical entity".

In the earlier decision T 208/84 (OJ EPO 1987, 14), it was held that a "physical entity may be a material object but equally an image stored as an electric signal" (cf. Reason 5). In this finding, the fact that the Board equated an "image" with a "material object" was apparently based on the assumption that the said "image" was that of a "material object". For, "in contrast", the Board in the earlier case held (cf. Reason 7) that "a method for digitally filtering (or, more generally: processing) image data (would) remain an abstract notion not distinguished from a mathematical (or, more generally: non-technical) method so long as it is not specified what physical entity is represented by the data and forms the subject of a technical process" (generalizations added). The "methods for design", as formerly claimed in the present case, would seem to fall under this latter case of an "abstract notion" and not under the former of a "physical entity".

Moreover, referring to the individual steps of designing, these would not seem to make a contribution to the art outside the fields of excluded matters, such as performing mental acts and implementing the resulting steps by programs for computers (Art. 52(2)(c) EPC).

Therefore, in accordance with the case law, the Board would agree with the rejection of the method claims in their earlier versions for the reason that they seemed

not to relate to a technical process making a contribution to the art in a field not excluded from patentability.

5.3 However, contrary to those earlier versions, Claims 3 and 4 now on file are clearly restricted to a method (process) of manufacturing a real (physical) object having technical features and thus to a technical process.

With particular reference to features (a) and (b) of Claims 3 and 4, the manufacturing processes now claimed no longer comprise only the "designing" method, marked (a), as did the said earlier versions of the method claims, but also, although in most general terms, the "producing" steps proper, marked (b), since in principle, it should be assumed that a claim is directed solely to the combination of **all** its features (following decision T 175/84, OJ EPO 3/1989, 71).

No objection under Article 52(2), if applied in conjunction with 52(3), EPC arises therefore in respect of these claims.

6. *Conclusions*

6.1 The independent product Claim 1 and method Claims 3 and 4 are therefore (points 3, 4 and 5, respectively) allowable.

6.2 No objection arises in respect of the dependent product and method Claims 2 and 5 to 7, respectively.

6.3 The same applies to the description and to the drawings.

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the first instance with the order to base the grant of a patent on the following documents:

Description:
Pages 1, 2, 6 to 9 and 11 filed on 19 March 1994,
pages 3 to 5, 10 and 12 filed on 11 November 1993.

Claims:
No. 1 to 4 filed on 19 March 1994,
No. 5 to 7 filed on 11 November 1993.

Drawing:
Sheets/Figs. 1 to 4 as published.

The Registrar: The Chairman:

M. Kiehl P. K. J. van den Berg