BESCHWERDEKAMMERN DES EUROPÄISCHEN PATENTAMTS

BOARDS OF APPEAL OF THE EUROPEAN PATENT OFFICE

CHAMBRES DE RECOURS DE L'OFFICE EUROPEEN DES BREVETS

A		B		C	X

File Number: T 9/91 - 3.4.1

Application No.: 82 304 312.0

Publication No.: 0 073 130

Title of invention: Method for manufacturing a mask type Read Only Memory

Classification: H01L 21/82

D E C I S I O N
of 14 July 1992

Proprietor of the patent: KABUSHIKI KAISHA TOSHIBA

Opponent: Deutsche ITT Industries GmbH, Freiburg

Headword: Programming Read Only Memory/TOSHIBA

EPC Article 56

Keyword: "Inventive step - yes"

Europäisches Patentamt | European Patent Office | Office européen des brevets

Beschwerdekammern | Boards of Appeal | Chambres de recours

Case Number : T 9/91 - 3.4.1

D E C I S I O N
of the Technical Board of Appeal 3.4.1
of 14 July 1992

Appellant : (Proprietor of the patent)
KABUSHIKI KAISHA TOSHIBA
72, Horikawa-cho
Saiwai-ku
Kawasaki-shi
Kanagawa-ken 210 (JP)

Representative :
Kirk, Geoffrey Thomas
BATCHELLOR, KIRK & CO.
2 Pear Tree Court
Farringdon Road
London EC1R 0DS (GB)

Respondent : (Opponent)
Deutsche ITT Industries GmbH,
-Patentabteilung-
Hans-Bunte-Strasse 19
Postfach 840
W - 7800 Freiburg i.Br. (DE)

Representative :
Reichel, Hermann
(authorised employee)
Deutsche ITT Industries GmbH

Decision under appeal :
Decision of the Opposition Division of the European Patent Office dated 6 November 1990 revoking European patent No. 0 073 130 pursuant to Article 102(1) EPC.

Composition of the Board :

Chairman : G.D. Paterson
Members : R.K. Shukla
H.J. Reich

Summary of Facts and Submissions

I. European patent No. 0 073 130 was revoked in a decision of the Opposition Division on the ground that the invention as claimed in Claim 1 lacked an inventive step having regard to the following prior art documents cited by the Opponent (Respondent):

D1 - US-A-4 080 718
D2 - GB-A-2 017 406 and
D4 - US-A-4 235 010.

Document D3 - I. Ruge, "Halbleiter-Technologie", Springer-Verlag, 1975, pages 298 to 299, was also cited by the Respondent during the opposition proceedings.

II. The Patentee lodged an appeal against the above decision and filed a new Claim 1 with the Statement of Grounds of Appeal on 5 March 1991. He requested that the decision under appeal be set aside and that the patent be maintained on the basis of the following documents:

Description : Pages 2 to 4 of the published patent in suit;

Claims : Claim 1 filed on 5 March 1991 and Claims 2 to 4 of the granted patent;

Drawings : Sheets 1 to 7 of the granted patent;

As an auxiliary request, oral proceedings were requested by the Appellant.

III. Claim 1 under consideration reads as follows:

"A method of manufacturing a mask type Read Only Memory comprising the steps of:

I forming a plurality of MOS transistors connected in series in a semiconductor substrate of a first conductivity type by

(a) selectively forming a first insulating layer having a thick portion (65) and a thin portion (67) for a field region and a gate insulating layer, respectively, on the semiconductor substrate,

(b) forming a polysilicon layer (68) on said insulating layer,

(c) forming gate electrodes (69, 70) for the MOS transistors by partially removing said polysilicon layer,

(d) using the gate electrodes as a mask forming regions (74, 76) of a second conductivity type in the substrate to be source and drain regions of the MOS transistors, said second conductivity type regions of adjacent transistors being connected so that the MOS transistors are connected in series, and

(e) forming a second insulating film (78) on the surface of the substrate in which the MOS transistors are formed;

II (a) forming a contact hole (79) in the second insulating film to expose the second conductivity type region of some of the MOS transistors,

(b) forming an aluminium contact electrode on the insulating film away from the transistors and which makes contact with the region of second conductivity type through said contact holes,

(c) forming bonding pads (81);

III (a) selectively removing at least part of the second insulating film (78) to expose the gate electrode, source and drain regions of certain of the MOS transistors,

(b) connecting the source and drain regions of each of said exposed MOS transistors by means of a channel

region (83) by ion implantation of an impurity of the second conductivity type; and

IV forming a protective film (84) on said bonding pads, outer electrode (80) and the MOS transistors, removing the protective film (84) from the bonding pads and providing an outer lead (86) to each of the bonding pads."

IV. Following a communication on behalf of the Board pursuant to Article 11(2) RPBA, oral proceedings were held in the presence of both parties on 14 July 1992.

V. The Appellant presented essentially the following arguments in support of his request:

An important difference between the method according to the present invention and the method disclosed in document D1 is that in document D1 metal contacts are formed to contact the source and gate regions after channel regions had been formed in selected transistors by ion implantation. Thus, the substrate has to be subjected to additional processing steps after the ion implantation step. In the method according to the invention, on the other hand, the metal contacts are formed before the implantation process, so that the number of manufacturing steps required after programming the ROM device are reduced and, consequently, the time delay in supplying the ROM device according to customer's specifications is also reduced. In the bulk manufacture of memory devices, such a saving of number of process steps makes a great difference in the production costs. Moreover, in the present invention, the location of the metal contact away from the MOS transistors enables the selected transistor to be ion implanted later in the manufacturing process than is the case in document D1.

The method as claimed is also distinguished over the method disclosed in document D2 in that in the former method a second insulating layer (78) entirely covers the MOS transistors and thereby provides the necessary protection against environment when the ROM devices are awaiting to be programmed according to customer's requirements. In document D2, on the other hand, in so far as its disclosure is clear, a composite second insulating layer (37,38) is completely removed from the entire memory array area, so that there is no protective layer as in the claimed invention at this stage of the process. Also, whereas in the invention the second insulating layer is patterned and used as a mask for programming, in the method of document D2 either a final protective oxide or a photoresist is used to this end, so that additional manufacturing steps are required as compared with the method according to the invention.

Although documents D3 and D4 disclose self-alignment of the gate electrode to the source and drain regions, the teaching of these documents is incompatible with that of document D2 so that it was not obvious to incorporate the teaching of either of the documents D3 and D4 in the method described in D2. The self-alignment of the gate electrode not only reduces the number of process steps but also improves the integration density of the memory cells.

VI. The arguments of the Respondent can be summarised as follows:

The method disclosed in document D2 deals with the same problem as the present invention, that is, programming of a ROM device at a late stage in the manufacturing process. Also, in the known method a protective layer is provided on the memory device after it has been programmed as in

the method of the invention. Admittedly, in the method according to document D2 the gate electrode is not self-aligned to the source and drain regions. However, as can be seen from document D3, this is a well-known technique forming part of any standard text book on semiconductor device technology. With regard to the use of a second insulating film as a mask during programming by ion-implantation, as against the use of a final passivation film as disclosed in document D2 for this purpose, this modification does not go beyond the normal activities of a person skilled in the art, so that the claimed subject-matter lacks the necessary inventive step.

VII. At the conclusion of the oral proceedings the decision was announced that the appeal is allowed.

Reasons for the Decision

1. Allowability of the Amendments

Although the features in new Claim 1 have been rearranged, the claim differs in substance from the published version only in that (i) a contact hole is formed to expose the second conductivity type region of some of the transistors (cf. feature II(a) of the claim) and (ii) an aluminium contact electrode is formed on the insulating film away from the transistors (cf. feature II(b) of the claim).

New feature (i) is disclosed on page 7,lines 12 and 13 of the application documents as originally filed. Similarly it is evident from the original disclosure on page 7, lines 13 to 16 in combination with Figure 5B that an aluminium contact electrode (80) is formed away from the transistors in the sense that it does not overlie the gate regions of the transistors.

The amendments therefore meet the requirements of Article 123(2) EPC.

2. Inventive step

The only issue which remains to be considered in the present appeal is, therefore, the question of inventive step.

2.1 The patent in suit concerns a method of manufacturing a mask type Read Only Memory (ROM) comprising series connected MOS transistors, which is programmed according to customer's specifications at a late stage of device fabrication, so that the delay in supplying the programmed ROM to the customer is reduced. In the method, after the formation of a field insulating layer (65) and a gate insulating layer (67), a gate electrode (69,70), and source and drain regions of MOS transistors are formed using the gate electrode as a mask so that it is self-aligned to the source and drain regions and the source regions of the adjacent transistors are interconnected (cf. features I(a) to I(d)). Subsequently, a second insulating film (78) is formed on the surface of the substrate in which the transistors are formed, a contact opening (79) exposing the source or drain region is provided in the second insulating film and a contact electrode (80) contacting the source or drain region through the opening and a bonding pad (81) are provided. The contact electrode is provided on the second insulating film away from the transistors in the sense that it does not overlie the gate regions of the transistors (cf. features I(e), II(a) to II(c)). At this stage of the device fabrication, therefore, the transistors are covered by the second insulating film, and the memory device is ready for programming according to customer's

specifications. For programming, the second insulating film is selectively removed to expose the gate electrode and source and drain regions of some of the selected transistors and ions having the same conductivity type as the source and drain regions are implanted so that the source and drain regions of the exposed transistors are interconnected by the channel regions (cf. features III(a) and III(b)). A final protective film (84) is then provided on the bonding pads (81), contact electrode (80) and the transistors, and the bonding pads are subsequently exposed and outer leads (86) are provided on the bonding pads (cf. feature IV).

2.2 In the Board's view, the prior art coming closest to the invention is disclosed in document D2 which, as correctly pointed out by the Respondent, is concerned with the manufacture of a ROM device wherein programming is carried out at a late stage of the device fabrication whereby delay in supplying the ROM device programmed according to customer's specifications is reduced. It is evident from Figure 2 that MOS transistors of this known device are connected in parallel.

In one embodiment described with reference to Figures 4a to 4f (see page 3, line 93 to page 6, line 9), after the formation of field oxide regions (24), openings in an oxide layer (31) defining source and drain regions of ROM array transistors are formed. Subsequently, the source and drain regions (16,17) are formed using the field oxide regions and a nitride layer (32) as a mask, a gate oxide (19) is formed and a polysilicon layer (35) is deposited over the entire substrate. As is evident from Figure 1, the source regions of the adjacent transistors are interconnected. The polysilicon layer is then patterned to form inter alia gate electrodes (11). The gate electrode is thus not self-aligned to source and drain regions as in

the method according to the invention. A composite insulating film, which can be regarded as the second insulating film (78) employed in the method according to the invention, consisting of a nitride film (37) and an overlying multilevel oxide (38) is deposited over the entire substrate and is then removed so that **the entire ROM array area**, a metal-to-polysilicon contact area (39), and a metal-to-source contact area (41) are exposed. Metal contacts in the contact areas (39,41), interconnections and bonding pads are then formed. At this stage in the process when the ROM devices are waiting customer's specifications for programming, the gate electrodes (11) in the ROM array are not covered by the composite film (37,38) (see the right-hand side of Figure 4f) and are exposed to the environment.

For programming according to customer's specifications, a protective oxide layer (21) covering the entire substrate is deposited and then patterned so that an aperture (22) is formed in the protective oxide layer (21) over each of the transistors to be programmed. Ions **having the same conductivity type as the substrate** are then implanted through the apertures in the channel area so as to raise the threshold voltage of the selected transistors. Although in connection with the programming step, a reference is made to Figure 4g in the description, there is no Figure 4g in the document.

In the above method of programming using the protective oxide layer (21) as the implant mask, the transistors which are programmed are left without a covering of the protective oxide layer, and it is recognised in the document that this might have detrimental effects on the transistors. As an alternative, therefore, a photoresist is used as the ion-implant mask, and after the

programming, the protective oxide layer (21) is deposited and patterned to expose only the bonding pads.

It is stated at page 5, lines 115 to 119 of document D2 that to provide additional protection, instead of removing the multilevel oxide coating (38) from the entire cell array area as shown in Figure 4f, it may be removed only over the gates of the transistor (10). There is no disclosure as to whether or not the underlying nitride layer is left over the gates of the transistors. The Board agrees with the Appellant that it is not clear from this passage whether the multilevel oxide is removed over the gates of all the transistors or only over the transistors to be programmed. In the Board's view, no matter how the above disclosure is interpreted, during programming a protective oxide or a photoresist is always required as a mask for ion-implantation.

2.3 In summary, therefore, the claimed method differs from the closest prior art in that

(i) the MOS transistors formed are connected in series;

(ii) the second conductivity type regions, that is, the source and drain regions (74,76) are formed using the gate electrodes as a mask so that the latter are self-aligned to the former;

(iii) at the device fabrication stage after the formation of metal contacts to the second conductivity type regions, interconnections and bonding pads, the second insulating film is left on the surface of the substrate in which the transistors are formed;

(iv) the second insulating film is selectively removed to expose the gate electrode, source and drain regions of the transistors to be programmed, and

(v) subsequently, the second insulating film is used as a mask during ion-implantation of an impurity in the channel regions of the exposed transistors,

(vi) the impurity being of the second conductivity type so that the source and drain regions are interconnected.

In this connection, it is to be noted that features (iv) to (vi), and also feature (iii) in so far as it influences subsequent programming steps, are concerned with the programming of the ROM device at a late stage in the manufacturing process, whereby the number of process steps required to complete the fabrication of the device after programming, and consequently the time in supplying the finished device, is reduced. Moreover, since at the end of the device fabrication when the device is awaiting to be programmed, the second insulating film according to feature (iii) covers the MOS transistors, whereby these are protected from detrimental effects of the environment.

Features (i) and (ii), on the other hand, are not at all concerned with programming, but relate respectively to the type of ROM device and formation of source and drain regions of the MOS transistors in a manner whereby not only is the gate electrode accurately aligned to the source and drain regions but additional masking and etching steps required in the prior art method of document D2 (for defining the source and drain regions) are avoided. These features, therefore, do not contribute to the solution of the problem of reducing the number of

process steps after programming, and are therefore to be considered separately from the distinguishing features (iii) to (vi) in the assessment of inventive step.

2.4 As regards the distinguishing feature (ii), the Board agrees with the Respondent that this is a well-established technique in the art and is normally employed with a view to self-aligning the gate electrode with the source and drain regions (cf. document D3, Figure 10.1 and the accompanying text). Moreover, in document D4 this technique is employed in the manufacture of a ROM having MOS transistors which are connected in series between a supply voltage VDD and the ground (cf. column 5, line 49 to column 6,line 25; column 3, lines 32 to 41; Figures 3, 5 and 6a to 6f). The Board is therefore of the view that the incorporation of the features (i) and (ii) in the method according to document D2 would have been regarded as obvious by a skilled person.

2.5 Document D1 relates in general to a method of fabricating a ROM device in which data programming is carried out at or near the last stage of fabrication. According to the method described with reference to Figures 1(a) to 1(g) in column 3, line 58 to column 5, line 66, before the last stage of programming, a metallisation pattern (30) remains over all rows of the ROM matrix defined by the field effect transistors that have been formed, and thus over all portions of the gate regions and a passivation film (32) covered by a photoresist is provided over the surface of the wafer. For programming the device by ion-implantation, the passivation film (32) as well as the underlying metallisation (30) need to be selectively removed to expose the desired gate locations. In a photolithographic operation subsequent to the ion-implantation, the passivation layer is again selectively

etched to define the areas for pad locations. Thus, contrary to the invention, in the above method the final passivation film, corresponding to the claimed protective film (84), and additionally an underlying metallisation are used as ion-implantation mask during the programming. Moreover, the bonding pads are formed not before but after the ion implantation. Thus the features (iii) to (v) are not suggested by the above embodiment.

In the method described with reference to Figures 4 and 5 (see, column 7, line 30 to column 8, line 3), contact openings (100) for source, drain and gate are formed in a phosphosilicate glass layer corresponding to the second insulating layer of the claimed invention, and simultaneously openings (102) over selected gate regions are formed for programming by ion implantation. The ion-implantation is followed by deposition of metal contacts in the openings (100) for the source and gate. Similarly, in the method described with reference to Figures 6 and 7 in document D1 (see column 8, lines 4 to 36), contact openings (108,110) for source, drain and gate electrode and openings over selected gate regions for programming are formed simultaneously in a phosphosilicate glass layer (98). After ion-implantation for programming, metallisation patterns (118,122,120) contacting the source, drain and gate are formed. In the method according to the embodiment illustrated in Figures 10 and 11 in document D1, contact openings for pad locations and openings over selected gate regions for programming are formed simultaneously. Thus, in the above embodiments openings for programming on the one hand and for metal contacts or bonding pads on the other are formed in the same photolithographic operation. As a result, in the above embodiments, contrary to the features (iii) to (v) of the invention, the metal contacts or bonding pads are formed always after the step of programming a selected

transistor by ion-implantation, so that features (iii) to (v) cannot be regarded as obvious in the light of these embodiments.

2.6 In the contested decision, it was held that starting with the method as claimed in document D1, it was a matter of routine design procedure to introduce a separate photolithographic step for programming and thereby accept the drawback of having an additional fabrication step. The Board, however, cannot follow this line of argumentation, firstly because it entails going against the teaching of document D1 and secondly, the problem underlying the invention, as implied in the above line of argumentation, also includes part of its solution, namely, providing a photolithographic step for programming which is in addition to that for forming contact openings, indicating a hindsight analysis which is not permissible in the assessment of inventive step.

2.7 For the foregoing reasons, in the Board's judgment, the subject-matter of Claim 1 as amended is not rendered obvious by the cited prior art within the meaning of Article 56 EPC. Claim 1 is, therefore, allowable under Article 52(1) EPC. Dependent Claims 2 to 4 relate to particular embodiments of the method according to Claim 1 and are, therefore, likewise allowable.

Order

For these reasons, it is decided that:

1. The appeal is allowed.

2. The case is remitted to the first instance with the order to maintain the patent in amended form on the basis of

Claim 1 as filed on 5 March 1991, together with Claims 2 to 4 as granted.

The Registrar: The Chairman:

M. Beer G.D. Paterson