BESCHWERDEKAMMERN DES EUROPÄISCHEN PATENTAMTS

BOARDS OF APPEAL OF THE EUROPEAN PATENT OFFICE

CHAMBRES DE RECOURS DE L'OFFICE EUROPEEN DES BREVETS

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File Number: T 693/90 - 3.4.1

Application No.: 83 303 768.2

Publication No.: 0 103 362

Title of invention: Semiconductor device with power lines

Classification: H01L 23/52

D E C I S I O N
of 11 August 1992

Proprietor of the patent: FUJITSU LIMITED

Opponent: Deutsche ITT Industries GmbH, Freiburg

Headword:

EPC Articles 56, 110

Keyword: "Inventive step of main request (no); a first document disclosing how to solve the objective problem, renders it obvious to use a particular means of a second document in a device of a third document.
Late filed and not clearly allowable auxiliary request not admissible."

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Beschwerdekammern | Boards of Appeal | Chambres de recours

Case Number : T 693/90 - 3.4.1

D E C I S I O N
of the Technical Board of Appeal 3.4.1
of 11 August 1992

Appellant : (Opponent)
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Decision under appeal :
Decision of Opposition Division of the European Patent Office dated 4 July 1990 rejecting the opposition filed against European patent No. 0 103 362 pursuant to Article 102(2) EPC.

Composition of the Board :

Chairman : G.D. Paterson
Members : H.J. Reich
Y. van Henden

Summary of Facts and Submissions

I. The Respondent is owner of European patent No. 0 103 362.

Claim 1 as granted reads as follows:

"1. A semiconductor device comprising:
a semiconductor substrate (11);
a logic circuit region (21) arranged in the semiconductor substrate, said logic circuit region having a plurality of logic circuits;
a peripheral circuit region (22) arranged around said logic circuit region, said peripheral circuit region including a plurality of output buffer circuits;
a first power line (13, 13') and a second power line (15, 15') distributed at least along the peripheral circuit region, said first power line being connected to each of said output buffer circuits; and
a sub-power line (16, 18) distributed on an insulating layer (14, 17) separating it from said first power line;
in which electric shorts are formed between said first power line and said sub-power line via through holes (33) in said insulating layer (14, 17) at each portion of said first power line under which it is connected to one of said output buffer circuits."

Claims 2 to 8 are dependent on Claim 1.

II. The grant of this patent was opposed by the Appellant on the ground of lack of inventive step, citing three documents, among them:

D1: US-A-3 981 070.

In the course of the proceedings before the Opposition Division the Opponent cited further document EP-B-0 016 577 which was introduced into the proceedings by the Opposition Division. The Board relied on the subject-matter of this document as prior art by citing the corresponding prior published European application:

D4: EP-A-0 016 577.

After having examined all four cited documents on the basis of Article 114(1) EPC, the Opposition Division rejected the opposition. It took in particular the view that it would not be obvious to use the teaching of the most relevant document D4 in the closest prior art as disclosed in document D1 for the following reasons: Document D4 intends to improve the resistance of a signal line which is made of polycrystalline silicon and carries currents of the order of microamps. It would be at least doubtful that it was obvious to apply the teaching of document D4 to a power line which is normally made of metal and carries currents of the order of milliamps. Moreover, the shorts between the known signal and sub-signal line are spaced from and not at the active device corresponding to an output buffer, and the upper of these two lines in fact is part of this active device and partially located in the same plane as the lower one.

III. The Appellant lodged an appeal against the decision of the Opposition Division.

IV. In a communication accompanying a summons to oral proceedings, the Board cited under Article 114(1) EPC European Search Report document:

D5: FR-A-2 426 334,

and notified to the parties its preliminary view that the teaching of document D5, i.e. to achieve the technical objects underlying the patent under appeal by reducing the effective resistance of the power lines, might encourage a skilled person to make an analogous use of the resistance-reducing line plus sub-line system according to document D4 in the device disclosed in document D1, in which use the claimed position of the shorts between the lines might be the result of a logical adaptation measure which can be expected from the skilled person. Also the dependent Claims 2 to 8 appeared not to contain any characteristic of inventive nature.

V. Oral proceedings were held on 11 August 1992, during which the Appellant (Opponent) requested that the decision under appeal be set aside and that the patent be revoked.

The Respondent requested that the appeal be dismissed and that the patent be maintained as granted, or as an auxiliary request put forward at the end of the oral proceedings that the patent be maintained on the basis of the combination of Claims 1, 6 and 7.

VI. In support of his request, the Appellant essentially submitted that:

(a) starting from document D1 as closest prior art, the problem underlying the patent under appeal is to avoid a voltage drop in a power line when increasing the degree of integration;

(b) document D4 discloses means to avoid voltage drops - admittedly in Figures 4 and 6 in a signal line. However, the teaching of Figure 2 of D4 is not limited to any particular use of these lines, so that it would be obvious to apply the line plus sub-line system of D4 to power lines. The resistance reducing

effect of the known line plus sub-line system is independent from any particular material of the conductive lines and leads to no technical difficulties in a use for power lines;

(c) document D5 deals as well with signal lines as with power lines;

(d) the use of the Ohm's Law in the positioning of the shorts is self-evident to the expert. A shrinkage of the multi-layer structure according to document D1 lies in the general trend. Document D1 was published in 1974 and represents a device with a relatively low degree of integration. It is a generally known measure in the art of shrinking to place device elements, which have formerly been arranged side by side, superposed upon another. Hence in shifting the known position of the short in Figure 4 of document D4 to the claimed position "at each portion of said first power line under which it is connected to one of said output buffer circuits" a skilled person would only apply measures which are generally known in the shrinkage of semi-conductor devices.

VII. The above submissions were contested by the Respondent, who argued essentially as follows:

(a) the two-level metallisation device of document D1 has no power lines, i.e. voltage and ground busses, in the peripheral circuit region as claimed in Claim 1. Interpreting the word "under" as beneath or in register and below, Figures 7 to 9 and column 2, lines 6 to 8, of document D4 show - contrary to the subject-matter of Claim 1 - no connections to a peripheral circuit under a power line;

(b) in the prior art the problem of resistance and inductance-caused voltage drops in power lines is solved by voltage tracking (D1, column 11, lines 42 to 58), by a particular ratio of resistance and inductance between voltage- and ground-line (D1, column 11, lines 28 to 36; column 2, lines 47 to 51; and Claim 6), by an increase of the line width (patent under appeal, column 1, lines 53, 54) or by delaying circuit actions and thus lowering the current amplitude (patent under appeal, column 1, line 65 to column 2, line 13). Hence, the known solutions point into other directions than to the use of a line plus sub-line system;

(c) document D5 teaches to solve the problem of coverage and fineness of thick busses by an offset and a different width of two power lines, which are in direct contact with each other;

(d) the line and sub-line system disclosed in document D4 is part of a signal line and does not extend to the power consuming device. Figures 3 and 4 of document D4 demonstrate clearly the local displacement between the short of line and sub-line and the contact area of the transistor which is moreover only connected to one line. Document D4 does not teach to extend the second line to the contact region and to provide the short directly above the power consuming device;

(e) the invention deals with a specific problem in a specific device. In particular, the claimed alignment of the shorts between line and sub-line with portions of the power line under which the latter is connected to an output buffer, is disclosed in no cited document. This alignment is not an automatic result of the use of Ohm's Law but is a non-obvious feature

of the invention which is crucial for its functioning and which allows to balance the extra costs of the additional method step for producing the sub-line.

VIII. At the conclusion of the oral proceedings, the decision was announced that the decision of the Opposition Division was set aside and that the European patent was revoked.

Reasons for the Decision

1. Inventive step - Claim 1 of the main request

1.1 From document D1 there is known in accordance with the wording of Claim 1:

"A semiconductor device comprising: a semiconductor substrate (see D1, 26 in Figure 3L); a logic circuit region (see dashed lines forming squares in Figure 5) arranged in the semiconductor substrate, said logic circuit region having a plurality of logic circuits (Figure 6); a peripheral circuit region arranged around said logic circuit region (surrounding the chess-board like central area in Figure 5), said peripheral circuit region including a plurality of output buffer circuits (T9 in Figure 5, 101 in Figure 7 and Figure 12); a first power line (117 in Figure 9) and a second power line (109 in Figure 9 and 113, 114 in Figure 7) distributed at least along the peripheral circuit region, said first power line being connected to each of said output buffer circuits (see potential V_{CC} at first power line 117 in Figure 9 and V_{CC} at the output buffer circuit in Figure 12)."

Contrary to the Respondent's view in paragraph VII(a), a comparison of the mask in Figure 9 for the uppermost second metallisation layer with the mask in Figure 7 for

the lowermost first metallisation layer results in the fact that the two outer U-shaped frame-like bus parts of the first power line 117 in Figure 9 overlap directly transistors 101 in Figure 7. They also have under themselves electrical connections to these transistors; see the mask for the through holes in Figure 8, the equidistant system of line-shaped through holes neighbouring directly the via holes 124 of ground distribution bus system 117, which each lead to the outer U-shaped electrode of transistors 101 in Figure 7 respectively. The fact that the second power line is as well "distributed at least along the peripheral circuit region" as claimed, follows directly from the contours of outermost line-shaped busses 109 in Figure 9 and 114 in Figure 7.

1.2 Starting from document D1, the objective problem underlying the patent in suit is to make the voltage drop in the power lines of an LSI - (large scale integration) - circuit as small as possible in order to avoid malfunctions in the LSI circuit with high levels of integration and large number of pins; see the patent in suit, column 1, lines 46 to 50, column 2, lines 18 to 21, and column 3, lines 27 to 34.

1.3 This problem is solved by the features distinguishing the subject-matter of Claim 1 from the prior art according to document D1, i.e. by:

"a sub-power line distributed on an insulating layer separating it from said first power line; in which electric shorts are formed between said first power line and said sub-power line via through holes in said insulating layer at each portion of said first power line under which is it connected to one of said output buffer circuits".

The above solution inter alia allows to halve the inherent resistance of the original power line; see the patent in suit, column 2, lines 28 and 29.

1.4 The general principle of the claimed solution of the objective problem, i.e. to avoid malfunctions in an LSI-circuit which are caused by voltage drops in power lines, by reducing the effective resistance of the power lines via an additional sub-power line, is known from document D5; see document D5, page 1, lines 28 to 35, page 5, lines 20 to 31 and additional line 3 in Figures 1 and 2. In the Board's view, a skilled person is able to recognise that the thickness and fineness problem of power lines and its solution according to document D5 - as put forward by the Respondent in paragraph VII(c) above - represents independent technical information which has no functional influence on the teaching to prevent malfunction by resistance reduction. Therefore, despite this separate technical information in document D5, document D5 teaches a skilled person unambiguously to solve the objective problem underlying the patent under appeal by increasing the effective current guiding cross-section of a power line via a supplementary line and thus encourages a skilled person to consult the prior art with regard to known realisations of an electric line plus a supplementary one for the purpose of lowering the effective resistance. Thus, in the Board's view, document D5 reduces the objective problem underlying the patent under appeal to the technical aim of lowering the effective resistance of a power-line, and guides a skilled person to consider the use of the teaching of document D4 in the device disclosed in document D1.

1.5 From document D4, there is known in the subsequent wording of Claim 1:

"a sub- ... line (see D4, 3 in Figure 2; and page 5, lines 19 to 22) distributed on an insulating layer (4 in Figure 2) separating it from said first ... line; in which electric shorts are formed between said first ... line and said sub- ... line via through holes (5, 6) in said insulating layer".

The teaching of Figure 2 of document D4 is not limited to any particular use but is quite generally presented in document D4 as a means to halve the effective line resistance; see D4, page 6, lines 7 to 10. In the Board's view, the fact that document D1 is already equipped with two metallisation planes renders an application of a line- and sub-line-arrangement in different metallisation planes according to document D4 rather appropriate. Moreover, the Board regards a skilled person to be able to foresee that, by separating lines 2 and 3 of Figures 1 and 2 of document D5 into two different metallisation layers with an interposed separating insulation layer, any thickness problems of the power lines can be avoided. Thus, it is obvious to a skilled person not to limit himself to the explicit particular teaching of document D5 but to make use of this evident additional advantage of the interposed insulation layer according to document D4.

Also the embodiments in Figures 4 and 6 of document D4 which are narrowed down to signal lines, would in the Board's view not prevent a skilled person from recognising that - contrary to the Respondent's view in paragraph VII(d) - the teaching of document D4 may without technical difficulties also be used in a power line in order to halve its resistance. A skilled person is supposed to know that the effect of reducing the resistance is based on the creation of a supplementary additional current guiding channel and thus on a volume effect which is independent

from the resistance properties of the line material and, within the first order approximation of Ohm's Law, also independent from any value of the current density.

1.6 It remains to be discussed, whether a skilled person can be expected to shift shorts 27 in Figure 4 (or 36 in Figure 6) of document D4 from their position laterally displaced from contact electrode 23 (or 33 in Figure 6) to portions of power line 117 of Figure 9 of document D1, under which this line is connected to one of transistors 101 (see also paragraph 1.1 above). A skilled person - in the Board's view - recognises that the position of shorts 27 or 33 on top of the thick oxide layers 22 or 32 is a planarisation measure in order to level out layer distortions caused by the relatively thin gate oxides, that it has nothing to do with resistance lowering, and that the short stops the parallel connection of line and sub-line and thus the resistance lowering effect. The Board regards it to be within the normal logical thinking of the skilled person that - in order to make full use of the halving effect of the effective resistance - the shorts should be provided at the beginning and at the end of the power transmission way and should approach the location of the power consumer as much as possible. Thus - contrary to the implicit view of the Respondent in paragraph VII(d) - in the Board's view, the remaining feature in Claim 1:

shorts formed "at each position of said first power line under which it is connected to one of said output buffer circuits"

has the character of a purely logical adaptation measure for making optimal use of the teaching of document D4 in the multi-layer system of document D1 which measure only needs the routine skill of an expert and will be taken

into consideration by him automatically. The fact that the alignment of short and output buffer balances extra costs for the production of sub-line, as the Respondent put forward in paragraph VII(e) above, represents an extra effect (bonus) of an obvious measure which - according to the normal practice of the Boards of Appeal of the EPO - is to be disregarded in the evaluation of an inventive step; see also T 21/81, OJ EPO 1983, 15.

1.7 The technically diverging solutions of the voltage drop problem put forward by the Respondent in paragraph VII(b) above, do not cast any technical doubts on the feasibility and on the reliability of the stated advantageous effects of the teachings disclosed in document D5 and D4 and thus, in the Board's view, do not discourage a skilled person from applying them in the device of document D1.

1.8 For these reasons, the Board considers that the subject-matter of Claim 1 of the main request is the result of a use of the teaching of document D4 in the device of document D1 combined with a logical one-way-street-like adaptation measure, which use is rendered obvious by the fact that document D5 informs a skilled person that the teaching of document D4 solves the objective problem underlying the patent under appeal. Therefore, in the Board's judgment, Claim 1 of the main request lacks an inventive step within the meaning of Article 56 EPC.

2. Claims 2 to 8 of the main request fall because of their dependency on Claim 1.

3. Auxiliary request

At the end of the oral proceedings the Respondent put forward the auxiliary request that the patent be maintained on the basis of the combination of Claims 1, 6 and 7.

It should be noted that according to the jurisprudence of the Boards of Appeal "a Board of Appeal may refuse to consider alternative claims which have been filed at a late stage, e.g. during the oral proceedings, if such claims are not clearly allowable"; see Decision T 153/85, OJ EPO 1988, 1, Headnote II.

This principle applies equally in examination and opposition proceedings (see also e.g. Decision T 95/83, OJ EPO 1985, 75). The necessity for amendments to be proposed in good time before oral proceedings has also been made clear in the "Guidance for Appellants and their Representatives" which has been published regularly in the Official Journal (most recently in OJ EPO 1989, 395).

In the present case, the Board had already informed the Respondent in the communication accompanying the summons for oral proceedings that no characteristic of inventive nature could be seen in the subject-matter of dependent Claims 2 to 8, and had requested the parties to file any further written observations at least one month before the date of the oral proceedings. The Respondent did not follow this invitation. Furthermore when the Respondent put forward his proposal during the oral proceedings, the Appellant stated that he was taken by surprise and was not in a position immediately to deal with such an auxiliary request.

In the Board's judgment, especially having regard to the Board's preliminary views set out in the communication accompanying the summons and referred to above, the auxiliary request is certainly not clearly allowable, and having regard also to the statements of the Appellant, this auxiliary request is not admissible at such a late stage in the appeal proceedings.

Furthermore, the Board would have reached the same conclusion as to the inadmissibility of the request even if the Board's communication accompanying the summons had not requested any further written observations to be filed at least one month before the oral proceedings.

Order

For these reasons, it is decided that:

1. The decision of the Opposition Division is set aside.

2. The European patent is revoked.

The Registrar: The Chairman:

M. Beer G.D. Paterson