BESCHWERDEKAMMERN DES EUROPÄISCHEN PATENTAMTS

BOARDS OF APPEAL OF THE EUROPEAN PATENT OFFICE

CHAMBRES DE RECOURS DE L'OFFICE EUROPEEN DES BREVETS

Publication in the Official Journal ~~Yes~~ / No

File Number: T 673/90 - 3.4.1

Application No.: 84 115 903.1

Publication No.: 0 159 408

Title of invention: Method of manufacturing a semiconductor device comprising resistors

Classification: H01L 21/31

DECISION
of 3 September 1991

Applicant: KABUSHIKI KAISHA TOSHIBA

Headword: Semiconductor/TOSHIBA

EPC Article 56

Keyword: "Inventive step (no)"-
"Analogous use without generally valid prejudice, representing a disregardable bonus effect"

Headnote

Case Number : T 673/90 - 3.4.1

DECISION
of the Technical Board of Appeal 3.4.1
of 3 September 1991

Appellant : KABUSHIKI KAISHA TOSHIBA
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Decision under appeal : Decision of Examining Division 048 of the European Patent Office dated 5 April 1990 refusing European patent application No. 84 115 903.1 pursuant to Article 97(1) EPC.

Composition of the Board :

Chairman : G.D. Paterson
Members : H.J. Reich
Y. van Henden

Summary of Facts and Submissions

I. European patent application No. 84 115 903.1 (publication No. 0 159 408) was refused by a decision of the Examining Division in respect of Claim 1 which was filed during oral proceedings held on 21 February 1990. A reasoned decision in writing was issued on 5 April 1990.

II. The reason given for the refusal was that Claim 1 was not allowable under Articles 52(1) and 54 EPC for lack of novelty with regard to the method known from document:

D2 : "NEC Research and Development", No. 56, January 1980, pages 170-174.

III. The Appellant lodged an appeal against this decision, and filed new main and auxiliary requests having main claims which both additionally comprised a series of measures disclosed in the original description, in particular the local definition in the first film of the low resistance portions self-aligned with the high resistance element by doping as disclosed in the description of the present application, Figure 2B and page 4, lines 24 to 35.

IV. In a communication preparing oral proceedings, the Board drew the Appellant's attention to the fact that a method wherein such a definition of a high resistance element by doping is used was known from document:

D4 : EP-A-0 078 190,

cited in the European Search Report. Furthermore, the Board informed the Appellant of its provisional view, that it might be regarded as obvious to replace the direct deposition of a metal silicide layer upon said low resistance portions in the method of document D4 by a

deposition of a metal layer and a subsequent siliciding step such as known from document D2, in particular page 171, lines 28 to 32, and to arrive thus at the subject-matter of the main claims of both said requests.

V. In response to this communication and as a basis for his intended request during oral proceedings, the Appellant filed on 20 August 1991 one new set of claims, wherein Claim 1 corresponds to that of his former auxiliary request, amending the words "wiring portion" into "laminated film structure resistor" as disclosed in the original description, page 5, lines 20-24.

VI. Oral proceedings were held before the Board at the end of which the Appellant requested that the decision under appeal be set aside and a patent be granted on the basis of Claims 1 to 15 as filed on 20 August 1991.

Claim 1 reads as follows:

"1. A method of manufacturing a semiconductor device comprising the steps of:

forming a first film (13) of high resistance and containing silicon on a semiconductor substrate (11);

forming a single mask (14) of a predetermined pattern on said first film (13), the mask (14) covering a predetermined region of said first film defining the location of a high resistance element; doping an impurity ion into those regions of said first film not covered by said single mask (14) to define the position of low resistance portions (15_1, 15_2) self-aligned with said high resistance element;

forming a second film (17) of metal on said regions of said first film not covered by said single mask (14) and said single mask (14);

siliciding those regions of said second film in contact with said low resistance portions so that metal-silicide regions are formed, said low resistance portions (15_1, 15_2) of said first film and said metal-silicide regions forming a laminated film structure resistor of low resistance, while the region (16) of said first film covered by said single mask (14) forms said high resistance element, and removing said second film (17) left on said single mask (14), and said laminated film structure resistor of low resistance is self-aligned with said high resistance region."

Claims 2 to 15 are dependent on Claim 1.

VII. In support of his request the Appellant argued essentially as follows:

(a) In the definition step of the high resistance element according to document D4 a single implantation mask consisting of a photoresist is formed above the polysilicon layer and subsequently used as a lift-off mask for depositing directly a metal-silicide layer. Such a photoresist mask would not maintain its shape at the temperatures necessary for alloying a metal and silicon and can therefore not be used in the claimed siliciding step.

(b) It would not be obvious to deposit a second film of metal on the first film (of high resistance and containing silicon) for siliciding purposes directly after the claimed implantation step. During this implantation step a thin layer of natural (native) silicon oxide is formed, which native oxide layer would always have been removed by etching prior to a following metal layer deposition step in all comparable prior art methods according to the

European Search Report, as can be seen in detail from:

(1) Document DE-A-3 204 054 (D5), page 15, para. 2;

(2) Document GB-A-2 102 625 (D1), page 3, lines 25 to 47;

(3) Document US-A-4 297 721 (D3), column 7, line 48 to column 8, line 6;

(4) Document D2, page 171, lines 28 to 32; and

(5) The prior art statement in the present application, page 2, lines 1 to 4.

(c) Native oxide would form a barrier to metal penetration in a siliciding process as can be seen from its use as an alloying-mask in the definition of the resistor according to Figure 2(e) of document D2. Therefore, the siliciding technique of document D2 would not be applicable after the implantation step according to Figure 1A of document D4 due to the formation of native oxide during this step.

(d) The present application teaches that the etching step of the native oxide between implantation and metal layer deposition can be left out, because it was found that alloying breaks through said native oxide. In the present application the metal layer deposition immediately after the implantation step is disclosed in the description, page 5, lines 5 to 8. If an etching step would have been used beforehand, it would have been explicitly stated as on page 4, lines 19 to 22.

Reasons for the Decision

1. The appeal is admissible.

2. Inventive Step

2.1 From document D4 there is known in the wording of Claim 1:

"A method of manufacturing a semiconductor device comprising the steps of:

forming a first film of high resistance and containing silicon (see D4, Figures 1a, 3) and page 3, lines 26 to 31 on a semiconductor substrate;

forming a single mask (5 in Figure 1a) of a predetermined pattern on said first film, the mask covering a predetermined region of said first film defining the location of a high resistance element (7 and page 3, lines 31 to 36);

doping an impurity ion (D4, page 4, lines 1 to 3) into those regions of said first film not covered by said mask to define the position of low resistance portions (6 in Figure 1A) self-aligned with said high resistance element;

forming a second film (8 in Figure 2A) on said regions of said first film not covered by said single mask so that metal silicide regions are formed (page 4, lines 9 to 14);

said low resistance portions (6) of said first film (3) and said metal-silicide regions (8; page 4, line 22) forming a laminated film structure resistor of low resistance, while the region (7) of said first film (3) covered by said single mask (5) forms said high resistance element, and removing (see Figure 3A) said second film (8 in Figure 2A) left on said single mask (5), and said laminated film structure resistor of low resistance is self-aligned with said high resistance region (see Figures 2A and 4B).

The method claimed in Claim 1 is distinguished from the prior art according to document D4 by the following features:

(a) forming a second film "of metal";

(b) "siliciding those regions of said second film in contact with said low resistance portions so that metal-silicide regions are formed."

2.2 In the prior art according to document D4, as in the method of Claim 1, the same single mask is used both for the definition of the high resistance element and for the self-alignment of the metal-silicide regions (overlying doped polysilicon and thus "forming a laminated film structure resistor of low resistance") to the high resistance element.

The disadvantage of misalignment as a result of using two separate masking steps, one for the high resistance element definition and one for its wiring by a metal silicide layer respectively (according to the Appellant's own prior art statement in the description, Figures 1A to 1E) is already avoided in this nearest prior art. Therefore, the object of providing in a simple operation a

semiconductor device of high packaging density - as mentioned in the original description, page 3, paragraph 1 - cannot form part of the objective problem.

Hence, starting from the nearest prior art according to document D4 the objective problem underlying Claim 1 reduces to the technical aim to make use of the known advantages (such as good adhesion) of the known "alloying" technique - i.e. of melting a metal layer upon a polysilicon layer in order to form a metal silicide layer - in the self-aligned wiring step of a high resistance element.

In the Board's view, no contribution to inventive step is to be found in the definition of the above problem.

2.3 Distinguishing features (a) and (b) mentioned above are known for the same technical purpose as in the present application from document D2, in particular Figure 2e and page 171, lines 28 to 32. In order to arrive at the subject-matter of Claim 1 a skilled person only has to replace the metal silicide deposition step in the method of document D4 by the siliciding steps - i.e. metal layer deposition plus subsequent alloying - as known from document D2. The Board holds this replacement to be a use of the known and expected advantageous properties of a known technology in a closely analogous situation, which use is regarded to be obvious to a skilled person.

2.4 The Appellant's arguments according to paragraphs VII(a) and VII(b) above are not relevant to the question whether the subject-matter of Claim 1 involves an inventive step. The subject-matter of Claim 1 does not specify the material for the mask. The open wording "comprising the steps of" in Claim 1 prevents a definition of protection, wherein the "second film of metal" is exclusively formed

directly after the doping step of "low resistance portions" without intervening measures (such as etch-removal of native oxides).

2.5 The Board saw no procedural necessity to invite the Appellant to amend his main claim in accordance with the presented arguments, because such amendments would not have led to an allowable claim for the following reasons:

2.6 A single mask consisting of "silicon oxide" as disclosed in the application, page 4, lines 15 to 20, is already applied in the siliciding technique according to document D2, see page 171, lines 28 to 30.

2.7 Even if the Board would accept that the text of the original description, page 5, lines 1 to 8, is an implicit disclosure of the direct sequence of the method steps doping and metal layer deposition, this measure would not imply an inventive step. The Appellant's evidence summarised in paragraphs VII (b) (1) to (5) did not convince the Board, that there was a prejudice of general validity in the art, that a polysilicon layer which is covered with a layer of natural (native) oxide cannot be alloyed with an overlying metal layer; see also the decision T 19/81, OJ EPO 1982, 51, paragraph 5.3:

2.7.1 The native oxide removal in document D5, page 15, paragraph 2, is not followed by a siliciding step but by a metallisation layer deposition; see 35a, b in Figure 9.

2.7.2 The etching step in document D1, page 3, lines 25 to 47, directly before the Pt-layer deposition only removes Si_3N_4 but not SiO_2; see page 3, line 35.

2.7.3 Document D3, column 7, line 50 mentions nitride as an alternative mask material, so that in this alternative a

direct etching of the Si_3N_4 layer into a siliciding mask directly before the deposition of metal layer 42 would not remove a native oxide on top of polysilicon layer 24. Moreover, in the method of document D3 the metal layer deposition is not followed by an alloying step. But layer 42 is used as metallisation; see Figures 5 and 6.

2.7.4 A skilled person knows that a dopant can also be diffused through a silicon oxide layer and that the effectiveness of such a layer as a mask depends on the thickness of the layer, diffusion time and temperature; see document I. Ruge "Halbleiter-Technologie" Springer-Verlag, Berlin, Heidelberg, New York, 1975, pages 235 to 243 in particular page 235, lines 17 to 21, as expert opinion.

2.7.5 In the Board's view, a skilled person will interpret the etching step mentioned in the present application, page 2, lines 1 to 4, as a consequence of the double application of the planar technology, i.e. as a mask-forming step, native oxides not being mentioned.

2.8 Even if the Board would regard a skilled person unable to expect or not to know, that a number of active contacting metals absorb or reduce native oxides - see document J.H. Pimbley: "VLSI Electronics Microstructure Science", Vol. 19, 1989, page 60, last paragraph, to page 61, paragraph 1; as expert opinion - this fact would only represent a disregardable bonus effect in the obvious application of the alloying technique of document D2; see also the decision T 192/82, OJ EPO 1984, 415, in particular paragraph 16.

2.9 For the above reasons, the Board regards it as obvious to make use of the siliciding technique known from document D2 in the high resistance element producing method of document D4.

3. Therefore, Claim 1 is considered to lack an inventive step and not to be allowable with regard to Articles 52(1) and 56 EPC. Claims 2 to 15 fall because of their dependence on Claim 1.

Order

For these reasons, it is decided that:

The appeal is dismissed.

The Registrar: The Chairman:

M. Beer G.D. Paterson