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Bezeichnung der Erfindung: PLL Control Circuit
Title of invention:
Titre de l'invention :

Klassifikation / Classification / Classement : G11B 5/09

ENTSCHEIDUNG / DECISION

vom / of / du 15 November 1990

Anmelder / Applicant / Demandeur :

Patentinhaber / Proprietor of the patent /
Titulaire du brevet : KABUSHIKI KAISHA TOSHIBA

Einsprechender / Opponent / Opposant : N.V. Philips' Gloeilampenfabrieken

Stichwort / Headword / Référence :

EPÜ / EPC / CBE Articles 54, 56, 114(1), 114(2)

Schlagwort / Keyword / Mot clé : "Novelty - yes" -
"Inventive step - no" -
"Late filed documents considered"

Leitsatz / Headnote / Sommaire

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Case Number : T 486/89 - 3.5.2

D E C I S I O N
of the Technical Board of Appeal
of 15 November 1990

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Decision under appeal :
Decision of the Opposition Division of the European Patent Office dated 14 June 1989 rejecting the opposition filed against European patent No. 0 096 106 pursuant to Article 102(2) EPC.

Composition of the Board :

Chairman : E. Persson
Members : W.J.L. Wheeler
A. Hagenbucher

Summary of Facts and Submissions

I. The grant of European patent No. 96 106 on the Respondent's European patent application No. 82 109 205.3, which was filed on 5 October 1982 claiming priority from a previous application in Japan dated 15 June 1982, was published on 19 March 1986. As granted, the patent had eight claims, of which Claim 1 was worded as follows:

"1. A phase locked loop control circuit for a digital information reproduction system such as a digital audio disk system, said phase locked loop control circuit having oscillator means (116) to produce an oscillation signal the frequency of which being controlled by an oscillation control signal, comparator means (110) connected to receive a first electrical signal which corresponds to a phase state of a digital information signal read out from a recording medium (54) of said information reproduction system and which has inverting period values in a range determined by minimum and maximum period values inherently defined in accordance with a chosen modulation technique, and the oscillation signal from said oscillator means (116), respectively, at first and second input terminals for producing a second electrical signal (128) which corresponds to the phase difference between the first signal and the oscillation signal and which is used to control the frequency of the oscillation signal, characterized in that said phase locked loop control circuit comprises detector means (122) for extracting a specific inverting period value from the readout digital audio signal to detect a deviation between said specific inverting period value and a period value obtained on the basis of said oscillation signal and for generating a third electrical signal (126) corresponding to said deviation, and adder means (112) connected to the output

terminals of said comparator means (110) and said detector means (122) for adding the second (128) and third (126) electrical signals and for supplying the added signals as said oscillation control signal to said oscillator means (116)."

Claims 2 to 8 were dependent on Claim 1.

II. On 16 December 1986 the Appellant filed an opposition, requesting revocation of the patent on the ground that its subject-matter did not involve an inventive step. Several prior art documents were cited, of which only the following is relevant to the present appeal:

DE-A-3 137 907 (Reference R4).

III. In the course of the proceedings before the Opposition Division, the Appellant cited the following additional prior art documents:

Electronic Components and Applications, Vol. 4, No. 3, May 1982, pages 131 to 141, Matull: "ICs for Compact Disc decoders" (Reference R8)
Textbook "Phaselock Techniques" by F.M. Gardner, 2nd edition, 1979, pages 84 to 87 (Reference R9)
Philips publication "Demodulator I.C. for the Compact Disc Digital Audio System", April 1982 (Reference R10)
Philips publication No. 82905 "News Report on ICs for Compact Disc", April 1982 (Reference R11).

IV. The Opposition Division took References R8 and R9 into account, but exercised discretion under Article 114(2) EPC to disregard References R10 and R11. The Opposition Division rejected the Opposition by a decision dispatched on 14 June 1989.

V. On 27 July 1989 the Appellant filed a notice of appeal against that decision, and paid the appeal fee. A written statement setting out the grounds of appeal was filed on 22 September 1989. It contains reasoning based on References R4, R8, R9 and R10.

VI. In a reply dated 5 April 1990, received on 6 April 1990, the Respondent defended the patent as granted and filed an alternative set of Claims 1 to 7 as an auxiliary request. Claim 1 of the auxiliary request was worded the same as Claim 1 of the main request except that the following passage was added at the end of the claim:

"and that said oscillator means comprises a voltage-controlled oscillator (116) which is arranged to have an output terminal connected to said detector means (112)."

VII. In a communication of the Board pursuant to Article 11(2) of the rules of procedure of the Boards of Appeal, it was noted that documents R8, R10 and R11 all related to the same piece of prior art, namely the SAA7010 chip, the precise details of which were in dispute. The Board, therefore, considered it appropriate, in the interests of a proper appreciation of the prior art, to take R10 and R11 into account in the present appeal.

VIII. Oral proceedings were held before the Board on 26 October 1990.

IX. The Appellant argued essentially that the detector 122 of the opposed patent was identical to the Tmax detector consisting of blocks 16b, 17b, 18b, 8 and 19 in Fig. 3 of R4 and that it was obvious to use the Tmax detector known from R4 in a combined phase and frequency control loop such as was known from R9 or R8 (SAA7010 chip and

associated circuitry as shown in Fig. 6 of R8). R10 contained further explanation of the SAA7010 chip and disclosed a Tmax detector in connection with the frequency detector. According to decision T56/87 (OJ EPO, 1990, 188) a piece of prior art should be considered in its entirety, as it would be done by a person skilled in the art. A skilled person would read R8 and R10 together as relating to the same piece of prior art. Claim 1 of the opposed patent did not specify to what extent the third electrical signal had to correspond to the frequency deviation. The too high, too low or inactive output of the frequency detector of the SAA7010 chip met the correspondence requirement as specified in the claim. R10 disclosed that the VCO output signal was used for all internal timing. It was clear to a skilled person that it must be fed back to the frequency detector, otherwise the control loop would be unstable. R10 alone or in combination with R8 anticipated Claim 1 of the opposed patent as granted or as amended in the auxiliary request.

X. The Respondent argued essentially that R4 related to motor control, not to VCO control. The Tmax detector known from R4 was not identical to that used in the present invention: in R4, Tmax was compared with a constant reference, whereas in the present invention it was compared with a signal obtained on the basis of the VCO output signal. It would be illogical to put the Tmax detector known from R4 in the circuit known from R9, since the latter circuit was not intended for use in a digital information reproduction system and did not have a Tmax detector. Use of the Tmax detector known from R4 in the frequency detector shown only as a block in R8 would not produce the present invention, since the Tmax detector would have a fixed reference and would not receive feedback from the VCO. The Opposition Division acted in accordance with decision T 156/84 (OJ EPO, 1988, 372) when

it disregarded R10 and R11. According to the fourth paragraph on page 12 of R10, Tmax and Tmin were used as frequency limit signals for the frequency detector. The Tmin and Tmax detectors were not part of the frequency detector. The three state push-pull output of the frequency detector did not correspond in magnitude to the deviation. In the third paragraph on page 12 of R10, the clock signal (output from the VCO) was only stated to be fed back to the phase detector. There was no disclosure in R8 or R10 of any feedback from the VCO to the frequency detector. There was no disclosure in R8 or R10 of how the frequency detector worked. The combined disclosure of R8 and R10 did not anticipate the present invention.

XI. The Appellant requested that the decision of the Opposition Division be set aside and that the patent be revoked.

XII. The Respondent requested that the appeal be dismissed and the patent maintained as granted (main request), or on the basis of Claims 1 to 7 filed on 6 April 1990 (auxiliary request).

Reasons for the Decision

1. The appeal complies with Articles 106 to 108 and Rule 64 EPC and is, therefore, admissible.

2. Documents R8 to R11 were filed after expiry of the 9-month period specified in Article 99(1) EPC. The Opposition Division exercised discretion under Article 114(2) EPC to disregard R10 and R11. However, both parties have presented to the Board arguments referring to R8 and R10. The Board has found R10 helpful in throwing light on the prior art chip SAA7010, the details of which

are in dispute, and therefore chooses not to disregard it. Since neither party referred to R11 in the present appeal, the Board will not consider it in the reasons for the decision.

3. After hearing the parties, the Board is of the opinion that the closest prior art is the demodulation circuit shown in the upper diagram of Fig. 6 on page 135 of R8. That circuit includes the SAA7010 chip, further details of which are given in R10. Although it does not follow from the Appellant's reference to the decision in case T 56/87 (see IX above), because the circumstances there were different from those in the present case, the Board nevertheless takes the view that a person skilled in the art would read these two references together as relating to the same piece of prior art.

3.1 R8 and R10 disclose a prior art circuit comprising the following features of relevance to Claim 1 of the opposed patent as granted:

A phase locked loop (PLL) control circuit for a digital audio disc (DAD) system, which PLL control circuit includes an oscillator (8.64 MHz VCO) to produce an oscillation signal the frequency of which is controlled by an oscillation control signal,

a phase comparator (in the phase and frequency detector block) connected to receive a first electrical signal corresponding to a phase state of a digital audio signal read out from a recording medium of the DAD system and which has inverting period values in a range determined by minimum and maximum period values (Tmin and Tmax) inherently defined in accordance with a chosen modulation technique (EFM), and the oscillation signal from the VCO, respectively, at first and second input terminals for

producing a second electrical signal (PD1, PD2) which corresponds to the phase difference between the first signal and the oscillation signal and which is used to control the frequency of the oscillation signal (see connections from PD1, PD2 via the loop amplifier and varicap to VCO1, VCO2, as shown in Fig. 6 of R8),

detector means for extracting specific inverting period values (Tmin and Tmax, see R10, page 12, fourth paragraph) from the read-out digital audio signal to provide frequency limit signals for a frequency detector (in the phase and frequency detector block),

wherein the frequency detector provides a coarse control signal for the PLL system (see R10, page 12, third paragraph) by generating a third electrical signal (the three state push-pull output FD, see R10, page 4, for pin 23) corresponding to a detected deviation,

and adder means (circuitry connected between FD, PD2, PD1, OA1 and OA2) connected to the output terminals of the phase comparator and the frequency detector for adding the second and third electrical signals and for supplying the added signals as said oscillation control signal to the VCO.

3.2 It is appropriate to note here that, in the opinion of the Board, the wording in the characterising part of Claim 1 of the patent as granted, namely "to detect a deviation ... and for generating a third electrical signal corresponding to said deviation", encompasses the possibility that the third signal could be a three state push-pull signal corresponding to the detected presence and direction of a deviation or to the absence of a deviation. The claim does not require a full correspondence with the magnitude of the deviation.

3.3 Thus R8 and R10 explicitly disclose nearly all the features specified in Claim 1 of the opposed patent as granted. The only feature specified in that claim which is not explicitly disclosed in R8 and R10 is the detection of a deviation between the specific inverting period (in practice Tmax) and a period value obtained on the basis of said oscillation signal.

4. The Appellant argued that to a person skilled in the art it was implicit that there must be feedback from the VCO to the frequency detector in the prior art circuit known from R8 and R10, otherwise the PLL loop would be unstable: any deviation detected by the frequency detector would lead to the VCO being controlled to its maximum or minimum frequency, according as the three state push-pull signal FD indicated the frequency of the VCO to be too low or too high. To a person skilled in the art it was, therefore, implicit that the frequency detector in the prior art circuit known from R8 and R10 detected deviation between the specific inverting periods Tmin and Tmax of the EFM signal and corresponding period values obtained on the basis of said oscillation signal.

4.1 The Respondent contested the implication in point 4 above and argued that a direct feedback from the VCO was neither disclosed nor necessary in the system known from R8 and R10. In the motor control system known from R4, Tmax was compared with a constant reference (19, Fig. 3), this being possible because the desired value of Tmax was known beforehand. It must be assumed that in the system known from R8 and R10, as in the present invention (see Fig. 2 of the opposed patent), the clock output of the PLL loop was also used to control the disc drive motor and would consequently affect Tmin and Tmax of the read-out EFM signal.

4.2 The Board notes that the Respondent's assumption that in the system known from R8 and R10 the clock output of the PLL loop was also used to control the disc drive motor is confirmed by R8, see Fig. 5 on page 134, noting the output shown from the SAA7020 chip to the motor control and the corresponding description in the third paragraph of the second column on page 136, according to which any discrepancy between the clock derived in the demodulator (i.e. from the VCO in the SAA7010 chip) and that from the crystal oscillator (in the SAA7020 chip) generates an error signal MCES which controls the speed of the motor spinning the disc.

4.3 Furthermore, it is noted that in the third paragraph on page 12 of R10, which discloses that a frequency detector and a phase detector provide the coarse and fine control signal for the phase locked loop (PLL) system, it is stated that the clock signal (VCO output divided by 2) completes the PLL loop when it is compared with the incoming data in the phase detector. This might be taken to imply that the PLL loop is complete without feedback from the VCO to the frequency detector.

4.4 On the other hand, near the top of page 1 of R10 it is stated: "A nominal 4.3MHz clock locked to the disc rate is also produced." The first item in the list of "Features" is: "Phase locked loop clock regenerator with frequency detector for locking". This might be taken to imply that there is feedback from the VCO to the frequency detector, especially as it belongs to the general knowledge of the person skilled in the art of phaselock circuits that a frequency difference discriminator can be added to a phaselock loop to bring the frequency of a VCO close to that of the signal to which it is to be phaselocked, see the text book R9, section headed Discriminator-Aided

Frequency Acquisition, noting that Fig. 5.12 on page 85 of R9 shows a PLL circuit with feedback from a VCO to a phase detector and a frequency difference detector whose outputs (after filtering) are added to produce the control signal for the VCO.

4.5 In the light of the above conflicting considerations, the Board cannot be absolutely sure as to whether the prior art circuit known from R8 and R10 includes feedback from the VCO to the frequency detector or not. The Board resolves this uncertainty to the benefit of the Respondent.

4.6 Such feedback is a requirement of Claim 1 of the patent as granted, which recites "a period value obtained on the basis of said oscillation signal". In the opinion of the Board, this excludes a fixed reference value calculated on the basis of the theoretical value of the frequency of the VCO. In Claim 1 of the auxiliary request, it is explicitly recited that the VCO has an output terminal connected to the detector means (122).

4.7 The Board, therefore, concludes that it has not been proven that Claim 1 of the patent as granted lacks novelty compared with the prior art known from R8 and R10. The same applies to Claim 1 of the auxiliary request.

5. However, as far as the question of inventive step is concerned, the problem solved by the circuit presently claimed according to the main and auxiliary requests, is the provision of a large enough capture range for the PLL. In the opinion of the Board, this problem is an obvious one to want to solve.

5.1 Now, as noted under point 4.4 above, it was already known from R8 and R10 to provide the PLL with a frequency

detector for locking, see e.g. the first "Feature" specified on page 1 of R10, although the precise details of how this was done are not clear from R8 and R10. Furthermore, as explained under point 4.4 above with reference to R9, it is part of the general knowledge of the person skilled in the art that one way of implementing the phase locked loop clock regenerator with frequency detector for locking, would be to provide feedback from the VCO to the frequency detector.

5.2 Moreover, as is explained in the right-hand column on page 133 of R8, the EFM signal contains minimum and maximum inverting periods (Tmin and Tmax in the terminology used in the opposed patent) for the express purpose of ensuring that the bit clock can be regenerated.

5.3 It therefore appears to the Board that it would be obvious to a person skilled in the art, starting from the prior art known from R8 and R10 and seeking to fill in the unclear details of the frequency lock on the basis of his general knowledge, to arrange for the frequency detector to detect a deviation between the value of Tmax (and/or Tmin, it doesn't matter) extracted from the read-out EFM signal and a period value obtained from the output of the VCO. In so doing he would make a circuit falling within the scope of Claim 1 of the Respondent's main and auxiliary requests.

5.4 In the result, the Board decides that the subject-matter claimed in Claim 1 of the Respondent's main and auxiliary requests does not involve an inventive step within the meaning of Article 56 EPC. Therefore, the patent cannot be maintained.

Order

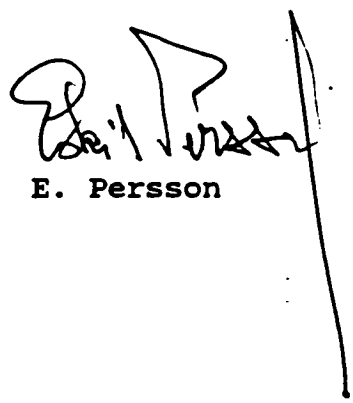
For these reasons, it is decided that:

1. The decision under appeal is set aside.

2. European Patent No. 96 106 is revoked.

The Registrar: **The Chairman:**

M. Kiehl



E. Persson

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