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Anmeldenummer / Filing No / N° de la demande : 84 402 757.3

Veröffentlichungs-Nr. / Publication No / N° de la publication : 149 402

Bezeichnung der Erfindung:
Title of invention:
Titre de l'invention : Programmable semiconductor memory device

Klassifikation / Classification / Classement : G11C 17/00

ENTSCHEIDUNG / DECISION

vom / of / du 3 May 1990

Anmelder / Applicant / Demandeur : FUJITSU LIMITED

Patentinhaber / Proprietor of the patent /
Titulaire du brevet :

Einsprechender / Opponent / Opposant :

Stichwort / Headword / Référence :

EPÜ / EPC / CBE Articles 56, 122

Schlagwort / Keyword / Mot clé : "Restitutio in integrum - granted"
"Inventive step - yes, after amendment"

Leitsatz / Headnote / Sommaire

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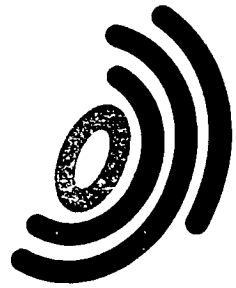

Case Number : T 178/89 - 3.5.1

D E C I S I O N
of the Technical Board of Appeal 3.5.1
of 3 May 1990

Appellant : FUJITSU LIMITED
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Decision under appeal : Decision of Examining Division 067 of the European Patent Office dated 30 September 1988 refusing European patent application No. 84 402 757.3 pursuant to Article 97(1) EPC

Composition of the Board :

Chairman : P.K.J. van den Berg
Members : W.J.L. Wheeler
E. Persson

Summary of Facts and Submissions

I. Appellant's European patent application No. 84 402 757.3, filed on 28 December 1984, claiming priority from a previous application in Japan dated 29 December 1983, was refused by a decision of the Examining Division dated 30 September 1988. That decision was taken on the basis of Claims 1 to 5 filed with the letter dated 19 August 1988.

II. The reason given for the refusal was that the subject-matter of the claims did not involve an inventive step, having regard to the following prior art documents:

D1: Paper by R.L. Cline: "Design limitations in bipolar PROMS 16k and larger" in 1978 WESCON TECHNICAL PAPERS, Los Angeles, California, 12-14 September 1978, Vol. 22, section 9/2, pages 1 to 6.

D2: US-A-3 533 088.

III. On 10 December 1988 the Appellant filed a notice of appeal against that decision. The appeal fee was paid on 7 December 1988. The statement of grounds was filed on 8 March 1989, together with replacement Claims 1 to 5 and a substantiated request for restitutio in integrum.

IV. In response to communications of the Board pursuant to Article 110(2) EPC, in which it was indicated that the request for restitutio in integrum would be granted, but certain deficiencies had to be corrected before the Board could order grant of a patent, the Appellant filed on 28 March 1990 a replacement page containing an amended Claim 1 and part of Claim 2, and replacement pages of description.

V. The Appellant requests, in effect, that the decision under appeal be set aside and a patent granted on the basis of the following documents:

- Claim 1 and Claim 2 (part), filed on 28 March 1990;
- Claim 2 (part) and Claims 3 to 5, filed on 8 March 1989;
- Description: pages 1, 2, 2a, 3, 7 and 9, filed on 28 March 1990; pages 4 to 6 and 8, as originally filed on 28 December 1984;
- Drawings, sheets 1/3 to 3/3 as originally filed on 28 December 1984.

VI. Claim 1 is now worded as follows:

"1. A programmable semiconductor memory device comprising:

a plurality of word lines (WL_1 - WL_m);

a plurality of bit lines (BL_1 - BL_ℓ) crossing said word lines;

programmable memory cells ($PMC_{m\ell}$) arranged at respective crossing points of said word lines and bit lines;

a word line address decoder (WD) for selecting one of said word lines in response to an input address signal (A_o - A_n); and

a word line driver means (DR) for absorbing a read current from the word line selected by the word line address decoder during a read operation of said programmable memory cells, and for absorbing a current from the word line selected by the word line address decoder during a write operation of said programmable

memory cells in which a write current flows from a selected bit line to said selected word line through said memory cell at their crossing point,

characterized in that said word line driver means comprises two separate drivers, both being driven in parallel by the word line address decoder, namely a read word line driver (DR), for absorbing said read current during a read operation, and a write only word line driver (DW), for absorbing said write current during the write operation, and that a cutting means (C_1 - C_m) is provided for cutting the connections between said write-only word line driver (DW) and said word lines, said cutting means comprising a plurality of fuses (F_{w1} - F_{wm}) respectively connected between said write-only word line driver and said word lines, the arrangement being such that said fuses can be broken after a writing operation is completed."

Claims 2 to 5 are dependent on Claim 1.

Reasons for the Decision

1. In the light of the documents filed in support of the request for restitutio in integrum the Board is satisfied that the Appellant had arranged a proper system for monitoring time limits, including a back up system, that the operation of this system was entrusted to suitable persons, and that the system was normally satisfactory. The present Board endorses the view taken by the Legal Board of Appeal in the case J 02/86 (Isolated mistake - restitutio/MOTOROLA, OJ EPO 1987, 362) that Article 122 EPC is intended to ensure that in appropriate cases the loss of substantive rights does not result from an isolated procedural mistake within a normally satisfactory system.

Thus, the Appellant's rights shall be restored and the statement setting out the grounds of appeal shall be deemed to have been filed in time.

2. After grant of the request for restitutio in integrum in respect of the time limit for filing the statement of grounds of appeal, the appeal complies with Articles 106 to 108 and Rule 64 EPC and is, therefore, admissible.

3. In the opinion of the Board, the present claims comply with Article 123(2) EPC. The present Claim 1 differs from the originally filed Claim 1 in that it has been recast in the two part form in accordance with Rule 29(1) EPC, reference signs have been introduced in accordance with Rule 29(7) EPC, certain features relating to the flow of the write current are now explicitly recited (they were implicit in the originally filed Claim 1 and described on originally filed pages 5 and 6), and the details of the cutting means (originally in Claim 3) have been included in Claim 1. Present Claims 2, 3, 4 and 5 correspond with original Claims 2, 4, 5 and 6 respectively.

4. The prior art portion of Claim 1 recites well known features of conventional programmable semiconductor memory devices, such as bipolar PROMS.

5. D1 discusses certain design limitations of bipolar PROMS. Teaching relevant to the present application appears in the section headed "Performance" on page 4 and in the section headed "A 32K PROM" on pages 6 and 7. The Board agrees with the Appellant that that teaching may be summarised as: bipolar PROMs have to be fast; high currents are needed to blow the fuse links for programming, requiring large transistors which are incompatible with optimum AC performance; superior performance has been obtained at the expense of chip area by using two sets of column decoders, one for programming (big transistors) and one for normal

operation (small transistors); a better approach is to include SCRs (in addition to small decoding transistors) in both the row and column drivers, for use during programming. D1 does not explicitly disclose two separate word line drivers driven in parallel by a word line address decoder or say anything at all about disabling the big transistors or SCRs after programming has been carried out.

6. The programmable semiconductor memory device according to the present Claim 1 of the present application differs from the prior art teaching derivable from D1 in that (a) the word line driver means comprises two separate drivers driven in parallel by the word line address decoder, namely a read word line driver for absorbing read current during a read operation and a write-only word line driver for absorbing write current during the write operation, and in that (b) cutting means is provided for cutting the connections between said write-only word line driver and said word lines, said cutting means comprising a plurality of fuses respectively connected between said write-only word line driver and said word lines, the arrangement being such that said fuses can be broken after a writing operation is completed.

7. Starting from the prior art according to D1, the problem solved by the present invention may be seen as twofold: first, filling in the missing details of the means for addressing the word line drivers - solved by (a); and second, how to prevent the high parasitic capacitance of the large transistors in the write-only word line drivers from adversely influencing read-out speed - solved by (b).

8. While it may be obvious to solve the above stated first problem by means of (a), the solution (b) of the second problem is not obvious, in the opinion of the Board, for

the following reasons. There is no evidence on the file that the desirability of cutting the connections between the write-only word line driver and the word lines to reduce the parasitic capacitance had been previously recognised. D1 is silent on this. Although it may be obvious that some means must be provided for preventing accidental operation of the big transistors or SCRs once programming has been completed, that in itself does not appear to necessitate cutting the connections between the write-only word line driver and the word lines. In D2, fuses (FA, FB, FC etc.) are provided for preventing the writing in of additional information after a write-in command has been terminated, but those fuses do not cut the connections between the line drivers and the word lines. Applying the teaching of D2 to the PROMs known from D1 would not lead to the invention as now claimed in Claim 1 of the present application. It is only after it has been appreciated that the permanently disabled write-only word line driver contributes parasitic capacitance which is worth while eliminating, that it becomes obvious to cut the connections between the line driver and the word lines.

9. In the result, the Board takes the view that the programmable semiconductor memory device now claimed in the present version of Claim 1 of the application involves an inventive step over the cited prior art and the decision under appeal must therefore be set aside.

10. The amendments made to the description are only for the purposes of adapting it to the present claims, acknowledging the prior art in accordance with Rule 27(1)(c) EPC, correcting obvious errors and removing inconsistencies. In the opinion of the Board, the current version of the application complies therefore as a whole with Article 123(2) EPC and meets the requirements for the grant of a European patent.

Order

For these reasons, it is decided that:

1. The request for restitutio in integrum in respect of the time limit for filing the statement of grounds of appeal is granted.

2. The decision under appeal is set aside.

3. The case is remitted to the first instance with the order to grant a patent on the basis of the Appellant's request (paragraph V above).

The Registrar: The Chairman:

M. Beer P.K.J. van den Berg