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Datasheet for the decision of 27 January 2025

Case Number: T 0316/22 - 3.5.06

Application Number: 16750681.5

Publication Number: 3329365

IPC: G06F9/30, G06F9/38

Language of the proceedings: EN

Title of invention:
VECTOR PROCESSING USING LOOPS OF DYNAMIC VECTOR LENGTH

Applicant:
ARM Limited

Headword:
Predicate flags/ARM

Relevant legal provisions:
EPC Art. 83, 84, 123(2)
RPBA 2020 Art. 11

Keyword:
Sufficiency of disclosure - (yes)
Claims - clarity (yes)
Amendments - extension beyond the content of the application as filed (no)

Decisions cited:
G 0001/03

Catchword:

Europäisches Patentamt
European Patent Office
Office européen des brevets

Beschwerdekammern

Boards of Appeal

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Case Number: T 0316/22 - 3.5.06

D E C I S I O N
of Technical Board of Appeal 3.5.06
of 27 January 2025

Appellant: (Applicant)	ARM Limited 110 Fulbourn Road Cherry Hinton Cambridge CB1 9NJ (GB)
Representative:	D Young & Co LLP 3 Noble Street London EC2V 7BQ (GB)
Decision under appeal:	**Decision of the Examining Division of the European Patent Office posted on 5 October 2021 refusing European patent application No. 16750681.5 pursuant to Article 97(2) EPC.**

Composition of the Board:

Chairman	M. Müller
Members:	G. Zucka
	K. Kerber-Zubrzycka

Summary of Facts and Submissions

I. The appeal is against the decision by the examining division, dispatched with reasons on 5 October 2021, to refuse European patent application 16750681.5, on the basis that the invention was not sufficiently disclosed in the application documents (Article 83 EPC). For its reasons, the decision, issued "according to the state of the file", made reference to the communication annexed to the examining division's summons to oral proceedings. No documents were cited during the first instance proceedings.

II. A notice of appeal was received on 9 December 2021, the appeal fee being paid on the same day. A statement of grounds of appeal was received on 2 February 2022.

III. The appellant requested that the decision under appeal be set aside and a patent be granted on the basis of claims 1 to 12 of the main or the auxiliary request filed with the statement of grounds of appeal. The appellant made a conditional request for oral proceedings.

IV. The board issued a summons to oral proceedings. In an annex to the summons, the board set out its preliminary opinion on the appeal, according to which neither request was allowable.

V. On 14 January 2025, the appellant filed claims for a main and three auxiliary requests, replacing the requests then on file.

VI. In the course of the oral proceedings before the board, the appellant filed claims for a new request via e-mail and declared this to be its sole request.

VII. The appellant requests that the decision under appeal be set aside and a patent be granted on the basis of claims 1 to 8 of the request labelled "first auxiliary request revised during OPs 27 Jan 2025" filed during the oral proceedings before the board.

VIII. Independent claim 1 reads as follows:

"Data processing apparatus comprising:

instruction decoder circuitry (50) to decode instructions; and

instruction processing circuitry (60, 90) to execute instructions decoded by the instruction decoder circuitry;

the instruction decoder circuitry being responsive to a WHILE instruction associated with a limit value and a counter variable, to control the instruction processing circuitry to:

determine, based on whether the counter variable and the limit value satisfy an arithmetic condition, whether to control a change of program flow, where controlling the change of program flow comprises performing a branch or setting one or more condition flags to control whether a separate branch instruction performs the branch, in which the arithmetic condition is a condition selected from the list consisting of:

the counter variable being less than an upper limit value;

the counter variable being greater than a lower limit value;

the counter variable being less than or equal to an upper limit value; and

the counter variable being greater than or equal to a lower limit value;

and select one or more predicate flags for setting to an active state so that a value of the counter variable, taking into account the number of predicate flags selected for setting to the active state, does not breach the arithmetic condition, wherein the predicate flags in the active state are indicative of positions of a data vector at which a vector processing instruction should be applied; and

the instruction decoder circuitry being responsive to a CHANGE instruction to control the instruction processing circuitry to change the value of the counter variable by an amount dependent upon a number of the predicate flags according to an associated saturation value so as to change the value of the counter variable no further than the saturation value."

IX. Independent claim 6 relates to a data processing method having method features corresponding to the features of independent apparatus claim 1.

X. Independent claim 7 relates to software implementing the method of claim 6.

XI. Independent claim 8 relates to a storage medium storing the software of claim 7.

XII. The further text on file is:

description pages
2 to 22 as originally filed,

1 and 23 received on 14 September 2018;

drawing sheets
1 to 6 as originally filed.

XIII. At the end of the oral proceedings, the chairman announced the board's decision.

Reasons for the Decision

1. *The application*

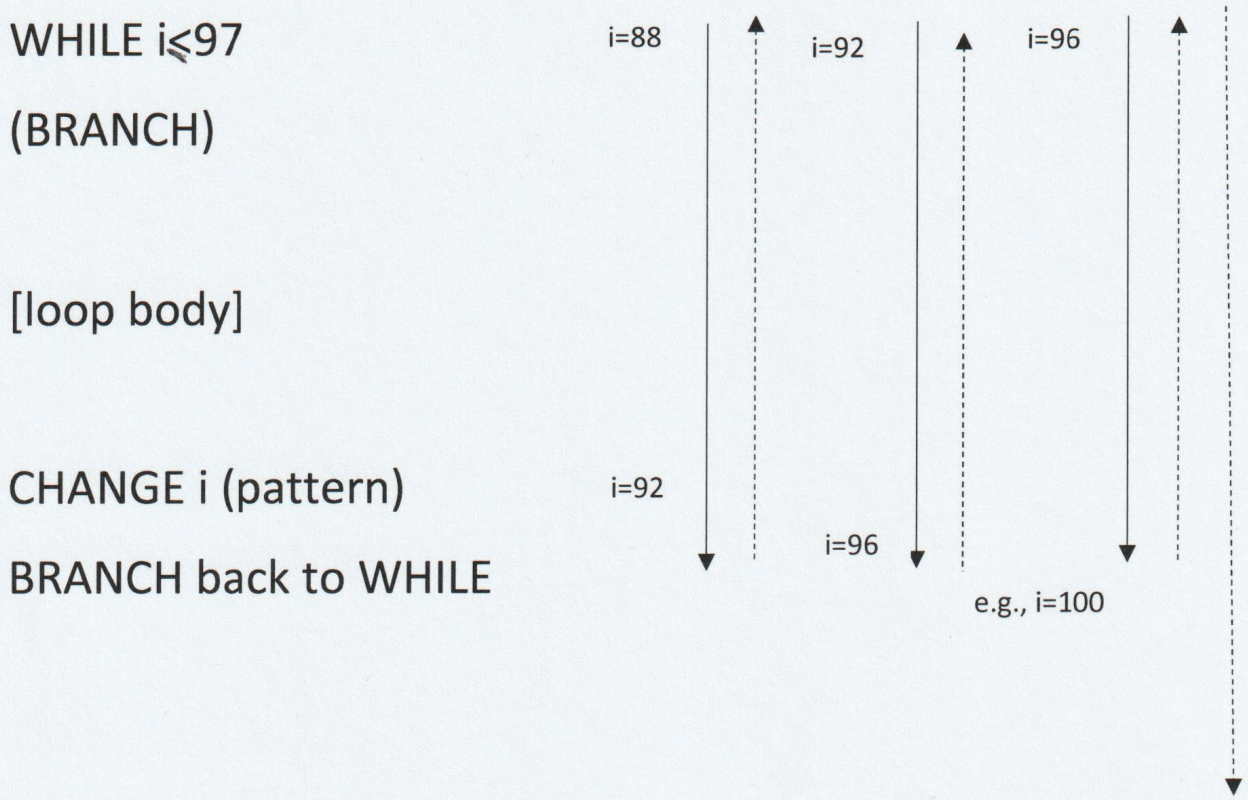
The application relates to vector processing operations, whereby a single vector processing instruction is applied to data items of a vector having a plurality of data items at respective positions in the data vector (description, page 1, lines 5 to 7). This can improve the efficiency and throughput of data processing compared to scalar processing (*ibid.*, lines 11 and 12).

According to the statement of grounds of appeal (section "Overview" spanning pages 1 and 2), the context of the invention is one where the vector length V_L is not fixed at the onset. WHILE and CHANGE instructions are used to control the advancement and termination of unrolled loops, i.e. loops where multiple operations are executed by the vector processor in an SIMD (single instruction multiple data) fashion, so that at each loop iteration a number of operations is conducted which depends on the vector length V_L.

At each loop iteration, a loop counter is advanced by the CHANGE instruction by an amount dependent on the vector length V_L. Each loop iteration is controlled by the WHILE instruction by setting so-called "predicate flags" to indicate which data items are to be vector processed in the current iteration, and so that the final iteration goes no further than the required number of operations.

The CHANGE instruction uses a proxy for the prevailing or applicable vector length, this proxy being the number of predicate flags.

The appellant handed out the following schematic illustration of the working of the claimed apparatus during the oral proceedings:



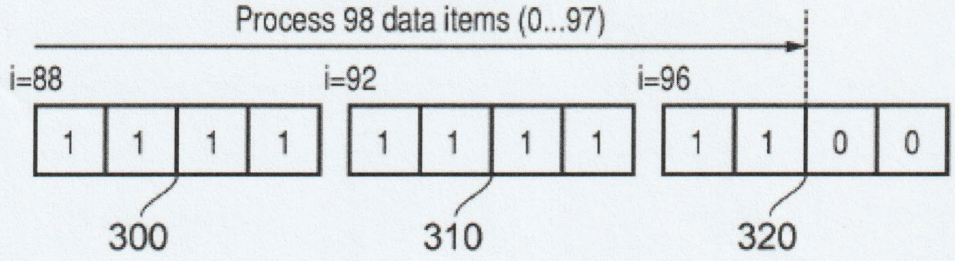


FIG. 5

- control of loop using WHILE – p. 16, l.14-18
  - separate branch optional – p. 13, l. 6-13
- change at end of loop – p. 18, l.12-13 (equating to step 220 or step 470)

2. *Amendments; Article 123(2) EPC*

Compared to claim 1 as originally filed, present claim 1 contains the following amendments:

(a) *The WHILE instruction is associated with a limit value and a counter variable.*

This is based on original figure 6 and page 16, lines 27 to 33 of the original description.

(b) *The instruction processing circuitry is controlled to determine, based on whether the counter variable and the limit value satisfy an arithmetic condition, whether to control a change of program flow.*

This is based on the original description page 6, lines 21 to 24 and page 13, lines 6 to 13.

(c) *Controlling the change of program flow comprises performing a branch or setting one or more condition flags to control whether a separate branch instruction performs the branch*

This is based on the original description page 13, lines 6 to 13.

(d) *The arithmetic condition is a condition selected from the list consisting of: the counter variable being less than an upper limit value; the counter variable being greater than a lower limit value; the counter variable being less than or equal to an upper limit value; and the counter variable being greater than or equal to a lower limit value.*

This is based on the original description page 6, lines 24 to 29, and original claim 2.

(e) *One or more predicate flags are selected for setting to an active state so that a value of the counter variable, taking into account the number of predicate flags selected for setting to the active state, does not breach the arithmetic condition.*

This is based on originally filed claim 24.

3. *Clarity; Article 84 EPC*

3.1 The board had raised a number of clarity issues in its summons (point 4.). It is satisfied that these were properly addressed in the current claim set.

Concerning point 4.1 of the summons, the board notes that a "processing loop" is no longer claimed, that the predicate flags are indeed part of the claimed apparatus, and that the WHILE and CHANGE instructions and their arguments, esp. the limit value and the counter variable, as well as the data vector are not *per se* part of the claimed apparatus but define the input it is meant to work on.

Concerning point 4.4 of the summons, the board takes note of the appellant's explanation made during oral proceedings that the term "predication" is commonly used in the context of processor architectures to control the conditional execution of instructions, but otherwise accepts the appellant's concession, also made during the oral proceedings, that as far as the claim is concerned, the term "predicate flags" is synonymous with "flags".

3.2 Concerning point 4.5 of the summons, the board has no reason to doubt the appellant's argument that the term "the saturation value" of a counter variable is understood by the person skilled in the art.

3.3 The board notes that the Written Opinion of the International Searching Authority (Separate Sheet point 4.) had considered certain features which were not present in then claim 1 to be essential for achieving the aim of the invention as stated in the application (see page 5, lines 15 to 20). The board sees however no reasons why the present claim 1, which shares many features with that earlier version of the claim, would be missing any essential features:

Concerning point 4.1 of said Separate Sheet, the board is of the opinion that it is not essential for the vector length and the WHILE, the CHANGE and the vector processing instructions to be part of a loop. Whilst according to the passage cited under 4.1 (which is on page 5, lines 15 to 20 of the description) the invention consists in providing instructions which are intended to be used in the coding of a loop, the loop itself is not a required part of the invention; it only emerges when the instructions are put to their intended use. What is essential (and follows from the claim) is that the programmer can use the WHILE and CHANGE instructions without needing to know V_L, whilst their execution does control the amount of parallelism.

Concerning point 4.2 of said Separate Sheet, the board is of the opinion that it is not essential to specify which predicate flags are set or how, especially considering that the description mentions different possible ways to set them (e.g. on page 9, lines 5 to 16, as well as figures 10 and 11 and related

description on page 18, line 33, to page 21, line 3) and leaves open additional possibilities. The invention as currently claimed is focussed on the circuitry executing the WHILE and CHANGE instructions and especially its use of "predicate flags" to control the parallelism in each iteration and to make sure that only the specified overall number of iterations is carried out.

Concerning point 4.3 of said Separate Sheet, the board considers that the number of available predicate flags is known for any given hardware constellation (see below). There is therefore no need to determine it.

Concerning point 4.5 of said Separate Sheet, the board accepts the argument made by the appellant during the oral proceedings that "a number of the predicate flags" as claimed does not necessarily designate all available predicate flags but may also relate to a subset of these, e.g. only those which have been set to an active state, and that the wording of the claim intends to cover all such cases.

3.4 The board therefore holds that claim 1 and for similar reasons claims 6, 7 and 8 satisfy the requirements of Article 84 EPC.

3.5 The board does agree with the examining division insofar as the claims do no completely specify the instruction processing circuitry necessary to implement WHILE and CHANGE instructions ready for use by the programmer to define a loop. The board notes however that the claims do not - and are not meant to - specify that a loop is to be defined, or which one, so that features missing to specify the implementation of any particular loop are not "essential" for the invention.

In other words, the board considers gaps in what the claims specify to be, in the case to hand, a matter of breadth rather than lack of clarity. That such gaps may, of course, influence which technical effects can be associated with the claimed subject-matter is to be considered with respect to Article 56 EPC.

4. *Sufficiency of disclosure; Article 83 EPC*

According to the communication referred to in the decision under appeal (point 3.1), the feature according to which the value of the counter variable is changed by "an amount dependent on a number of the predicate flags" lacks sufficient disclosure in the application as filed. The skilled person would also not know from general knowledge how to implement the determination of the number of predicate registers in a vector processor (point 3.12).

With regard to the present version of claim 1, the board accepts the reasoning made by the appellant during the oral proceedings that the quantity of available predicate flags would be fixed by the hardware, i.e. it would already be known by the processing apparatus as claimed (as expressed by the examining division itself; *ibid.* 3.9). The board also notes that this holds irrespective of whether the number of predicate flags is the same as or different from the number of processing lanes (points 3.6 and 3.10). For that reason, there is no need to specify in the application in what manner the number of predicate flags can be established.

Moreover, the board considers that the skilled person is capable of determining "an amount dependent on a number of predicate flags" by which to change the value

of the counter variable: For instance, in the example depicted in figure 5 and assuming the number of predicate flags to be identical to the number of execution lanes, this number would, in all but the last iteration, be identical to the number of available predicate flags. And it should never be larger than the number of available predicate flags. Generally, many different amounts are possible within the scope of the claim, but choosing one or the other poses no problem for the person skilled in the art. It is true that not all "amounts" chosen will produce WHILE and CHANGE instructions which allow the coding of a processing loop as intended, but as the processing loop itself is not a feature of the claim, this is not a deficiency under Article 83 EPC but a matter of breadth to be addressed under inventive step (see also G1/03, point 2.5.2).

The board therefore holds that the requirements of Article 83 EPC have been satisfied.

5. *Inventive step; Article 56 EPC*

The board does not consider it appropriate that it would be the first instance deciding on the matter of inventive step in the present case. It therefore remits the case to the examining division (Article 11 RPBA), in order for the division to take a decision on that matter.

The board notes in this regard that the International Search Report cites a number of prior art documents as being particularly relevant. In the related application 15 386 025.9 (mentioned in the present case in the communication dated 27 January 2020), the same

documents were cited in the Search Report and further ones were introduced later in examination.

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the examining division for further prosecution.

The Registrar: The Chairman:

L. Stridde M. Müller

Decision electronically authenticated