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Datasheet for the decision of 30 May 2023

Case Number: T 0048/21 - 3.5.07

Application Number: 14764967.7

Publication Number: 2959400

IPC: G06F15/173

Language of the proceedings: EN

Title of invention:
Disaggregated network architecture for data centers

Applicant:
Huawei Technologies Co., Ltd.

Headword:
Disaggregated network architecture/HUAWEI

Relevant legal provisions:
EPC Art. 56
RPBA 2020 Art. 13(2)

Keyword:
Inventive step - main request and first and second auxiliary requests (no)
Amendment after summons - exceptional circumstances (no) - third to eighth auxiliary requests

Decisions cited:
T 0003/90

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Case Number: T 0048/21 - 3.5.07

D E C I S I O N
of Technical Board of Appeal 3.5.07
of 30 May 2023

Appellant: (Applicant)	Huawei Technologies Co., Ltd. Huawei Administration Building Bantian Longgang District Shenzhen, Guangdong 518129 (CN)
Representative:	Epping - Hermann - Fischer Patentanwaltsgesellschaft mbH Schloßschmidstraße 5 80639 München (DE)
Decision under appeal:	**Decision of the Examining Division of the European Patent Office posted on 15 July 2020 refusing European patent application No. 14764967.7 pursuant to Article 97(2) EPC**

Composition of the Board:

Chair	J. Geschwind
Members:	R. de Man
	C. Barel-Faucheux

Summary of Facts and Submissions

I. The appellant (applicant) filed an appeal against the decision of the examining division refusing European patent application No. 14764967.7.

II. The contested decision cited, *inter alia*, the following documents:

D1: US 8 041 875 B1, 18 October 2011;
D2: US 2006/0221832 A1, 5 October 2006.

The examining division decided that the subject-matter of claim 1 of the main request and of the auxiliary request lacked inventive step over document D1. It referred to document D2 as evidence of common general knowledge.

III. With its statement of grounds of appeal, the appellant maintained its main request and its auxiliary request and filed a further, second auxiliary request.

IV. In a communication accompanying the summons to oral proceedings, the board expressed the preliminary opinion that the subject-matter of claim 1 of the main request and of the first and second auxiliary requests lacked an inventive step.

V. With a letter dated 15 February 2023, the appellant maintained its main request and first and second auxiliary request and filed new third to eighth auxiliary requests.

VI. In a subsequent letter, the appellant informed the board that it would not attend the oral proceedings. The board then cancelled the oral proceedings.

VII. The appellant requests that the decision under appeal be set aside and that a patent be granted on the basis of the claims of the main request or, in the alternative, of one of the first to eighth auxiliary requests.

VIII. Claim 1 of the main request reads as follows:

"A system comprising:

an interconnect network (270);

a plurality of process memory modules (250);

a plurality of processor modules (210) configured to share access to the memory modules (250) via the interconnect network (270), wherein each processor module (210) is positioned in a separate network element from each memory module (250); and

a plurality of process acceleration modules (260), wherein the plurality of processor modules (210) are further configured to share access to the process acceleration modules (260) via the interconnect network (270)."

IX. Claim 1 of the first auxiliary request reads as follows:

"A data center comprising:

an interconnect network (270);

a plurality of process memory modules (250);

a plurality of processor modules (210) configured to share access to the memory modules (250) via the interconnect network (270), wherein each processor

module (210) is positioned in a separate network element from each memory module (250);

a plurality of process acceleration modules (260), wherein the plurality of processor modules (210) are further configured to share access to the process acceleration modules (260) via the interconnect network (270);

a plurality of data storage modules (220) configured for data storage, wherein the plurality of processor modules (210) are further configured to share access to the storage modules (220) via the interconnect network (270); and

a plurality of network interface controller modules (230) configured for core network connectivity, wherein the plurality of processor modules (210) are further configured to share access to the network interface controller modules (230) via the interconnect network (270), wherein each processor module (210) is positioned in a separate network element from each storage module (220), network interface controller module (230), and process acceleration module (260)."

X. Claim 1 of the second auxiliary request is identical to claim 1 of the first auxiliary request.

XI. Claim 1 of the third auxiliary request reads as follows:

"A system comprising:

an interconnect network (270);

a plurality of process memory modules (250), wherein each process memory module (250) consists of Random Access Memory, RAM;

a plurality of processor modules (210) configured to share access to the process memory modules (250) via the interconnect network (270), wherein each processor

module (210) consists of a single processor or a processor cluster and is positioned in a separate network element from each process memory module (250); and

a plurality of process acceleration modules (260), wherein the plurality of processor modules (210) are further configured to share access to the process acceleration modules (260) via the interconnect network (270)."

XII. Claim 1 of the fourth auxiliary request differs from claim 1 of the third auxiliary request in that:

- the text ", positioned in a blade server" has been inserted after "RAM"; and
- the text "is positioned in a separate network element from" has been replaced with "is positioned in a blade server separate from".

XIII. Claim 1 of the fifth auxiliary request reads as follows:

"A data center comprising:

an interconnect network (270);

a plurality of process memory modules (250), wherein each process memory module (250) consists of Random Access Memory, RAM;

a plurality of processor modules (210) configured to share access to the process memory modules (250) via the interconnect network (270), wherein each processor module (210) consists of a single processor or a processor cluster and is positioned in a separate network element from each process memory module (250);

a plurality of process acceleration modules (260), wherein the plurality of processor modules (210) are further configured to share access to the process

acceleration modules (260) via the interconnect network (270);

a plurality of data storage modules (220) configured for data storage, wherein each data storage module (220) consist of disk drives, solid state drives or a redundant array of independent disks, RAID, and the plurality of processor modules (210) are further configured to share access to the data storage modules (220) via the interconnect network (270); and

a plurality of network interface controller modules (230) configured for core network connectivity, wherein the plurality of processor modules (210) are further configured to share access to the network interface controller modules (230) via the interconnect network (270), wherein each processor module (210) is positioned in a separate network element from each data storage module (220), network interface controller module (230), and process acceleration module (260)."

XIV. Claim 1 of the sixth auxiliary request differs from claim 1 of the fifth auxiliary request in that:

- the text ", positioned in a blade server" has been inserted after "RAM";
- the text "positioned in a blade server" has been inserted after "RAID,"; and
- the two instances of "is positioned in a separate network element from" have been replaced with "is positioned in a blade server separate from".

XV. Claim 1 of the seventh auxiliary request is identical to claim 1 of the fifth auxiliary request.

XVI. Claim 1 of the eighth auxiliary request is identical to claim 1 of the sixth auxiliary request.

XVII. The appellant's arguments, where relevant to the decision, are discussed in detail below.

Reasons for the Decision

1. It is well established in the case law of the boards of appeal that the appellant's statement that it would not take part in the oral proceedings is to be understood as a withdrawal of its request for oral proceedings in the absence of any indication to the contrary (see decision T 3/90, OJ EPO 1992, 737, Reasons 1, and Case Law of the Boards of Appeal, 10th edition, 2022, III.C. 4.3.2). The decision can therefore be taken without holding oral proceedings.

2. The application relates to a network architecture for data centers.

Main request

3. *The invention as defined by claim 1*

3.1 Claim 1 is directed to a system comprising an interconnect network, a plurality of "process memory modules", a plurality of "processor modules", and a plurality of "process acceleration modules".

3.2 The processor modules are configured to share access to the memory modules and to the process acceleration modules via the interconnect network.

3.3 Each processor module is positioned in a separate network element from each memory module.

4. *Inventive step*

4.1 Document D1 relates to providing resources such as peripheral interfaces and peripheral components in a virtualised, shared and redundant manner to multiple servers connected over an I/O bus interface (see column 1, lines 19 to 24).

It discloses an interconnect network comprising three servers 201, 211 and 221 and a plurality of process acceleration modules 257 and 259 (see Figure 2A; column 6, lines 22 to 28 and 43 to 52). Each server includes a processor and a memory (column 6, lines 24 to 26). The interconnect network may be based on the PCI Express bus architecture (column 6, lines 55 to 57).

The I/O bus interconnect allows aggregation of the memory address spaces of the servers into an aggregated memory address space (Figure 4; column 9, lines 3 to 27). The processors also share access to the process acceleration modules via the interconnect network (column 7, lines 1 to 11).

4.2 The servers of document D1, which include both a processor and a memory, are "processor modules" within the meaning of claim 1. Indeed, paragraph [0023] of the present application confirms that processor modules may include a memory in addition to a processor, and Figure 2 of the application shows an embodiment of the invention in which each processor module 210 includes both a processor 215 and a memory 217.

4.3 The system of claim 1 differs from the disclosure of document D1 in that it additionally includes a

plurality of "memory modules" positioned in network elements separate from the "processor modules".

4.4 In one line of reasoning developed in its communication, the board argued that a server of document D1, which shares its memory with other servers, is also a "memory module" within the meaning of claim 1 and that adding a fourth server 231 to the interconnect network of document D1 would result in a system as claimed, comprising a plurality of two processor modules and a plurality of two memory modules, each processor module being positioned in a separate network element from each memory module.

The appellant presented a number of arguments in an attempt to refute this line of reasoning. Although the board is not necessarily convinced by these counterarguments, it will now focus on its alternative line of reasoning, which - in line with the appellant's and the examining division's interpretation of claim 1 - assumes that the memory modules are positioned in network elements which do not contain any processor.

4.5 The purpose of the PCI Express interconnect network of the system of document D1 is to allow PCI Express devices to be added to the network and to virtualise and share them with the servers.

Document D2 discloses a PCI Express bus 112 connecting processing elements 120 to a memory system 130 (Figure 1 and paragraphs [0047] to [0049]). The memory system 130 is in a separate network element from the processing elements and is therefore a "memory module" within the meaning of claim 1.

The board is unable to see any inventive merit in adding, to the PCI Express interconnect network of document D1, memory modules which were available at the priority date and which were designed to be connected to a PCI Express interconnect network, i.e. in using those modules for their intended purpose. Such a modification of the system of document D1 provides only the expected advantages (and disadvantages) of such modules and of the interconnect network.

4.6 The appellant argued that the distinguishing feature ensures a flexible and cost-efficient operation by allowing for "replacements at pool level instead of at server level within the data center"

However, the fact that adding a separate memory module network element to an interconnect network means that this separate element can be separately replaced if it breaks down is an expected advantage of separate memory module network elements and is also present in document D2.

4.7 The appellant further argued that adding the memory modules of document D2 to the system of document D1 would not lead to a system satisfying the feature "each processor module is positioned in a separate network element from each memory module", because each server network element of document D1 included both a processor and a memory. Document D1 provided no motivation to separate processor and memory within the servers, and such a separation would go against the very essence of document D1.

However, in the present application the processor modules may also include both a processor and a memory (see point 4.2 above). The claim does not require that

the processor modules themselves do not contain any memory, and it is therefore not necessary to remove the server memory from the servers to arrive at the claimed invention.

4.8 Hence, the subject-matter of claim 1 of the main request lacks an inventive step (Articles 52(1) and 56 EPC).

First auxiliary request

5. Claim 1 of the first auxiliary request adds to claim 1 of the main request the following features:
- the system is a "data center";
- the system comprises a plurality of data storage modules configured for data storage;
- the system comprises a plurality of network interface controller modules configured for core network connectivity;
- the plurality of processor modules are also configured to share access to the data storage modules and the network interface controller modules via the interconnect network;
- each processor module is "positioned in a separate network element from each storage module, network interface controller module, and process acceleration module".

6. *Inventive step*

6.1 Document D1 discloses that the virtualisation switch can be implemented in a system such as a data center (column 8, lines 10 to 12).

The system of document D1 comprises data storage modules and network interface controller modules

(Figure 2A; column 6, lines 43 to 48, "Internet SCSI (iSCSI)/.../Serial ATA (SATA) 251" and "NIC 255", cf. column 1, lines 31 to 33). Since they are virtualised, the processor modules are configured to share access to these modules via the interconnect network (column 6, lines 48 to 52).

The processor modules are positioned in servers 201, 211 and 221, which are separate from each network interface controller module and process acceleration module at the resource virtualisation switch 243 (Figure 2A).

6.2 In its statement of grounds of appeal, the appellant argued that document D1 did not disclose that the actual storage resources behind the peripheral interfaces such as SATA were positioned in a network interface separate from the processor modules. The appellant pointed out that document D1, in column 5, lines 11 and 12, stated that storage resources including local disks could be shared and virtualised.

The board agrees that the iSCSI and SATA interfaces which are part of the virtual switch 243 are not themselves data storage modules, and that the actual data storage modules may be local disks which are part of the servers.

However, the data storage modules may as well be well-known network drives which are separate from the servers. In fact, the statement in column 5, lines 11 to 13, that "[s]torage resources including local disks can be shared and virtualized to allow stateless computing" clearly leaves open the possibility that the shared and virtualised storage resources also include

non-local disks such as network drives, and the board therefore considers this to be an obvious possibility.

6.3 Hence, the features added to claim 1 of the first auxiliary request do not overcome the board's objection of lack of inventive step over document D1 raised for the main request (Articles 52(1) and 56 EPC).

Second auxiliary request

7. The second auxiliary request was filed with the statement of grounds of appeal.

Since its claim 1 is identical to claim 1 of the first auxiliary request, it follows from point 6. above that the subject-matter of claim 1 of the second auxiliary request lacks an inventive step (Articles 52(1) and 56 EPC).

In these circumstances, it is not in the interest of procedural efficiency to consider whether the second auxiliary request should be refused admission into the proceedings under Article 12(4) RPBA 2020. The request is therefore admitted.

Third to eighth auxiliary requests

8. *Admission into the appeal proceedings*

8.1 The third to eighth auxiliary requests were filed after the notification of the board's summons to oral proceedings. Under Article 13(2) RPBA 2020, such requests are, in principle, not be taken into account unless there are exceptional circumstances, which have been justified with cogent reasons.

8.2 The appellant argued that the board's inventive step reasoning as presented in its communication, including the board's interpretation of the claims, differed from that in the contested decision. This new reasoning contained elements which could not have been foreseen by the appellant and thus could not have been addressed by filing amendments at an earlier stage of the proceedings. This exceptional circumstance justified the admission under Article 13(2) RPBA 2020 of the third to eighth auxiliary requests, which clarified the functionality of the individual modules and their physical arrangement separate from each other and ruled out any interpretation where the individual modules contained additional resources.

8.3 The board accepts that one line of reasoning presented in its communication contained new elements which the appellant reasonably could not have anticipated and which therefore would have justified the admission of amendments appropriately addressing them if the board had maintained that line of reasoning. However, the board has not relied on this line of reasoning when deciding on the main request and the first and second auxiliary requests (see point 4.4 above). Instead, the board has essentially confirmed the inventive-step objection based on a combination of documents D1 and D2 raised in the decision under appeal. Although its reasoning is not identical to that of the examining division, in the board's view it does not contain any elements which the appellant could not have foreseen. In particular, while the board's reasoning does rely on claim 1 of the main request and the first and second auxiliary requests not ruling out that a processor module may include a memory, this interpretation of the claims is plainly in line with the definition of a "processor module" in paragraph [0023] of the present

application and with the embodiment of the invention shown in Figure 2 (see point 4.2 above), so that it could not reasonably have surprised the appellant.

8.4 Hence, the board does not consider that there are exceptional circumstances within the meaning of Article 13(2) RPBA 2020 and therefore does not admit the third to eighth auxiliary requests into the appeal proceedings.

9. Since none of the requests admitted into the proceedings is allowable, the appeal is to be dismissed.

Order

For these reasons it is decided that:

The appeal is dismissed.

The Registrar: The Chair:

S. Lichtenvort J. Geschwind

Decision electronically authenticated