

**Internal distribution code:**

- (A) [ - ] Publication in OJ
- (B) [ - ] To Chairmen and Members
- (C) [ - ] To Chairmen
- (D) [ X ] No distribution

**Datasheet for the decision  
of 12 September 2022**

**Case Number:** T 0964/20 - 3.5.05

**Application Number:** 14767183.8

**Publication Number:** 3044687

**IPC:** G06F13/38

**Language of the proceedings:** EN

**Title of invention:**

ASCERTAINING COMMAND COMPLETION IN FLASH MEMORIES

**Applicant:**

Qualcomm Incorporated

**Headword:**

ASCERTAINING COMMAND COMPLETION IN FLASH MEMORIES / Qualcomm

**Relevant legal provisions:**

EPC Art. 56, 123(2)  
RPBA 2020 Art. 13(1)

**Keyword:**

Inventive step - effect not made credible within the whole scope of claim

**Decisions cited:**

T 2764/19



**Beschwerdekammern**  
**Boards of Appeal**  
**Chambres de recours**

Boards of Appeal of the  
European Patent Office  
Richard-Reitzner-Allee 8  
85540 Haar  
GERMANY  
Tel. +49 (0)89 2399-0  
Fax +49 (0)89 2399-4465

Case Number: T 0964/20 - 3.5.05

**D E C I S I O N**  
**of Technical Board of Appeal 3.5.05**  
**of 12 September 2022**

**Appellant:** Qualcomm Incorporated  
(Applicant) 5775 Morehouse Drive  
San Diego, CA 92121-1714 (US)

**Representative:** Carstens, Dirk Wilhelm  
Wagner & Geyer Partnerschaft mbB  
Patent- und Rechtsanwälte  
Gewürzmühlstraße 5  
80538 München (DE)

**Decision under appeal:** **Decision of the Examining Division of the  
European Patent Office posted on 5 December 2019  
refusing European patent application No.  
14767183.8 pursuant to Article 97(2) EPC.**

**Composition of the Board:**

**Chairman** E. Konak  
**Members:** N. H. Uhlmann  
F. Blumer

## **Summary of Facts and Submissions**

- I. The applicant appealed against the examining division's decision to refuse the European patent application in suit.
- II. The examining division decided that the main request and the auxiliary request did not meet the requirements of Article 56 EPC and that the auxiliary request additionally did not comply with the provisions of Article 84 EPC.
- III. The examining division made reference, *inter alia*, to the following documents:  
  
D1 US 6 587 893  
D2 US 2006/235999
- IV. With the statement setting out the grounds of appeal the appellant resubmitted the two requests on which the contested decision had been based.
- V. The board summoned the appellant to oral proceedings.  
  
In a communication under Article 15(1) RPBA 2020, the board set out its provisional opinion on the case.
- VI. With a letter dated 11 August 2022, the appellant submitted an amended main request and amended auxiliary requests 1 to 3.
- VII. The oral proceedings took place by videoconference.
- VIII. The appellant requested that the decision under appeal be set aside and that a patent be granted on the basis of the main request or on the basis of any one of auxiliary requests 1 to 3, all requests as filed with the letter dated 11 August 2022.

IX. Claim 1 of the main request is worded as follows:

"A universal flash storage, UFS, system comprising:

a control system (16, 20) comprising a host controller (16) and a host software (20), wherein the host controller (16) is configured to interoperate with the host software (20);

a doorbell register (30) having a number of bits equal to a number of transfer request slots handled by the host controller (16);

a completion notification register (32) having a same number of bits; and

the control system (16, 20) operatively coupled to the doorbell register (30) and the completion notification register (32) and configured to:

set a doorbell bit in the doorbell register (30) for a send request start;

issue a transfer request to a device (12), wherein the send request start is associated with the transfer request;

set a completion bit in the completion notification register (32) on transfer request completion; and

clear the doorbell bit on the transfer request completion."

X. Claim 1 of auxiliary request 1 is based on claim 1 of the main request. The wording "wherein said setting of the completion bit is for indicating a completion of the transfer request" has been added to claim 1.

XI. Claim 1 of auxiliary request 2 is based on claim 1 of the main request. The wording "clear the completion bit after processing completion of the transfer request" has been added to claim 1.

XII. Claim 1 of auxiliary request 3 is based on claim 1 of auxiliary request 1. The wording "clear the completion bit after processing completion of the transfer request" has been added to claim 1.

### **Reasons for the Decision**

1. The application in hand pertains to a flash storage system comprising a doorbell register and a completion notification register having the same number of bits. The bits in the registers are set and cleared in the course of transfer request processing.
2. Document D1 discloses a method for processing requests to memory using an in-progress register.

### **Main request**

3. Inventive step
  - 3.1 Document D1 forms a suitable starting point for the problem-solution analysis.
  - 3.2 Distinguishing features

The appellant argued that D1 additionally did not disclose that the doorbell register has a number of bits equal to a number of transfer request slots.

The board is not convinced. The in-progress register in D1 anticipates the claimed doorbell register. According to the embodiment described in column 3, lines 31 to 38, there is a single bit in the in-progress register for each cache line. The "single bit for each cache line" qualifies as the "equal number" as per claim 1. Furthermore, the requests and responses are tracked by matching them with the cache line. Hence, the number of requests/responses corresponds to the number of cache lines.

Consequently, the board confirms the distinguishing features as set out in the decision under appeal, namely:

A: the storage system is a UFS system

B: completion notification register having a same number of bits, wherein a completion bit is set in the completion notification register on transfer request completion

3.3 The examining division found that these features solved unrelated, partial problems and that feature A did not contribute towards inventive step. The appellant did not object to these findings.

3.4 Regarding feature B, the following is noted.

3.4.1 The introduction of the completion notification register and the setting of a completion bit in it does not lead to any effect because the values of the bits in this register (and in the doorbell register) do not play any role in the system as claimed. Hence, distinguishing feature B amounts to an arbitrary, non-functional modification of the prior art. According to the established case law, any such arbitrary modification is to be disregarded in the assessment of inventive step (see the Case Law of the Boards of Appeal, 10th edition 2022, chapter I.D.9.6; see also T 2764/19, Reasons 3.3.3).

3.4.2 The appellant argued that the distinguishing features led to the effect of avoiding software locks, thus improving the operating efficiency. Furthermore, software interrupts could occur at any time.

The board disagrees. The observation in point 3.4.1 notwithstanding, an interrupt occurring between the setting of the completion bit and the clearing of the doorbell bit (the last two steps in claim 1) may lead

to race conditions related to those described in paragraphs 28 and 29 of the description of the application. Furthermore, race conditions are not avoided because the last two steps in claim 1 are performed by the control system, which also comprises host software, so these steps do not necessarily take place at the same point in time. Race conditions were, in principle, to be prevented through the use of software locks.

For the same reasons, feature B does not allow for a hardware solution instead of a software lock solution.

- 3.4.3 The appellant suggested that the problem solved by difference B was "to provide an alternative completion notification".

However, as explained in point 3.4.1 above, feature B does not lead to any technical effect, so it cannot solve any technical problem.

- 3.4.4 The appellant submitted that the technical effect was "to provide means for indicating transfer request completion".

The board holds that any such effect cannot be caused by feature B because the request completion is also indicated by clearing a bit in the doorbell register (last step in claim 1), which is disclosed in D1.

- 3.4.5 The appellant explained that decision T 2764/19 referred to different subject-matter, meaning that it was not applicable.

The board notes that while the specific factual situation in the case underlying decision T 2764/19 is different, the same general principle regarding arbitrary modifications applies.

3.4.6 The appellant argued that according to claim 1, the completion bit was set and the doorbell bit was cleared at the same point in time, i.e. "on transfer request completion". Consequently, no interrupt could occur between the setting of a bit and the clearing of another bit.

This argument is not convincing. According to Figure 5 and paragraph 34 of the description, the "transfer request completion" is a process comprising a plurality of steps 120 to 138. Hence, the wording "on transfer request completion" does not define a single point in time. Furthermore, Figure 5 and paragraph 34 clearly relate to these setting and clearing steps.

3.4.7 The formulation "at the same time" in paragraph 20 of the description is in the context of the bits being set and cleared by the controller of the host - a hardware component. By contrast, claim 1 states that a control system performs these steps. The control system comprises the host controller and host software. Hence, this formulation does not support the appellant's arguments. Moreover, features which are not mentioned in claim 1 cannot contribute to any inventive step.

3.4.8 The appellant argued that there was, at most, a short period of time between the setting and clearing step in claim 1. The probability of a race condition was thus much smaller than in document D1, constituting an improvement over D1.

The board notes that D1 does not disclose any race conditions or software locks. Consequently, no such improvement can be recognised.

3.5 For these reasons, the subject-matter of claim 1 does not involve an inventive step and the main request is not allowable.



### **Auxiliary requests 1 and 3**

#### 4. Admission

4.1 These auxiliary requests were submitted after the summons to oral proceedings had been issued. Hence, their admission is governed by the provisions of Article 13(1) and (2) RPBA 2020.

4.2 The following wording has been added to claim 1 of these requests:

"wherein said setting of the completion bit is for indicating a completion of the transfer request."

4.3 According to the appellant, this amendment was based on paragraph 34 of the description, in particular the following sentences:

"Initially, the hardware clears the doorbell register 30 and sets the command completion register 32 (block 122). An interrupt occurs (block 124). The host software 20 reads the command completion register 32 (block 126) to ascertain what tasks are completed."

4.4 The board holds that according to this passage, the purpose of the completion bit is disclosed in the context of the host software's reading of the command completion register. There is no basis in the application as filed to define the purpose of setting the completion bit.

4.5 Hence, this amendment does not meet the requirements of Article 123(2) EPC.

4.6 For these reasons, the board decided that since auxiliary requests 1 and 3 gave rise to a new objection, they did not meet the criteria set out in Article 13(1) RPBA. Thus, auxiliary requests 1 and 3 were not admitted into the proceedings.

## **Auxiliary request 2**

5. Inventive step

5.1 The following step has been added to claim 1:

"clear the completion bit after processing completion of the transfer request"

5.2 The appellant argued that the technical effect of this step was that the bit in the completion register was reset to its initial state and thus could be reused for new transfer requests.

The board does not accept that this effect is achieved. As explained above with regard to the main request, the values (whether set or cleared) of the bits in the completion register do not play any role in the system as claimed.

5.3 Thus, the additional step of clearing the completion bit does not lead to any effect for the reasons given above with regard to the main request.

5.4 For these reasons, the subject-matter of claim 1 does not involve an inventive step.

6. Conclusion

None of the appellant's admissible requests is allowable.

**Order**

**For these reasons it is decided that:**

The appeal is dismissed.

The Registrar:

The Chairman:



K. Götz-Wein

E. Konak

Decision electronically authenticated