Internal distribution code:

(A) [-] Publication in OJ
(B) [-] To Chairmen and Members
(C) [-] To Chairmen
(D) [X] No distribution

Datasheet for the decision of 21 April 2021

Case Number: T 2481/19 - 3.5.07

Application Number: 03026868.4

Publication Number: 1422830

IPC: H03M13/29

Language of the proceedings: EN

Title of invention:
Method and apparatus for controlling turbo decoder input

Applicant:
Samsung Electronics Co., Ltd.

Headword:
Controlling turbo decoder input/SAMSUNG

Relevant legal provisions:
EPC Art. 56, 84, 123(2)

Keyword:
Inventive step - (yes)
Claims - clarity after amendment (yes)
Amendments - after amendment - added subject-matter (no)

Decisions cited:
T 0823/11, T 1066/13, T 2707/16, T 2377/17

Europäisches Patentamt
European Patent Office
Office européen des brevets

Beschwerdekammern

Boards of Appeal

Chambres de recours

Boards of Appeal of the
European Patent Office
Richard-Reitzner-Allee 8
85540 Haar
GERMANY
Tel. +49 (0)89 2399-0
Fax +49 (0)89 2399-4465

Case Number: T 2481/19 - 3.5.07

D E C I S I O N
of Technical Board of Appeal 3.5.07
of 21 April 2021

Appellant: (Applicant)	Samsung Electronics Co., Ltd. 129, Samsung-ro Yeongtong-gu Suwon-si, Gyeonggi-do, 443-742 (KR)
Representative:	Nederlandsch Octrooibureau P.O. Box 29720 2502 LS The Hague (NL)
Decision under appeal:	**Decision of the Examining Division of the European Patent Office posted on 6 February 2019 refusing European patent application No. 03026868.4 pursuant to Article 97(2) EPC**

Composition of the Board:

Chairman	J. Geschwind
Members:	P. San-Bento Furtado
	C. Barel-Faucheux

Summary of Facts and Submissions

I. The appeal lies from the decision of the examining division to refuse European patent application No. 03026868.4 on the grounds that the subject-matter of claim 1 of a main request and of first and second auxiliary requests lacked inventive step in view of a prior-art document D1, cited as "'1x EV-DV Forward Link Overview', XP002303828" on page 4 of the decision.

II. In the section "Summary of Facts and Submissions", the decision under appeal cites several documents on pages 1 and 2, including the following documents D1 and D9:

D1: WO 02/21715 A, published on 14 March 2002;

D9: "1x EV-DV Forward Link Overview", internet citation, 16 November 2001, XP002247591.

III. With the statement of grounds of appeal, the appellant requested that the decision under appeal be set aside. It also filed an amended set of claims and argued that the submitted claims were allowable.

IV. The appellant was invited to oral proceedings. In a subsequent communication, the board informed the appellant that in spite of the conflicting indications in the decision under appeal regarding documents D1 and D9 and the closest prior art, the board had been able to establish that the closest prior art document D1 was the same as document D9 and corresponded to the document retrieved from the following URL:
https://www.3gpp.org/ftp/tsg_ran/TSG_RAN/TSGR_AHs/2001_11_3GPP2_HSDPA_Harmonisation/Docs/RPA010004.pdf.

A copy of the document, which the board referred to as "document D9", was annexed to the board's communication.

The board expressed the preliminary opinion that independent claims 1 and 8 did not fulfil the requirements of Article 84 EPC and that claims 4 to 7 and 11 to 14 did not satisfy the requirements of Articles 84 and 123(2) EPC. The subject-matter of independent claims 1 and 8 seemed to be inventive over the prior art cited in the application.

V. With a letter of reply dated 16 February 2021, the appellant filed new claims 1 to 6.

VI. In a telephone conversation on 19 April 2021, the representative was informed that the amendments made had overcome the objections raised by the board in its preliminary opinion but that minor corrections to the independent claims were still necessary. The appellant was further informed that the board had identified deficiencies in the examination proceedings and in the decision under appeal with regard to the use of documents D1 and D9 and the length of the proceedings and might deal with these issues in the final decision.

VII. With a letter of 20 April 2021, the appellant filed amended claims 1 to 6. Oral proceedings were cancelled.

VIII. The appellant's final request was that the contested decision be set aside and that a patent be granted on the basis of claims 1 to 6 filed with the letter of 20 April 2021.

IX. Claim 1 reads as follows (itemisation added by the board):

(a) "A method of receiving code symbols corresponding to an interleaved encoder packet, EP, storing the systematic code symbols, first parity code symbols and second parity code symbols in first, second and third memories respectively in an interleaved order, and inputting the stored code symbols to a turbo decoder in a mobile communication system, the method comprising the steps of:

(b) receiving (S200), by a receiver of the mobile communication system, the size of the EP;

(c) generating (S400), by the receiver, read addresses so that the code symbols at the read addresses are in a deinterleaved order corresponding to the interleaving; and

(d) reading (S500), by the receiver, the code symbols at the read addresses from the memories and outputting the read code symbols to the turbo decoder,

(e) wherein in the mobile communication system a transmitter encodes the encoder packet EP including information bits and tail bits at a predetermined code rate and subblock-interleaves code symbols of a plurality of encoded subblocks prior to transmission, and

(f) the turbo decoder has two sequentially operating constituent decoders, the method further comprises the step of:

(g) generating (S460), by the receiver, chip select signals for the memories in synchronization to a decoder clock signal; and

(h) wherein the code symbols are provided to the two constituent decoders according to the read addresses and the chip select signals;

(i) wherein the step of generating the read addresses and the chip select signals comprises the steps of:

(j) setting (420) symbol type signal DT_IDC to 0 when a data symbol corresponding to an information bit is output to the turbo decoder and setting (S415) DT_IDC to 1 when a tail symbol corresponding to a tail bit is output to the turbo decoder, each time the decoder clock signal is triggered;

(k) generating (S445) a temporary address, TMP_ADDR indicating the interleaved position of a code symbol to be output to the turbo decoder in a subblock that the code symbol belongs to;

(l) generating (S450) the read addresses using TMP_ADDR, the EP size, and a memory select signal RAM_SEL, wherein the RAM_SEL is 0 only when data symbols are read for the first constituent decoder, wherein the RAM_SEL is produced by OR-operating DT_IDC and DEC_IDX, wherein the DEC_IDX set to 0 identifies the first constituent decoder; and

(m) generating (S460) the chip select signals for the first, second and third memories, wherein the chip select signals are generated using RAM_SEL, TMP_ADDR, the EP size, and temporary chip select signal TMP_CS, wherein the TMP_CS is produced by OR-operating DT_IDC and the inverse of DEC_IDX."

X. Dependent claim 2 reads as follows:

"The method of claim 1, wherein when the EP size is one of 408, 792 and 1560, the read addresses RAM0_ADDR, RAM1_ADDR and RAM2_ADDR for the first, second and third memories are determined by

if RAM_SEL=0

RAM0_ADDR=TMP_ADDR

RAM1_ADDR=2xTMP_ADDR

RAM2_ADDR=2xTMP_ADDR

else
RAM0_ADDR=TMP_ADDR
RAM1_ADDR=2xTMP_ADDR+1
RAM2_ADDR=2xTMP_ADDR+1."

Dependent claim 3 reads as follows:
"The method of claim 2, wherein the chip select signal RAM0_CS for the first memory is TMP_CS and the chip select signals RAM1_CS and RAM2_CS for the second and third memories are 1."

XI. Independent claim 4 reads as follows:
"An apparatus for receiving code symbols corresponding to an interleaved encoder packet EP, storing the systematic code symbols, first parity code symbols and second parity code symbols in first, second and third memories respectively in an interleaved order, and inputting the stored code symbols to a turbo decoder having two sequentially operating constituent decoders in a mobile communication system, the apparatus comprising:

a memory unit (200) having the first, second and third memories (210,220,230), for storing the received code symbols separately as information symbols and parity symbols; and

a read address generator (100) for generating read addresses to read the code symbols from the first, second and third memories so that the code symbols at the read addresses are in a deinterleaved order corresponding to the interleaving,

wherein the read address generator comprises:

means for generating the memory select signal RAM_SEL based on a decoder index DEC_IDX identifying a first constituent decoder of the turbo decoder in the current operation and a symbol type signal DT_IDC indicating whether the type of the code symbol is a

data symbol or a tail symbol according to the EP size, wherein the memory select signal RAM_SEL indicates whether data symbols are read for the first constituent decoder;

means for generating a temporary read address TMP ADDR indicating the interleaved position of the code symbol to be read in a subblock to which the code symbol belongs;

means for generating a temporary chip select signal TMP_CS using DT_IDC and DEC_IDX;

an input address generator (125) for generating the read addresses using RAM_SEL, TMP ADDR, and the EP size; and

a chip select signal generator (150) for generating chip select signals for the memories using RAM_SEL, TMP_CS, TMP ADDR, and the EP size."

XII. Dependent claims 5 and 6 specify further features of the apparatus in equivalent terms to those of dependent claims 2 and 3, respectively.

Reasons for the Decision

Application

1. The invention concerns a method and an apparatus for receiving code symbols of an interleaved encoder packet EP and inputting them to a turbo decoder in a mobile communication system according to the standard 1xEV-DV (see the application as filed, page 6, lines 17 to 22).

1.1 The interleaved encoder packet EP is generated at the transmitter, which includes a turbo encoder and a channel interleaver. The turbo encoder encodes an input data stream using two encoders ENC1 and ENC2 and outputs code symbols including input information bits

and corresponding tail bits (page 6, line 26, to page 7, line 25; page 9, lines 18 to 30; Figures 1 and 4).

This gives rise to five sub-blocks S, P0, P1, P'0 and P'1 of symbols as illustrated in Figures 4 and 5 of the application, where S contains the systematic code symbols, P0 and P1 contain the first and second parity bits of ENC1, respectively, and P'0 and P'1 the first and second parity bits of ENC2. In this example, each sub-block also includes four tail bits (page 10, line 18, to page 12, line 12).

1.2 As illustrated in Figure 5, the channel interleaver permutes the order of the code symbols by classifying the code symbols received from the turbo encoder into the sub-blocks (symbol separation), interleaving the respective sub-blocks according to the same interleaving rule (sub-block interleaving) and alternately arranging the interleaved symbols of the sub-blocks (sub-block symbol grouping) (page 6, line 24, to page 7, line 25; page 10, line 18, to page 12, line 6; Figures 1 and 5). In accordance with the 1xEV-DV standard, different EP sizes are available, for example 408, 792 and 1560 bits, including six tail bits (page 7, lines 8 to 12; page 13, line 19, to page 14, line 1; Figure 7).

1.3 At the receiver, the code symbols are stored in a buffer, in the form of the interleaved groups, prior to decoding by two constituent decoders. Channels are de-interleaved when the code symbols are read from the decoder input buffer (page 12, lines 8 to 12; page 13, lines 12 to 17). The buffer is composed of three memories for storing the three types of code symbols SYS, PA0 and PA1 and providing them in parallel to the constituent decoders (page 14, lines 3 to 6).

As shown in Figure 8, the decoder input buffer comprises random access memories RAM0, RAM1 and RAM2 for storing the code symbols of the sub-blocks S, P0/P'0 and P1/P'1. Sub-block S is stored in RAM0. For EP sizes of 408, 792 and 1560, sub-blocks P0/P'0 and P1/P'1 are stored in RAM1 and RAM2, respectively (page 14, lines 8 to 22; Figure 8; page 15, lines 18 to 21).

1.4 In order to provide the code symbols in de-interleaved and ungrouped order from the buffer memories, a read address generator (RAG) 100 outputs three read addresses for the three RAMs in response to signals received from the turbo decoder (see Figure 9 reproduced above). The memory unit composed of the three RAMs outputs three code symbols at the read addresses to the turbo decoder (page 14, line 27, to page 15, line 30; Figure 9). A block diagram of the RAG 100 is illustrated in Figure 12 reproduced below.

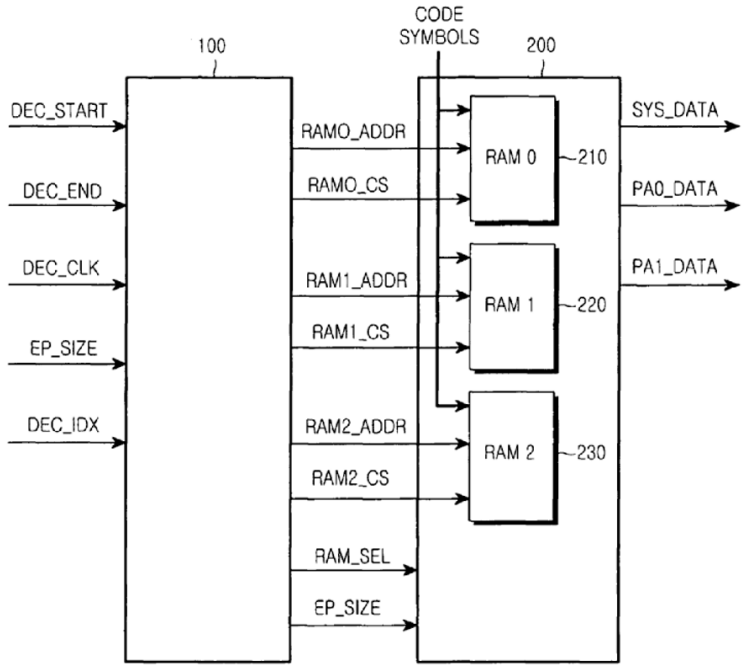

FIG.9

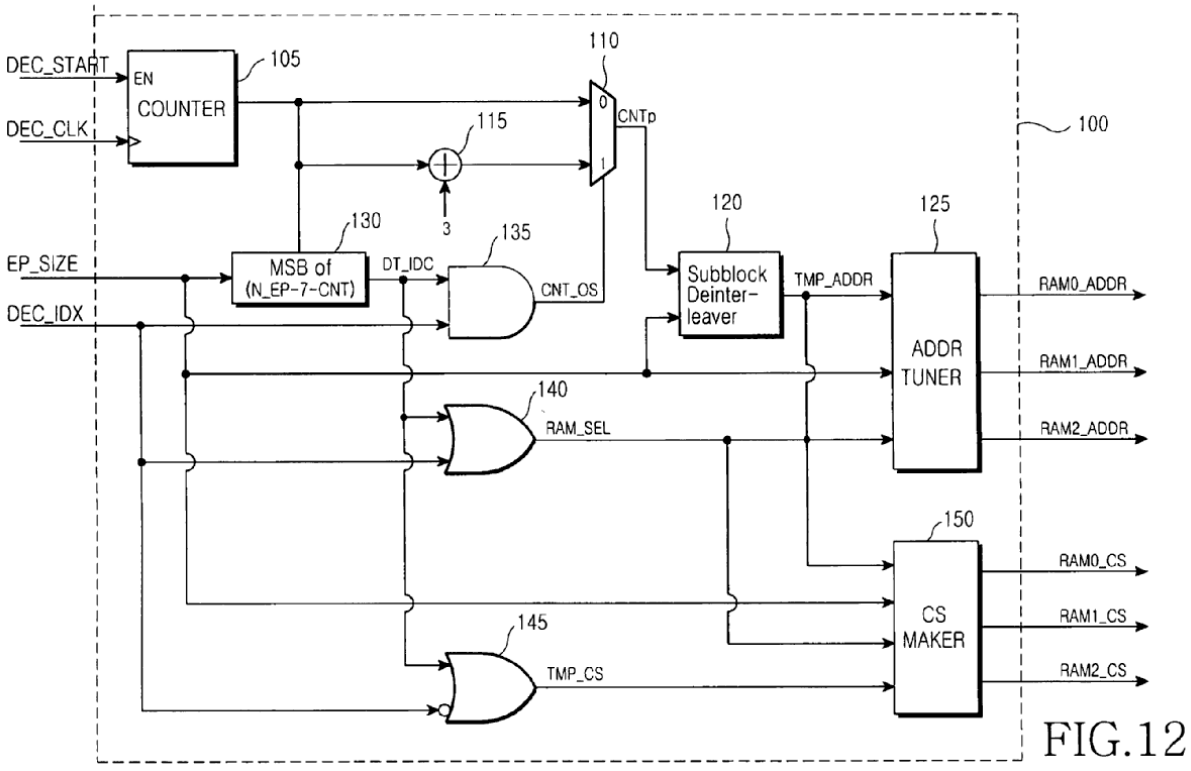

FIG.12

Clarity and added subject-matter

2. The objections raised by the board under Articles 84 and 123(2) EPC have been overcome by amendment.

2.1 Claim 1 is essentially based on original claims 1 (features (a) and (d)), 8 (features (c) and (e) to (h)) and 9 (features (i) to (m)) along with some additional features from the description, as explained in the following. The clarification in features (b), (c), (d) and (g) that some steps are performed by the receiver is implicit from the original claims.

2.1.1 Features (a) and (d) are based on original claim 1 combined with features clarifying that the different types of symbols are stored in the three memories, respectively, in an interleaved order, as explained in the application as filed on page 9, lines 25 to 30 (systematic symbols SYS and parity symbols PA0 and

PA1), page 14, lines 3 to 22 with reference to Figure 8 (storage of the types of symbols in three memories, respectively), and page 15, lines 18 to 21 (interleaved order).

2.1.2 Feature (b) is disclosed on page 29, lines 1 to 11, which explains that the size of the EP is received in control data by a receiver of the mobile communication system (corresponding to the receiver described on page 3, lines 6 to 14).

2.1.3 Features (l) combine features from original claim 9 with the specifications that the memory select signal RAM_SEL is 0 only when data symbols are read for the first constituent decoder, and that DEC_IDX set to 0 identifies the first constituent decoder. These features are directly and unambiguously derivable from original claim 4 (which uses the designation "memory select signals RAM_SEL"), in combination with page 17, lines 2 to 4, and page 18, lines 5 to 10.

2.2 Similarly, independent claim 4 is based essentially on original claims 18, 19 and 21, and the passages cited above for claim 1. The features of the read address generator RAG, which includes an input address generator 125 and a chip select signal generator 150, are also disclosed in the description on page 18, line 12, to page 13, line 6, with reference to Figure 12 reproduced above.

2.3 Dependent claims 2, 3, 5 and 6 correspond to original claims 10, 11, 23 and 24, respectively.

Closest prior-art document

3. The decision under appeal cites two documents as "document D1", namely patent document WO 02/21715 cited on page 1 of the written decision, and the closest prior-art document XP002303828 cited on page 4 (see points I and II above). In addition, the written decision cites document D9, with XP number XP002247591, on page 2 (see point II above).

The closest prior-art document D1 cited on page 4 of the contested decision and document D9 cited on page 2 have the same title but different XP numbers (document identifiers specific to the EPO databases). The board could not retrieve any document from the EPO databases with the XP number of the closest prior-art document D1 (XP002303828) indicated on page 4 of the written decision, which provides only the title of the document. Page 2 indicates that document D9 is an internet citation, but the board could not find in the electronic file a copy of the document corresponding to the internet disclosure nor any indication of the URL from which the document was retrieved. The search report indicates that the document with XP number XP002247591, i.e. document D9, was retrieved from the internet, but it does not provide the URL address. From the EPO databases, the board managed to obtain the URL corresponding to document D9 and was able to establish that the document could still be retrieved at that address (see point IV above).

In spite of the conflicting and insufficient indications in both the decision under appeal and the electronic file, the board concluded that the closest prior-art document D1 referred to in the inventive-step reasoning on pages 4 to 7 of the decision under appeal is the same as document D9 cited on page 2, and

corresponds to the internet disclosure at the URL address at which the board arrived after consulting the EPO's database. The board annexed a copy of document D9 to its communication and reviewed the inventive-step assessment in the decision under appeal in light of document D9. The appellant did not object to this.

Inventive step

4. Document D9 is a presentation on the 1xEV-DV Forward Link technology. It discloses the fixed packet sizes (corresponding to the EP sizes of the invention in this case), turbo coding and quasi-complementary turbo code (QCTC) interleaving (page 2 entitled "Key Aspects of Current 1xEV-DV Forward Link Design"); a forward packet data channel including a phase "Add 6-Bit Turbo Encoder Tail Allowance", a "Turbo Encoder R=1/5" and a "QCTC Channel Interleaver" (page 12, "Format Packet Data Channel"); and interleaving of sub-blocks S, P0, P'0, P1, P'1 (page 14) and a forward secondary packet data control channel including a "Block Interleaver" (page 16).

4.1 In the decision under appeal, the examining division conceded that document D9 did not disclose the first, second and third memories, nor did it disclose generating read addresses of information symbols in the first memory and of parity bit symbols in the second and third memories, outputting the code symbols in parallel to the two constituent decoders and generating chip select signals. Compared with claim 1 of the requests considered in the decision under appeal, current claim 1 specifies further features describing details of the implementation.

Document D9 can be considered to implicitly disclose decoding and some form of de-interleaving at the

receiver. However, no details of an implementation of the de-interleaving are described. Document D9 does not disclose at least features (g) to (m) and the following part of feature (a):

(a') storing the systematic code symbols, first parity code symbols and second parity code symbols in first, second and third memories respectively.

4.2 The board agrees with the appellant that, compared with the prior art of document D9, the distinguishing features provide an efficient solution, in terms of data processing rate, for constructing the turbo decoder data input means at a receiver. This effect is mentioned for instance on page 2, lines 9 to 15, and page 14, lines 3 to 6, of the description as filed.

4.3 Since the invention concerns a hardware implementation of a method for receiving code symbols, storing them in a memory, and inputting them to a turbo decoder, there is no doubt that the claimed subject-matter and the aforementioned effect are technical.

4.4 Even though some of the distinguishing features could, in isolation, be considered either obvious for the skilled person or commonly known implementation details, the board is of the opinion that the skilled person would not arrive at the combination of the distinguishing features without exercising inventive skill or without a prompt in that direction. None of the cited prior-art documents discloses the distinguishing features or provides a suggestion which would lead the skilled person to the claimed solution.

4.5 Therefore, the method of claim 1 is inventive over the prior art cited in the proceedings (Article 56 EPC).

4.6 Similar comments apply to independent claim 4, which also specifies feature (a') and many implementation details of the read address generator, including features corresponding substantially to features (g) to (m). For essentially the same reasons as given for claim 1, the board is satisfied that the apparatus of claim 4 is inventive (Article 56 EPC).

4.7 Dependent claims 2, 3, 5 and 6 specify additional features and thus also comply with Article 56 EPC.

Concluding remarks

5. In view of the above, the board has no objections against the claims and the decision under appeal is to be set aside. However, the description and drawings may need to be adapted to the claims. Therefore, the case is to be remitted to the department of first instance for granting on the basis of claims 1 to 6 filed on 20 April 2021, and the description and drawings to be adapted if necessary. The appellant may also want to correct minor typographic mistakes in the claims (e.g. "TMP ADDR" to "TMP_ADDR" in claim 4).

6. In its examination of the appeal case, the board identified some deficiencies in the proceedings before the examining division and in the decision under appeal.

6.1 The closest prior-art document D9 on which the inventive-step reasoning for the refusal was based has not been correctly cited and identified in the decision under appeal (see also points IV. and 3. above), and there is insufficient information on file about that document. It is unclear whether a patent professional or a member of the general public with no access to the internal EPO databases would have been able to

understand which document was used as the closest prior art and to obtain a copy of the document, let alone review the reasons for refusing the application. As explained above, however, the board did manage to obtain a copy of the document and review the decision under appeal.

6.2 In addition, the information on file is insufficient to establish when the internet disclosure of document D9 became public (see also T 1066/13 of 9 July 2018, reasons 3 to 5). Document D9 retrieved by the board does not include a publication date. The search report and the decision under appeal indicate that the document was published on 16 November 2001, but the board could not find any explanation in the file on how the publication date was established or any evidence concerning the publication date of document D9.

6.3 Another deficiency concerns the excessive length of the proceedings. The application, which claims priority from a Korean application filed on 23 November 2002, was filed as a European application on 24 November 2003 and refused at the oral proceedings on 13 November 2018. Between the applicant's letter of 22 March 2010 and the summons to oral proceedings eight years later on 8 May 2018 the examining division did not issue any office actions. In line with a number of decisions of the Boards of Appeal, including T 823/11 of 21 December 2015, T 2377/17 of 3 December 2018 and T 2707/16 of 11 December 2018, such delays may constitute a procedural violation.

7. In the grounds of appeal the appellant had not mentioned any such issues and had implicitly requested that the case be remitted for grant (see point III. above). The board was able to obtain a copy of the closest prior-art document used in the decision under

appeal. In light of this, and for the sake of procedural efficiency, the board opted to examine the ground for refusal in substance and mention in its communication the most relevant issues regarding the closest prior art (see point IV. above). For the reasons below, the question of whether those deficiencies amounted to a substantial procedural violation within the meaning of Rule 103(1)(a) EPC does not have to be answered.

7.1 The appellant (applicant) did not request reimbursement of the appeal fee or ever mention any deficiencies. During the long examination proceedings, it did not request accelerated processing of the application or otherwise protested against the long duration of the examination.

7.2 According to decision T 2707/16, "a reimbursement of the appeal fee in view of unreasonable delays in first-instance proceedings should be regarded as equitable only where the applicant has made clear by some action that [it] did not tacitly agree with the stagnation of the proceedings" (Reasons 36). Since this criterion is not met in the case in hand, it is irrelevant whether the unreasonable examination delays constituted a substantial procedural violation.

7.3 As for the incorrect citation of the closest prior-art document in the decision under appeal, the board was able to identify the document referred to and review the inventive-step assessment in the contested decision. Since the claimed subject-matter is inventive over the disclosure of document D9, and the appellant did not contest it as prior art, there is no further need to establish whether the internet disclosure of D9 was indeed made public before the application's effective filing date. The board will therefore not

rule on whether the deficiencies regarding the citation of the closest prior-art document constituted a substantial procedural violation.

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the department of first instance for further prosecution.

The Registrar: The Chairman:

T. Buschek J. Geschwind

Decision electronically authenticated