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Datasheet for the decision of 11 January 2023

Case Number: T 1361/19 - 3.4.03

Application Number: 10156350.0

Publication Number: 2230691

IPC: H01L27/146

Language of the proceedings: EN

Title of invention:
Semiconductor device and method of manufacturing the same, and electronic apparatus

Applicant:
Sony Group Corporation

Headword:

Relevant legal provisions:
RPBA 2020 Art. 13(1), 13(2)
EPC Art. 54, 56

Keyword:
Amendment after summons - taken into account (yes)
Novelty - main request (yes)
Inventive step - main request (yes) - non-obvious modification

This datasheet is not part of the Decision.
It can be changed at any time and without notice.

Decisions cited:
T 0247/20, T 2920/18, T 1569/17

Catchword:

This datasheet is not part of the Decision.
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Beschwerdekammern

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Case Number: T 1361/19 - 3.4.03

D E C I S I O N
of Technical Board of Appeal 3.4.03
of 11 January 2023

Appellant: (Applicant)	Sony Group Corporation 1-7-1 Konan Minato-ku Tokyo 108-0075 (JP)
Representative:	MFG Patentanwälte Meyer-Wildhagen Meggle-Freund Gerhard PartG mbB Amalienstraße 62 80799 München (DE)
Decision under appeal:	**Decision of the Examining Division of the European Patent Office posted on 29 November 2018 refusing European patent application No. 10156350.0 pursuant to Article 97(2) EPC.**

Composition of the Board:

Chairman	M. Papastefanou
Members:	J. Thomas
	E. Mille

Summary of Facts and Submissions

I. The appeal is against the decision of the examining division to refuse European patent application No. 10 156 350 on the grounds that

- the subject-matter of the then main request extended beyond the the content of the application as filed and the wording of the claims was not clear and concise,
- the subject-matter defined in claim 1 of the then first auxiliary request was not new, and
- the then second and third auxiliary requests were not admitted into the proceedings under Rule 137(3) EPC, because they were late filed and the subject-matter defined in claim 1 of the then second auxiliary request was *prima facie* not new and the wording of the claims of the then third auxiliary request was not clear and concise.

II. At the end of the oral proceedings before the Board the appellant requested that the decision under appeal be set aside and that a patent be granted on the basis of the set of claims of the new main request submitted by the appellant during the oral proceedings before the Board or alternatively one of the first to eighth auxiliary requests, the first auxiliary request corresponding to the main request submitted with the statement setting out the grounds of appeal and the second to eighth auxiliary requests corresponding respectively to the first to seventh auxiliary requests submitted with the statement setting out the grounds of appeal.

III. The current main request is composed of the following application documents:

Description:
page 1 filed by the appellant during the oral proceedings before the Board and
pages 2 to 32 as originally filed (page 33 to be deleted).

Claims:
No. 1 to 3 of the main request filed by the appellant during the oral proceedings before the Board.

Drawings:
Sheets 1/29 to 29/29 as originally filed.

IV. The following documents are referred to:
D1: FR 2 910 707 A1
D1*: US 8 003 433 B2 (family member of document D1)

V. Independent claim 1 of the main request reads as follows:

"*A method of manufacturing a semiconductor device to provide a back-illuminated solid-state imaging device (1), comprising the steps of:*
bonding a first semiconductor substrate (31) and a second semiconductor substrate (45) together, wherein the first semiconductor substrate (31) includes a pixel array (23) in a half-finished product state, and, formed on the first semiconductor substrate (31), a first multi-wiring layer (41) including a metal wiring layer (40) and a first layer (57) of the first multi-wiring layer (41);
the second semiconductor substrate (45) includes a logic circuit (25) in a half-finished product state,

and, formed on the second semiconductor substrate (45), a second multi-wiring layer (55) including a metal wiring layer (53) and a second layer (57) over the second multi-wiring layer (55); and
the first semiconductor substrate (31) and the second semiconductor substrate (45) are bonded together, such that the first and second multi-wiring layers (41, 55) face to each other;
after bonding, thinning the first semiconductor substrate (31) to a thickness of 1 to 10 µm;
next, forming a through-connection hole (61) penetrating the first semiconductor substrate (31), the first multi-wiring layer (41) and the first and second layers (57), so as to expose the metal wiring layer (53) of the second multi-wiring layer (55), and a connection hole (62) passing through the first semiconductor substrate (31) into the multi-wiring layer (41), so as to expose the metal wiring layer (40) of the first multi-wiring layer (41);
electrically connecting the pixel array (23) and the logic circuit (25) by embedding a through-connection conductor (64) into the through-connection hole (61), the through-connection conductor (64) penetrating the first semiconductor substrate (31), the first multi-wiring layer (41) and the first and second layers (57), extending to the logic circuit (25) of the second semiconductor substrate (45) and electrically connecting to the wiring layer (53) of the second multi-wiring layer (55), and embedding a connection conductor (65) in the connection hole (62) and electrically connecting the metal wiring layer (40) of the first multi-wiring layer (41);
forming a connection wiring (72) electrically connected to the through-connection conductor (64) and the connection conductor (65)."

VI. The appellant's arguments, insofar as they are relevant to the present decision, may be summarised as follows:

The newly submitted main request should be admitted into the proceedings since the appellant had always claimed that the manufacturing method was novel and inventive over the documents D1 / D1*. Only the discussion at the oral proceedings allowed the precise differentiation between the device and manufacturing method. Therefore, an appropriate reaction from the appellant should be possible.

As far as novelty and inventive step are concerned, the two separate manufacturing steps for the electrical connection of the pixel array to the logic circuit presented the differentiating feature. In contrast, documents D1 / D1* disclosed only one manufacturing step for making the connection between the pixel array and the logic circuit by applying a single layer in and between the connection and through-connection holes. Manufacturing the electrical connection wiring between small scale and closely spaced connection and through-connection holes by firstly filling the holes with a conductor and then, in a separate manufacturing step, providing the connection wiring between the holes allowed a more precise and selective electrical connection in contrast to a widely applied connecting layer (D1 / D1*: layer 50). This solution was neither shown nor hinted at in documents D1 / D1* and was also not rendered obvious on the basis of common general knowledge. All other cited documents were further away from the claimed subject-matter. Hence, the claimed subject-matter involved an inventive step.

VII. The examining division's arguments, insofar as they are relevant to the present decision, may be summarised as follows:

The provision of the conductive layer (50) anticipated both manufacturing steps, the step of "*electrically connecting the pixel array (23) and the logic circuit (25)*" by providing a connection conductor and a through-connection conductor in the respective connection hole and the through-connection hole and the step of "*forming a connection wiring (72)*" in order to connect the the pixel array to the logic circuit (Reasons, point 4.2).

Reasons for the Decision

1. Admission of the main request into the proceedings

1.1 The main request was filed during the oral proceedings before the Board and thus after the notification of the summons to oral proceedings. Hence, without prejudice to the party's arguments, its admittance is governed by Article 13(1) and (2) RPBA 2020 according to which any amendment to a party's appeal case is, "*in principle, not taken into account unless there are exceptional circumstances, which have been justified with cogent reasons by the party concerned*".

1.2 The Board follows decision T 247/20, point 1.3 of the Reasons, in that the examination under Article 13(2) RPBA 2020 is of a two-step nature, i.e. in that it is first necessary to examine whether there is an "*amendment to a party’s appeal case*". If that question is answered in the negative, there is no discretion not to take the relevant submission into account. However, if the question is answered in the positive, it is

necessary to examine whether the party concerned has provided cogent reasons for the existence of exceptional circumstances which may justify the submission at such an advanced stage of the proceedings.

1.3 Whether the deletion of part of the claims in a pending request constitutes an "*amendment to a party's appeal case*" within the meaning of Article 13 RPBA 2020 is controversially discussed among the Boards and accordingly answered differently (see e.g. T 2920/18, point 3.6 with sub-points or T 1569/17, point 4.3 with sub-points).

1.4 In the case at hand, the Board is of the opinion that the limitation of the present main request to a "*method of manufacturing a semiconductor device*" with the deletion of the claims referring to "*[a] semiconductor device*" is not an amendment to the party's appeal case, even if the deletion of claims could always be considered as an "*amendment*" as such.

The factual situation with respect to the remaining part, namely the claims related to a "*method of manufacturing*", did not change at all compared to all submissions related to the manufacturing method prior to this amendment. The claimed "*method of manufacturing*" was part of the discussion before the examining division (see minutes of the oral proceedings before the examining division, ninth paragraph) and the examining division dealt with the identical claims in its decision (Reasons, point 4.2). Moreover, the discussion of inventive step of the claims of the previous main request (filed with the statement setting out the grounds of appeal and identical to the first auxiliary request of the impugned decision), which

contained the claims directed to the "*method of manufacturing*" in unchanged form, was dealt with in the statement setting out the grounds of appeal (pages 13 to 15, "*b) Inventive Step*"). Therefore, the subject-matter of the present main request (i.e. the method claims of the previous main request) was already part of the examining division's decision and was entirely addressed by the appellant in its statement setting out the grounds of appeal. Consequently, the deletion of the device claims does neither result in a changed factual situation for the "*method of manufacturing*" nor in a different weighting of the remaining subject-matter due to the deletion of the device claims.

The fact that the manufacturing method is considered differently in the new main request is not a consequence of the deletion of the device claims, but merely due to a different consideration of the manufacturing method itself after discussion during the oral proceedings before the Board. In view of this, the new main request submitted at the oral proceedings before the Board is not considered to be an amendment to the party's appeal case, as all of the appellant's arguments and submissions on this remaining part ("*the method of manufacturing*") remained unchanged. Consequently, the Board has no discretion not to admit this new main request into the proceedings under Article 13(2) RPBA 2020.

1.5 Hence, the main request is admitted into the proceedings.

2. Documents D1 and D1*

Novelty and inventive step are discussed with regard to documents D1 and D1* which are related family

documents. Document D1, written in French, was published prior to the filing date of the present application whereas document D1*, written in English, was published after the filing date of the present application. Due to the languages used, the appellant referred to the family document D1* and the Board agreed that document D1* could be used for the discussion of novelty and inventive step, since its content is, apart from one paragraph irrelevant to the present case, the same as that of document D1. Therefore, in the following, reference is made to document D1* and thus implicitly to the equivalent content of document D1.

3. Novelty

Document D1* discloses (the references in parentheses in this paragraph refer to document D1*) a method of manufacturing a semiconductor device to provide a back-illuminated solid-state imaging device, comprising the steps of:
bonding a first semiconductor substrate (12) and a second semiconductor substrate (30) together (Figures 3 and 4, column 6, lines 17 to 25), wherein the first semiconductor substrate (12) includes a pixel array (column 4, lines 18 to 27) in a half-finished product state (Figure 1), and, formed on the first semiconductor substrate (12), a first multi-wiring layer (24) including a metal wiring layer (16, 18, 20, 22) and a first layer (28) of the first multi-wiring layer (24);
the second semiconductor substrate (30) includes a logic circuit (Figure 2; column 6, lines 1 to 5) in a half-finished product state, and, formed on the second semiconductor substrate (30), a second multi-wiring layer (44) including a metal wiring layer (42, 38, 40)

and a second layer (48) over the second multi-wiring layer (44); and
the first semiconductor substrate (12) and the second semiconductor substrate (30) are bonded together, such that the first and second multi-wiring layers (24, 44) face to each other (Figure 3); after bonding, thinning the first semiconductor substrate (12, figures 4 and 5, column 6, lines 37 to 45) to a thickness of 1 to 10 µm (column 6, lines 49 to 50,"*3 to 5 µm*");
next, forming a through-connection hole (figures 5 and 6) penetrating the first semiconductor substrate (12), the first multi-wiring layer (24) and the first and second layers (28, 48), so as to expose the metal wiring layer (42) of the second multi-wiring layer (44), and a connection hole (Figures 10 and 11) passing through the first semiconductor substrate (12) into the multi-wiring layer (24), so as to expose the metal wiring layer (16) of the first multi wiring layer (24); electrically connecting the pixel array and the logic circuit by ~~embedding a through connection conductor (50) into the through-connection hole~~ providing a conductive layer in the through-connection hole (50; Figures 10 and 11), the through-connection conductor (layer 50) penetrating the first semiconductor substrate (12), the first multi-wiring layer (24) and the first and second layers (28, 48), extending to the logic circuit (Figures 10 and 11) of the second semiconductor substrate (30) and electrically connecting to the wiring layer (42) of the second multi-wiring layer (44), and ~~embedding a connection conductor (50) in the connection hole~~ providing the same layer (50) also in the connection hole (Figures 10 and 11) and thereby electrically connecting the metal wiring layer (16) of the first multi-wiring layer (24) whereby the layer (50) is also provided on the surface so as to connect the logic circuit with the pixel array

~~forming a connection wiring electrically connected, to the through-connection conductor and the connection conductor~~.

Contrary to the argumentation of the examining division, which apparently read the provision of the electrically conducting layer 50 in document D1* on both manufacturing steps, the Board is of the opinion that in the present definition of claim 1 the electrical connection of the logic circuit to the pixel array is undoubtedly made in two separate manufacturing steps and not in a single one. The last step of "*forming a connection wiring*" which is electrically connected to the through-connection conductor and the connection conductor is according to the wording of claim 1 a separate manufacturing step compared to the previous step ("*electrically connecting the pixel array and the logic circuit by embedding ...*") in which a connection conductor is embedded in the connection hole and through-connection conductor is embedded in the through-connection hole. This is also clear from the punctuation, as the first manufacturing step is separated from the second manufacturing step by a semicolon. Both manufacturing steps are also presented as separate steps in the description of the application (e.g. description, page 19, lines 1 to 4 and lines 19 to 20 or page 30, lines 17 to 19). Hence, these two manufacturing steps are not to be mixed up with a single manufacturing step and consequently present a novel feature.

Therefore, the subject-matter defined in present claim 1 is new over the teaching of documents D1 / D1*.

4. Inventive step

4.1 Closest prior art

It is undisputed that document D1 (and consequently also D1*, see point 2. above) represents the closest prior art because it also relates to a manufacturing method of a semiconductor device wherein two wafers with electrical components (a pixel array and a logic circuit) are bonded together and these electrical components are electrically connected together from a single side.

4.2 Differentiating features

As indicated under point 3. above, the subject matter defined in the present claim 1 differs from the manufacturing method known from documents D1 / D1* by the two separate manufacturing steps for connecting the pixel array to the logic circuit, wherein in a first step, a connecting material is embedded in the connection hole and the through-connection hole, and in a second step, a connection wiring is provided to connect the two holes to each other at the (rear) surface of one of the bonded wafers.

4.3 Objective technical problem / technical effect

This differentiating feature has the technical effect of allowing precise and selective connections between the conductors in the connection and through-connection holes as well as the wiring on the surface. The advantage is that the holes, through holes and their connections can be located more precisely and selectively in contrast to a layer covering the whole surface as done in document D1 / D1*. This is particularly advantageous if the entire device is very small.

4.4 Obviousness

At first glance, it may seem obvious from an electrical point of view to connect the pixel array to the logic circuit either by a single connection through a conducting layer (as realised in documents D1 / D1* by layer 50) or by a plurality of interconnected electrical conductors (as realised in the present application). However, the Board finds it not obvious from a manufacturing point of view to modify the manufacturing method known from documents D1 / D1* in such a way as to arrive at the claimed manufacturing method for the following reasons.

When starting from documents D1 / D1* there is no motivation for the skilled person to change the rather simple one-step manufacturing method in order to provide a more precise connection between the holes. Normally a plurality of connection holes is foreseen in such a kind of devices, as for example one hole for connecting each pixel row of the image sensor. The electrical components in these different holes are to be connected separately to the logic circuit. Providing a separate connection wiring on the (rear) surface of the device has the advantage that the connection between the different holes can also be precisely and selectively manufactured between small holes and through-holes which are also more precisely and more selectively manufactured at preferred locations in the device. In contrast, the connection proposed in document D1, where a single connection layer is applied to the surface and the holes in a single manufacturing step is simpler but not as precise and selective between different connection and through-connection holes and their specific locations. Consequently, the

two-step manufacturing process according to the present invention is not a straightforward development. It is a more complicated manufacturing process that enables the specific selective and precise positioning of the connection and through-connection holes and the electric wiring there between. Even if the person skilled in the art was looking for a more precise connection, there are many other ways to implement a more precise connection. It is therefore not obvious to the skilled person why they should change the rather simple one-step manufacturing process known from documents D1 / D1* to arrive at the claimed two-step manufacturing method as defined in claim 1.

4.5 Therefore the Board concludes that the subject-matter defined in present claim 1 involves an inventive step. The same conclusion applies to claims 2 and 3 because of their dependence on claim 1.

5. The Board, thus, judges that the application and the invention to which it relates, in the version according to the appellant's main request, meet the requirements of the EPC. Hence, a patent is to be granted on the basis of that version (Articles 97(1) and 111(1) EPC).

6. Since the main request succeeds, the discussion of any of the auxiliary requests is not necessary.

Order

For these reasons it is decided that:

The decision under appeal is set aside.

The case is remitted to the examining division with the order to grant a patent in the following version:

Description:
page 1 filed by the appellant during the oral proceedings before the Board and
pages 2 to 32 as originally filed.

Claims:
No. 1 to 3 of the main request filed by the appellant during the oral proceedings before the Board.

Drawings:
Sheets 1/29 to 29/29 as originally filed.

The Registrar: The Chair:

S. Sánchez Chiquero M. Papastefanou

Decision electronically authenticated