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Datasheet for the decision of 11 September 2020

Case Number: T 2708/16 - 3.5.07

Application Number: 09740614.4

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Language of the proceedings: EN

Title of invention:
Multi-level feed-back digital-to-analog converter using a chopper voltage reference for a switched capacitor sigma-delta analog-to-digital converter

Applicant:
Microchip Technology Incorporated

Headword:
Digital-to-analog converter using a chopper voltage reference for a switched capacitor sigma-delta ADC/Microchip Technology

Relevant legal provisions:
EPC Art. 84, 83, 56, 111

Keyword:

Claims - independent claims of sole request - after amendment (yes)
Sufficiency of disclosure - (yes)
Inventive step - after amendment (yes)
Appeal decision - remittal to the department of first instance (yes)

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Case Number: T 2708/16 - 3.5.07

D E C I S I O N
of Technical Board of Appeal 3.5.07
of 11 September 2020

Appellant: (Applicant)	Microchip Technology Incorporated 2355 West Chandler Boulevard Chandler, AZ 85224-6199 (US)
Representative:	sgb europe Lechnerstraße 25a 82067 Ebenhausen (DE)
Decision under appeal:	**Decision of the Examining Division of the European Patent Office posted on 14 July 2016 refusing European patent application No. 09740614.4 pursuant to Article 97(2) EPC.**

Composition of the Board:

Chair	P. San-Bento Furtado
Members:	C. Barel-Faucheux
	E. Mille

Summary of Facts and Submissions

I. The applicant (appellant) appealed against the decision of the examining division refusing European patent application No. 09740614.4, filed as international application PCT/US2009/061617 and published as WO 2010/048371.

II. The decision cited the following document, *inter alia*:
D1: WO 2008/014246 A1, published on 31 January 2008.

III. The examining division decided that the application did not disclose the subject-matter of independent claims 1 and 8 of the main and auxiliary requests in a manner sufficiently clear and complete for it to be carried out by a person skilled in the art (Article 83 EPC), and that the subject-matter of independent claims 1 and 8 of both requests was not clearly defined (Article 84 EPC) and lacked inventive step (Article 56 EPC). Furthermore, for both requests, dependent claims 2, 4 to 7, 10 and 13 to 15 did not fulfil the requirements of Article 84 EPC, while dependent claims 2, 3, 9, 12 and 14 did not fulfil the requirements of Article 56 EPC.

IV. With the statement of grounds of appeal, the appellant filed a new sole request replacing the previous requests. It made some remarks regarding procedural aspects.

V. The application cites the following prior art document:
D7: US 7102558 B2, published on 5 September 2006.

VI. In a communication under Article 15(1) RPBA accompanying the summons to oral proceedings, the board

expressed its preliminary opinion that independent claims 1 and 8 did not fulfil the requirements of Article 84 EPC, and that the objections under Article 83 EPC in the decision under appeal seemed instead to relate to clarity. It seemed that the skilled person would be able to implement the subject-matter of claim 1 in the light of the description.

The subject-matter of independent claims 1 and 8 and of dependent claims 2, 3, 9, 12 and 14 did not seem to be new over the disclosure of document D1, and the subject-matter of claim 1 did not seem to be inventive over either document D7 or the prior art acknowledged in the application, in combination with the disclosure of document D1. With regard to the procedural aspects mentioned by the appellant, the board was of the preliminary view that no procedural error had occurred.

VII. In response, the appellant submitted a new sole (main) request and arguments.

VIII. The oral proceedings were held as scheduled. During the oral proceedings the appellant filed a new set of claims to replace the previous claims. At the end of the oral proceedings, the chairwoman pronounced the board's decision.

IX. The appellant's final requests were that the decision under appeal be set aside and that a patent be granted on the basis of the set of claims 1 to 16 submitted during the oral proceedings.

X. Claim 1 of the sole request reads as follows:

"A multi-bit digital-to-analog converter (DAC) comprising:

- a chopped reference voltage generator generating a reference voltage and offset voltage, wherein the offset voltage is alternatingly added to or subtracted from the reference voltage;

- a switched capacitor stage (102; 155) receiving said chopped reference voltage and configured to generate a plurality of output voltages according to respective DAC input values;

- a switching sequencer (160; 610) for generating control signals, wherein for generating one of said plurality of output voltages said switching sequencer (160; 610) controls said switched capacitor stage (102; 155) to generate one of a plurality of switching patterns through said control signals, wherein each switching pattern controls switches of said switched capacitor stage (102; 155) during a charge phase and a transfer phase thereby generating the one of said plurality of output voltages,

characterized in that

chopping of the chopped reference voltage generator is synchronized with the charge phase and the transfer phase, and

for at least one DAC input value the switching sequencer (160; 610) provides two different switching patterns (A, B), wherein each of the two different switching patterns (A, B) generates a first one of said plurality of output voltages defined by said at least one DAC input value with a different output offset voltage added thereto, and wherein one of the two switching patterns (A) contributes a positive output offset voltage to the output voltage and the respective other switching pattern (B) contributes a negative output offset voltage to the output voltage and wherein output offset voltages added to the output voltages generated by the two different switching patterns cancel each other out."

XI. Claim 8 reads as follows:

"A method for producing output voltages of a plurality of output voltages in a switched capacitor multi-bit digital-to-analog converter (DAC), comprising the steps of:

- providing a chopped reference voltage generator generating a reference voltage and offset voltage, wherein the offset voltage is alternatingly added to or subtracted from the reference voltage;

- generating a plurality of output voltages according to respective DAC input values with a switched capacitor stage (102; 155) receiving said chopped reference voltage;

- generating control signals by a switching sequencer (160; 610), wherein for generating one of said plurality of output voltages said switching sequencer (160; 610) controls said switched capacitor stage (102; 155) to generate one of a plurality of switching patterns through said control signals, wherein each switching pattern controls switches of said switched capacitor stage (102; 155) during a charge phase and a transfer phase thereby generating the one of said plurality of output voltages, characterized in that the method further comprises the steps of:

synchronizing a chopping of the chopped reference voltage generator with the charge phase and the transfer phase, and

for at least one DAC input value providing by the switching sequencer (160; 610) two different switching patterns (A, B), wherein each of the two different switching patterns (A, B) generates a first one of said plurality of output voltages defined by said at least one DAC input value with a different output offset

voltage added thereto, and wherein one of the two switching patterns (A) contributes a positive output offset voltage to the output voltage and the respective other switching pattern (B) contributes a negative output offset voltage to the output voltage and wherein output offset voltages added to the output voltages generated by the two different switching patterns cancel each other out."

XII. The appellant's arguments, where relevant to this decision, are addressed in detail below.

Reasons for the Decision

Admissibility of the appeal

1. The appeal complies with the provisions of Rule 101 EPC and is therefore admissible.

Invention

2. The application relates to a digital-to-analog converter (DAC) for an analog-to-digital converter (ADC) and, more particularly, to a way of reducing 1/f noise and direct current (DC) offset from a voltage reference source associated with a switched capacitor multi-level sigma-delta ADC (see international publication, page 1, lines 1 to 13, and page 10, line 23 to page 11, line 9).

3. Figure 2 of the application illustrates a schematic circuit diagram of capacitor switching arrays and a differential amplifier for use in a multi-bit digital-to-analog converter (DAC). In this specific example of Figure 2, a five-level feed-back DAC is shown. The five-level feed-back DAC can be operated using

switching patterns that generate five equally spaced charge quantities during two phases, such as a charge phase and a transfer phase, of a differential charge transfer. A pattern defined by two phases generates an output voltage of the DAC. Conventional switching patterns are illustrated by Figures 3a to 3e. The five equally distributed charge levels in this five level embodiment are 2C*Vref, C*Vref, 0, -C*Vref and -2C*Vref (page 10, penultimate line to page 11, line 11, and page 12, lines 7 to 10).

4. The problem addressed by the present invention is that the conventional different switching sequences as shown in Figures 3a to 3e produce good results with high precision assuming that the reference voltage Vref does not have any offset. However, in reality, the reference voltage has an offset, Voffset, that negatively influences the performance of the DAC (page 13, line 28 to page 14, line 1; paragraph bridging pages 13 and 14).

5. The invention solves this problem by providing a chopped reference voltage with alternating positive and negative offset voltages synchronised with the charge and transfer phases and by using two different switching patterns contributing a negative and positive output offset voltage to the output voltage which cancel each other out.

6. If the reference voltage is chopped, a real voltage reference is assumed to produce an effective voltage reference Vrefeff = Vref + Voffset during Pl and Vrefeff = Vref - Voffset during P2, with phases P1 and P2 being the (pre-)charge and transfer phases of a pattern (page 15, last paragraph).

7. Table 2 reproduced below shows that when considering the reference voltage offset in such a DAC, certain input values generate output voltages that may or may not be affected by the reference voltage offset Voffset. In the specific example, sequences 2, 3, 4, 6, 7 and 8 generate output voltages that depend on the reference voltage offset. For the input value 0, sequences 4 and 6 can be omitted as sequence 5 produces a zero output, i.e. without offset. Thus, the five-level DAC is only affected by the offset for input values +1 and -1 (page 16, Table 2 and first paragraph of the text).

#	P1 (Vref+Voffset)	P2 (Vref-Voffset)	DAC Input	Total Charge (SQ)
1	+Vref +Voffset	-Vref + Voffset	+2	(+2Vref) * C
2	+Vref +Voffset	0	+1	(+Vref + Voffset) * C
3	0	-Vref + Voffset	+1	(+Vref - Voffset) * C
4	+Vref +Voffset	+Vref -Voffset	0	(+2Voffset) * C
5	0	0	0	0
6	-Vref -Voffset	-Vref + Voffset	0	(-2Voffset) * C
7	0	+Vref -Voffset	-1	(-Vref + Voffset) * C
8	- Vref - Voffset	0	-1	(-Vref - Voffset) * C
9	-Vref -Voffset	+Vref -Voffset	-2	(-2Vref) * C

8. In the embodiment of Figure 6, each capacitor 132a and 132b of Figure 2 has been replaced with two capacitors (142a, 152a), and (142b, 152b), respectively. As shown in Figure 6, splitting will result in a value of C/2 for each capacitor 142a, 142b, 152a and 152b (page 17, lines 17 to 21).

9. Each capacitor of half the value (C/2) is switched with a different switching pattern A or B, as shown in Figures 4a, 4b, 5a and 5b, in order to cancel the offset dependent remainder charge when the input of the

DAC is equal to 1 or - 1. For the input values 0, 2 and - 2, the same switching patterns as shown in Figures 3a, 3c and 3e apply to both switching circuits (description, page 17, lines 21 to 27).

Interpretation of claim 1

10. Claim 1 defines a multi-bit digital-to-analog converter (DAC) as illustrated by Figures 2 or 6.

10.1 This multi-bit DAC comprises a chopped reference voltage generator generating an (effective) reference voltage
Vrefeff = Vref + Voffset during Pl and
Vrefeff = Vref - Voffset during P2.

10.2 It also comprises a switched capacitor stage (Figure 2, 102, and Figure 6, 155) which receives said chopped reference voltage and is configured to generate a plurality of output voltages according to respective DAC input values (i.e. DAC input values "-2", "-1", "0", "+1", "+2", see Table 2 on page 16 reproduced in point 7. above). For the split configuration of the switched capacitor of Figure 6, the switching patterns for the upper and lower reference switching circuits will follow lines 2 and 3 for a +Vref*C transfer and lines 7 and 8 for a -Vref*C transfer and are shown in Figures 4a, 4b, 5a and 5b (page 18, lines 5 to 7; see also Tables 3a and 3b on page 18). Therefore, the "output voltages" of the claim correspond to the "Total Charge (SQ)" in Table 2, or in Tables 3a and 3b.

10.3 The DAC of claim 1 also comprises a switching sequencer ("switching control unit" 160 and 610 in Figures 2 and 6) for generating control signals, wherein for generating one of said plurality of output voltages

said switching sequencer controls said switched capacitor stage to generate one of a plurality of switching patterns through said control signals. Each switching pattern controls switches of said switched capacitor stage during a charge phase and a transfer phase, thereby generating the one of said plurality of output voltages (see Figures 4a, 4b, 5a and 5b).

10.4 For the DAC input value "+1", there are two switching patterns (numbered 2 and 3 in Table 2) that respectively generate a total charge (+Vref + Voffset) * C and (+Vref - Voffset) * C, and for the DAC input value "-1", there are two switching patterns (numbered 7 and 8 in Table 2) that respectively generate a total charge (-Vref + Voffset) * C and (-Vref - Voffset) * C.

10.5 By combining 2 and 3 for a DAC input value "+1" and 7 and 8 for a DAC input value "-1", offset cancellation can be achieved after each pair of transfers for the configuration in Figure 2. This corresponds to the "serial solution" evoked by the appellant in its arguments, and described in the application, for example on page 16, last full paragraph and on page 19, last paragraph. For the split switched capacitor of Figure 6, the offset cancellation can be achieved within a single transfer. This corresponds to the "parallel solution" evoked by the appellant in its arguments (see grounds of appeal, paragraph bridging pages 4 and 5) and described in the application, for example on page 17, last full paragraph, with reference to Figure 6.

Clarity, support and sufficiency of disclosure - claims 1 and 8

11. With the statement of grounds of appeal, in reply to the communication of the board and during the oral proceedings, the appellant amended claims 1 and 8, thereby overcoming all outstanding lack of clarity objections. Claim 1 defines a multi-bit DAC as described in point 10. above. Independent claim 8 defines a method for producing output voltages in a switched capacitor multi-bit DAC in terms of features corresponding to the features of claim 1. Thus, the board is satisfied that claims 1 and 8 are now clear.

12. In the appealed decision, two objections under Article 83 EPC were raised.

12.1 The first objection was that the disclosure of the description did not support that "for at least one DAC input value" two switching patterns were generated for the same output voltage, when the DAC input value is one of "+2", "0", or "-2" (point 13.1.2 of the decision under appeal).

12.1.1 Claim 1 specifies that "for at least one DAC input value the switching sequencer (160; 610) provides two different switching patterns (A, B)". It does not specify that for all possible DAC input values, two different switching patterns (A, B) generating a first one of said plurality of output voltages are provided. Furthermore, the feature is supported by the description (see e.g. page 15, last paragraph to page 17, last paragraph). Therefore, this objection is not justified.

12.2 The examining division also objected that the application did not provide details of how two

different switching patterns for the same output voltage could be applied with a switched capacitor stage having one (single) capacitor. It argued that the "switching pattern shown in fig. 4a (or fig. 4b) applied to a switched capacitor stage having one capacitor (Fig. 2) does not cancel out the offset for the same output voltage of the DAC within one charge and transfer phase (Fig. 4a: P1, P2)" (point 13.2 of the decision under appeal).

12.2.1 The description on page 18, line 5 to page 19, line 2, including Tables 3a and 3b, explains how, with the implementation of the multi-bit DAC of Figure 6, the offset Voffset is cancelled within one single charge and transfer phase. Indeed, this corresponds to the parallel implementation evoked by the appellant in its arguments. The decision under appeal did not question that the parallel solution of Figure 6 is sufficiently disclosed, and the board does not question this either.

12.2.2 The board acknowledges that in the serial solution, a pair of transfers is necessary for achieving offset cancellation (page 16, last full paragraph). However, claim 1 does not specify that the cancellation of the offset for the same output voltage of the DAC is within one (single) charge and transfer phase. Therefore, the implementation of that embodiment of the multi-bit DAC does not pose an unreasonable degree of difficulty.

12.3 In the board's opinion, the skilled person is able, on the basis of the description and using their common general knowledge, to implement the serial solution with cancellation of the offset in an even number of cycles.

13. In light of the foregoing, the board is satisfied that claim 1 and the corresponding claim 8 satisfy the requirements of Articles 83 and 84 EPC.

Basis in application as filed – claims 1 and 8

14. Claim 1 is based on claims 1 and 3 as originally filed and on Figure 2 and the corresponding description (page 10, line 29, to page 11, line 9; page 14, line 20, to page 16, line 14) together with Table 2 on page 16, as well as on Figure 6 and the corresponding description (page 17, lines 17 to 27; page 18, line 1, to page 19, line 2).

Therefore, claim 1 and the corresponding independent claim 8 satisfy the requirements of Article 123(2) EPC.

Inventive step over the prior art acknowledged in the application and disclosed in D7

15. Document D7 discloses a five-level feed-back DAC in a switched capacitor sigma-delta analog-to-digital converter (ADC)(column 1, lines 16 to 20). The five-level feed-back DAC has an improved switching sequence that boosts the number of quantisation levels of the conventional feed-back DAC from 2 to 5 (column 1, lines 60 to 67).

The techniques and DAC of D7 are described in detail in the present application, in which they are acknowledged as prior art.

15.1 Figure 1 of D7, which illustrates a five-level DAC including a switched capacitor stage, is identical to Figure 2 of the present application, but with a capacitance of C/2 in D7 instead of C in the present

application, and without a representation of a switching control unit. The description of Figure 1 of D7 in column 3, lines 10 to 40, is repeated in amended form in the description of Figure 2 of the present application on page 10, line 29, to page 12, line 6. Document D7 does not mention switching patterns, but it discloses switching sequences of the switches, and the timing diagrams of the switching sequences illustrated in Figures 2a to 2e of D7, and their description on column 3, line 41 to column 4, line 53, correspond to Figures 3a to 3e of the present application, and their description on page 12, line 7 to page 13, line 27.

15.2 Even though a switching control unit ("switching sequencer" in claim 1) is not shown in Figure 1 of D7, it is implicit from D7 that the switching sequences are produced by a switching sequencer.

Moreover, column 4, lines 54 to 67 of D7 discloses that the intermediate levels $C*V_{REF}/2$, 0 and $-C*V_{REF}/2$ (corresponding in the present application to $C*V_{REF}$, 0 and $-C*V_{REF)}$ can also be achieved through other switching sequences. Therefore, a switching sequencer is at least implicitly disclosed in D7.

15.3 D7 thus implicitly discloses Table 1 on page 15 of the present application.

15.4 The passages of the present application on page 10, line 29 to page 11, line 6, and page 11, lines 10 and 11 teach that the five-level feed-back DAC of Figure 2 can be operated using switching patterns that generate five equally spaced charge quantities during two phases, such as a charge and a transfer phase, of a differential charge transfer.

Figures 3a-3e illustrate timing diagrams for conventional switching patterns of the switches 104 to 116 used to obtain the five equally distributed charge levels 2C * Vref, C * Vref, 0, -C * Vref and -2C * Vref.

15.5 The application states on page 13, line 28 to page 14, line 1, that "[t]he conventional different switching sequences as shown in Figs. 3a-e produce good results with high precision assuming that the reference voltage does not have any offset. However, in reality the reference voltage Vref will have an offset Voffset that can and will negatively influence the performance of the digital-to-analog converter as will be explained in detail below." (emphasis added by the board). What follows from page 14, lines 1 to 19, is a general presentation of the invention, which is to "combine a conventional multi-bit DAC with a voltage reference that is using a Chopper algorithm and provide at the same time for a DAC that is inherently linear and for a removal of offset [...] induced by the reference circuit".

15.6 The explanation of the negative influence of the offset Voffset on the performance of the conventional DAC then starts on page 14, line 20, with reference to Figure 2. Basically the charging, during the charging phase or the next transfer phase, of the sampling caps 132a and 132b at either "0", "+Vref" and "-Vref" depending on the DAC input yields that, depending on the switching sequence, there are 9 possibilities for switching patterns with such a DAC, transferring only 5 levels for the total charge. In the conventional switching patterns as illustrated by Figures 3a to 3e, a "1" logic level depicts the respective switches in the closed position and a "0" logic level depicts the

respective switches in the open position (page 12, line 7 to page 13, line 27). In each of these figures, switches 104, 106 and 108 follow the same pattern as the corresponding switches in the other figures. For the combination of switches 112, 114 and 116, there are 3 possibilities in both the charge phase and the transfer phase yielding 9 possibilities in total, as illustrated in Table 1. The sentence on page 15, first full paragraph of text, concludes that "[c]onventional DACs, thus, merely select 5 suitable patterns to produce five distinct output voltages and use only those for operating the DAC".

15.7 It follows that Table 1 is a representation of the switching patterns or sequences that are known to the skilled person and can be used by the conventional DACs, such as the DAC from D7.

16. The distinguishing features of claim 1, having regard to this acknowledged prior art or the five-level DAC disclosed in document D7, are the following:

(F1) a chopped reference voltage generator is used that comprises alternating positive and negative offset voltages;

(F2) chopping of the chopped reference voltage generator is synchronized with the charge phase and the transfer phase, and

(F3) for at least one DAC input value the switching sequencer provides two different switching patterns (A, B), wherein each of the two different switching patterns (A, B) generates a first one of said plurality of output voltages defined by said at least one DAC input value with a different output offset voltage added thereto, and wherein one of the two switching patterns (A) contributes a positive output offset voltage to

the output voltage and the respective other switching pattern (B) contributes a negative output offset voltage to the output voltage and wherein output offset voltages added to the output voltages generated by the two different switching patterns cancel each other out.

17. The problem to be solved is to cancel the direct current (DC) offset generated by the reference voltage generator.

18. Document D7 does not consider offsets in the reference voltage generator. However, when trying to implement the five-level feed-back DAC from document D7, the skilled person would be confronted with the above mentioned problem. The skilled person would then come across document D1, which relates to analog-to-digital converters (ADCs) and, more particularly, to a way of reducing 1/f noise and DC offset from a voltage reference source associated with the analog-to-digital converter (description, page 1, lines 5 to 7).

18.1 In D1, a switched capacitor sigma-delta converter uses a digital-to-analog converter (DAC) in a feedback loop that applies a voltage(s) to an analog summing node located at the front end (analog portion) of the delta-sigma modulator (page 1, lines 26 to 28).

The two-level sigma-delta DAC shown in Figure 9 of D1 includes a "switched capacitor stage" which receives a reference voltage and generates a plurality of output voltages according to respective DAC input values (page 14, lines 1 to 7).

18.2 D1 teaches that "[f]or each DAC output configuration, i.e., for each DAC input code, the idea is to modulate

the chopping algorithm so that whenever an offset component is transferred by the DAC to the sigma-delta modulator, this offset component will be cancelled by an opposite offset component that would be obtained using the complimentary chopper configuration" (page 4, lines 24 to 27). It concludes by explaining that "[i]f one extracts the chopper sequencing related to each individual DAC input every time this input is given by the modulator, this sequence would be the standard chopping sequence : + , - that would cancel the offset after each even number of samples" (page 5, lines 3 to 5) (emphasis added by the board).

18.3 Figure 1 of D1 reproduced below illustrates a sigma-delta analog-to-digital converter (ADC) having a chopper stabilized voltage reference controlled by a serial bit stream from the sigma-delta modulator 106. A multi-level digital-to-analog converter (DAC) with a level higher than 2 may be used with the sigma-delta modulator 106 (page 8, lines 16 to 19; Figure 6). A digital filter 108 receives the over-sampled serial bit stream 112 and decimates and/or digitally low-pass filters the digital serial bit stream 112 so as to produce an n-bit parallel data word (on bus 110 in Figure 1) representative of the analog voltage on the input 118 (page 8, lines 24 to 27).

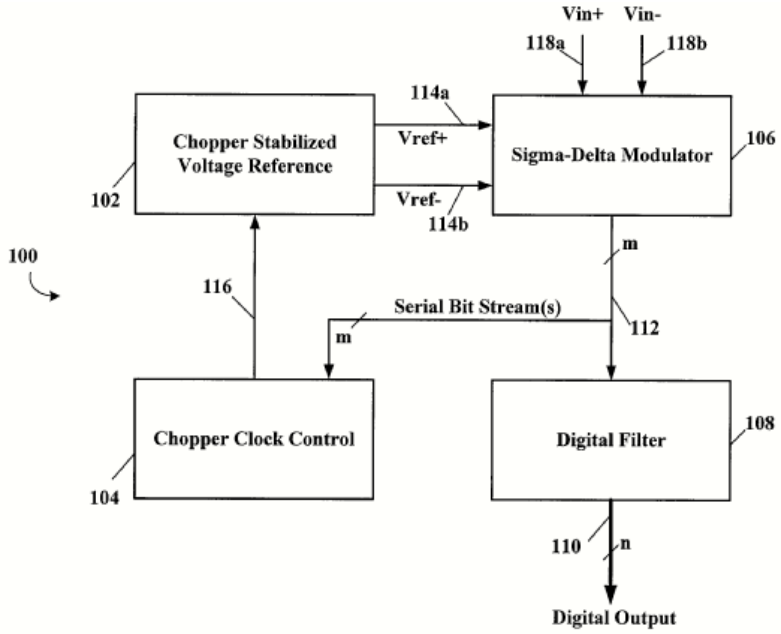

FIGURE 1

18.4 Figure 2 of D1 illustrates the chopper stabilized voltage reference generator 102 of Figure 1. Clocks from the chopper clock 116 are used to control the chopper modulator 224 and chopper demodulator 228. The reference voltage 114, Vref, will take on two values depending on the chop signal on the chopper clock 116 as follows:

Vref = Vref + Voff (voltage offset) if the chop signal is at a logic "1" and **Vref = Vref - Voff** if the chop signal is at a logic "0". So long as an equal number of chop signals at logic "1" and logic "0" are performed, the voltage offset component is canceled out, i.e., the + Voff and - Voff will cancel out (page 9, lines 12 to 19).

18.5 Figure 5 of D1 reproduced below illustrates a two-level sigma-delta modulator as used in Figure 1. The two-level sigma-delta modulator 106a may comprise a two-level digital-to-analog converter (DAC) 560.

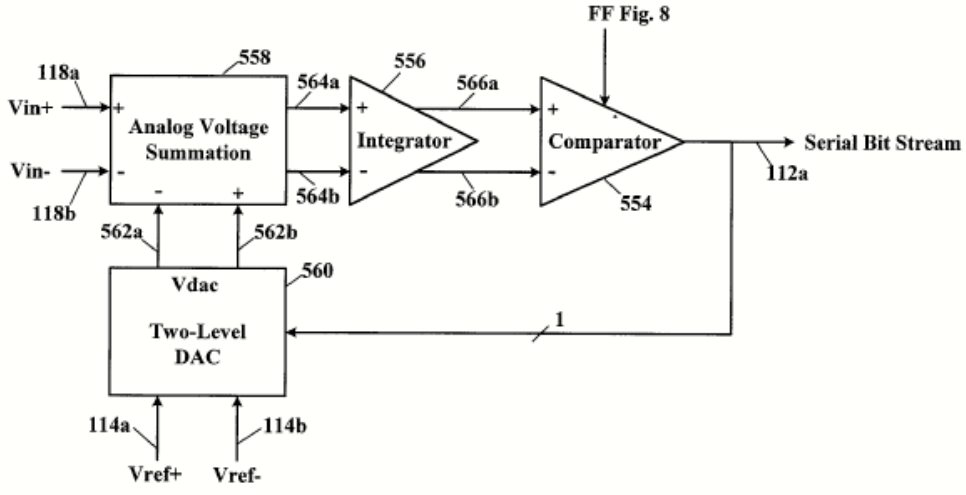

Figure 5

18.6 In its written submissions, the appellant argued that synchronised chopping as defined in feature (F2) meant that chopping was only dependent on the charge/transfer phases and not on any other parameter such as the DAC input. No further modulation was necessary. On the contrary, the solution of D1, as described on page 4, lines 11 to 18, relied on remembering the configuration of the chopper reference voltage generator and applying a complementary configuration the next time a Vref transfer was produced. This required modulation of the voltage reference generator. In other words, the voltage reference generator needed to be controlled to generate complementary offset voltages during the charge and transfer phases because the switching pattern for capacitive switching stage would not be altered.

At the oral proceedings the appellant further argued that document D1 taught the use of a bitstream to control the chopper clock, for example on page 9, lines 12 to 19, and page 19, lines 13 to 21, and in Figure 1. Document D1 explained in several passages, for example on page 4, lines 2 to 4, page 11, lines 11

to 25, and page 12, lines 1 to 3, that the "standard chopper algorithm (sequence of + -) for the voltage reference" did not cancel the offset component with any incoming bitstream.

18.7 The passage on page 10, line 26, to page 11, line 10, of D1 uses the example of a serial bit stream 112a having logic levels 1, 0, 1, 0, 1, 0, 1, 0 and "a standard chopper algorithm (sequence of + - repeated)" for the voltage reference 114, i.e. the Vref at the input of the DAC will be alternately Vref+Voff or Vref-Voff.

If the chopped reference voltage 114 is integrated with the serial bit stream 112a, the Vref component at the output of the integrator 556 will be: - (Vref+Voff) + (Vref-Voff) -(Vref+Voff) + (Vref-Voff) - (Vref+Voff) + (Vref-Voff) . . . = - n*Voff (after n samples). The offset component is not cancelled because the chopped offset is modulated by the bitstream. Similarly, the passage on page 11, lines 11 to 25 of D1 uses the example of logic levels 0, 1, 0, 1, 0, 1, 0, 1 for the serial bit stream 112a and a standard chopper algorithm for the voltage reference 114, in which case the Vref component at the output of the integrator 556 will be: + (Vref+Voff) - (Vref-Voff) + (Vref+Voff) - (Vref-Voff) + (Vref+Voff) - (Vref-Voff) . . . = + n*Voff (after n samples).

These two examples show that the integrated reference component at the output of the integrator is bitstream-dependent and can lead to very different results even with the same input voltage as soon as the bitstream varies. D1 teaches that this problem leads to major non-linearity issues in the transfer function of the

ADC and needs to be overcome when using chopped reference voltage sources.

The authors of D1 conclude on page 12, first three lines: "The two examples given herein above show the limitation of the standard chopper algorithm and clearly show the need of modulating the chopper algorithm with the bitstream in order to properly cancel the offset component with any incoming bitstream".

18.8 Page 18, lines 4 to 8 of D1 teaches that "[t]he chopper clock control 104a ensures that the chopper stabilized voltage reference 102 always is chopped (clock 116) such that there are an equal number of Vref = Vref + Voff and Vref = Vref - Voff during each sampling sequence of phases Pl and P2 correlated with the bit patterns from the serial bit stream 112a so that an equal number of + Voff and - Voff components cancel each other out".

18.9 The chopper clock 116 is synchronized with the sampling phase of the DAC output, i.e. the reference is sampled during phase Pl and transferred during phase P2 (page 18, lines 14 and 15). Page 19, lines 15 to 21 explains that "[t]he chopper clock control 104b ensures that there are an equal number of pairs of samples taken for each level asserted such that there are an equal number of Vref = Vref + Voff [....] and Vref = Vref - Voff during each sampling sequence of phases Pl and P2 correlated with the bit patterns from the serial bit stream 112b at each level [...] so that an equal number of + Voff and - Voff of the reference voltage samples occur and thereby canceled each other out after integration".

19. Feature (F2) specifies that "chopping of the chopped reference voltage generator is synchronized with the charge phase and the transfer phase".

19.1 D1 teaches that the chopper clock 116 is synchronized with the sampling phase of the DAC output. Here the reference is sampled during phase Pl and transferred during phase P2. So the chopper clock 116 only changes synchronously with the phase Pl. This synchronization is done by the latch 332 that latches the current chopper clock 116 during phase Pl (page 18, lines 14 to 17).

19.2 The board notes that if the skilled person considered using the standard chopping algorithm mentioned in D1 in the way described by features (F1) and (F2), in particular, a chopping synchronised with the charge and transfer phases, the skilled person would arrive at Table 2 reproduced in point 7. above.

19.3 However, neither D1 nor the acknowledge prior art of document D7, suggest providing two different switching patterns (A, B) by means of the switching sequencer, for at least one DAC input value. Document D7 mentions that the intermediate levels can be achieved through other switching sequences (column 4, lines 54 to 61), but not how this can be used to solve any problem. Instead, five switching patterns are selected to produce five distinct output voltages (see also page 15, first full paragraph of the present application). None of the other cited prior-art documents discloses feature (F3).

20. The board agrees with the appellant that the skilled person would not arrive at a solution comprising features (F1), (F2) and (F3). The solution proposed by

document D1 relies on modulating the chopper algorithm with the bitstream and not on providing two different switching patterns for at least one DAC input value as described in (F3). Therefore, the skilled person would not arrive at the combination of the three distinguishing features.

21. The board thus concludes that the claimed subject-matter is inventive over the acknowledged prior art disclosed in D7 in combination with the prior art considered in this case. The other prior-art documents considered in the proceedings are less relevant.

It follows that claim 1 and the corresponding method claim 8 satisfy the requirements of Article 56 EPC.

Further prosecution

22. In summary, the board finds that independent claims 1 and 8 of the appellant's request satisfy the requirements of the EPC. However, the dependent claims submitted during oral proceedings before the board may need to be adapted to the independent claims and the description and the drawings may need to be adapted to the claimed subject-matter before a patent can be granted.

23. The case is therefore to be remitted to the examining division, in accordance with Article 111 EPC, with the order to grant a patent based on independent claims 1 and 8 filed during the oral proceedings, dependent claims based on those filed during the oral proceedings before the board and adapted to independent claims 1 and 8, as well as the description and drawings adapted to the set of allowable claims.

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the examining division with the order to grant a patent on the basis of the following documents:
   - independent claims 1 and 8 as filed during the oral proceedings; and
   - dependent claims to be adapted;
   - description to be adapted.

The Registrar: The Chair:

S. Lichtenvort P. San-Bento Furtado

Decision electronically authenticated