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Datasheet for the decision of 17 December 2021

Case Number: T 2033/16 - 3.4.03

Application Number: 09831339.8

Publication Number: 2374122

IPC: G09G3/20, G09G3/32

Language of the proceedings: EN

Title of invention:
LOW POWER CIRCUIT AND DRIVING METHOD FOR EMISSIVE DISPLAYS

Applicant:
Ignis Innovation Inc.

Headword:

Relevant legal provisions:
EPC Art. 56, 123(2), 84
RPBA Art. 12(4)
RPBA 2020 Art. 13

Keyword:
Inventive step - main request (yes)

Decisions cited:

Catchword:

Europäisches Patentamt
European Patent Office
Office européen des brevets

Beschwerdekammern

Boards of Appeal

Chambres de recours

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Case Number: T 2033/16 - 3.4.03

D E C I S I O N
of Technical Board of Appeal 3.4.03
of 17 December 2021

Appellant: (Applicant)	Ignis Innovation Inc. 50 Bathurst Drive, Unit 12 Waterloo, Ontario N2V 2C5 (CA)
Representative:	Grünecker Patent- und Rechtsanwälte PartG mbB Leopoldstraße 4 80802 München (DE)
Decision under appeal:	**Decision of the Examining Division of the European Patent Office posted on 1 March 2016 refusing European patent application No. 09831339.8 pursuant to Article 97(2) EPC.**

Composition of the Board:

Chairman	G. Eliasson
Members:	A. Böhm-Pélissier
	C. Heath

Summary of Facts and Submissions

I. The appeal is against the decision of the Examining Division to refuse European patent application No. 09 831 339. The refusal was based on the ground of added subject-matter (Article 123(2) EPC) for the Main Request. The Auxiliary Request was not admitted under Rule 137(3) EPC.

II. The Appellant (Applicant) **requests** that the decision under appeal be set aside and that a patent be granted on the basis of the new Main Request, i.e.
Description: pages 1, 1a, 2-5 as filed with letter dated 26 November 2021, pages 7-38 as published (page 6 deleted),
Claims: 1-15 as filed with letter dated 26 November 2021,
Drawings: Sheets 1/30-30/30 as published,

or based on First or Second Auxiliary Request as filed with the statement of grounds of appeal. Oral Proceedings are requested in the event a patent cannot be granted on the basis of these requests.

III. Reference is made to the following documents:

D1 = WO 2006/128069 A2
D2 = US 2008/100543 A1
D3 = EP 1 439 520 A2

IV. Highlighting (additions/emphasis, **bold**, ~~deletions~~) and labelling in citations are added by the Board.

V. **Claim 1** of the **Main Request** (as filed in reaction to the communication of the Board under Article 15 RPBA 2020) reads:
(amendments with respect to the Main Request - onto which the impugned decision was based - are highlighted):

(A) A display system, comprising:
(B) a pixel circuit (24a, 44a, 64a, 84a) including a light emitting device (106),
(C) a driving transistor (102) for driving the light emitting device (106),
(D) the driving transistor (102) being coupled between a power supply (110) and the light emitting device (106),
(E) and a switch transistor (104) having a gate terminal, a first terminal and a second terminal,
(F) wherein one of the first and second terminals of the switch transistor is coupled to the gate terminal of the driving transistor (102) and the other one of the first and second terminals is connected to a common node (A01) of the driving transistor and the light emitting device;
(G) a gate driver (28, 48, 68, 88) adapted to drive the switch transistor (104) in the pixel circuit via an address line (30, 50, 70, 90) connected to the gate terminal of the switch transistor;
(H) a capacitor (14, 46, 86, 108) coupled between a data line (32, 52, 92) and a gate terminal of the driving transistor; and
(I) a ramp voltage generator (12) coupled to the data line and adapted to provide a time-variant voltage to the capacitor,
(J) where the capacitor converts the time-variant voltage to a current,
characterized by

(K) a controller (29, 49, 69, 89) adapted to control and schedule programming and driving of the pixel circuit by controlling the generation of the time-variant voltage in the ramp voltage generator and the operation of the gate driver such that:
(L2) during a first stage (122) of a programming cycle (120) of the pixel circuit, the ramp voltage generator provides the time-variant voltage to the capacitor and the address line (90) is operated to switch ~~while~~ the switch transistor (104) ~~is~~ on so that a bias current is provided by the capacitor ~~to the pixel via the data line~~ via the switch transistor; and
(M) during a second stage (124) of said programming cycle (120), applying a programming voltage to the data line while the switch transistor (104) is off so as to store said programming voltage in the capacitor;
(N) wherein the power supply (110) coupled to the driving transistor is low during the programming cycle (120).

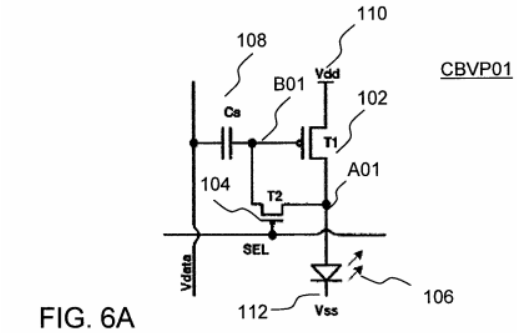


FIG. 6A

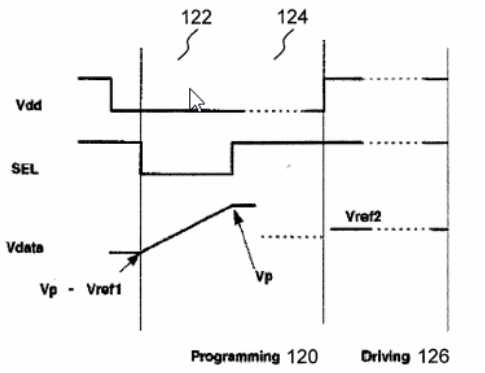


FIG. 6B

Application

VI. **Claim 13** of the Main Request reads:
(labelling in analogy to claim 1)

(K') A method of operating a pixel circuit (CBVP01)
(B') including a light emitting device (106),

(C') a driving transistor (102) adapted to drive the light emitting device,
(D') the driving transistor being coupled between a power supply (110) and the light emitting device (106),
(E') a switch transistor (104) coupled between a first node (A01) coupled to both the driving transistor and the light emitting device,
(F') and a second node (B01) coupled to the gate terminal of the driving transistor,
(H') and a storage capacitor (108) directly coupled between a data line (Vdata) and the second node (B01), the method comprising:
(L2') in a first stage (122) during a programming cycle (120) of the pixel circuit, ~~changing~~ providing a time variant voltage ~~provided~~ to the storage capacitor
(I') via a ramp voltage generator (12) coupled to the data line
(G') and operating the address line to switch the switch transistor on,
(J') the storage capacitor electrically coupling to the driving transistor while the switch transistor is turned on,
(L2'') such that a bias current is conveyed through the driving transistor, the switch transistor, and across the storage capacitor,
(L2''') to allow the gate terminal of the driving transistor to adjust to a bias voltage (VB) dependent on a function of the electrical characteristics of the driving transistor;
(M') and in a second stage (124) during the programming cycle (120), applying a programming voltage on the data line while the switch transistor is turned off, so as to store the programming voltage in the storage capacitor;
~~wherein the time variant voltage is provided via a ramp voltage generator (12) coupled to the data line~~

(N') and wherein the power supply (110) coupled to the driving transistor is low during the programming cycle (120).

Reasons for the Decision

1. The appeal is admissible.

2. **The invention as claimed**

2.1 Electro-luminance displays, such as liquid crystal displays (LCD), light emitting displays (LED) and in particular active-matrix organic light emitting diode (AMOLED) displays with amorphous silicon, need to be supplied with an accurate and constant drive current. However, the small drive current leads to a large parasitic capacitance and increases the settling time. Furthermore, there is a demand of continuously reducing the size and power consumption of the driver circuits.

2.2 The present invention aims to provide an improved driver circuit with an operation method that can improve the lifetime, image uniformity, stability and/or yield of the display, and can provide a high-resolution stable low power display (paragraphs [0003] and [0004] of the publication of the application).

2.3 This is achieved by sharing a current bias line with a voltage data line. In a first stage during a programming cycle a time variant voltage is provided to a capacitor via a ramp voltage generator, such that a bias current is conveyed through the driving transistor. In a second stage a programming voltage is applied on the same line while the switch transistor is turned off, so as to store the programming voltage in

the capacitor (the power supply coupled to the driving transistor is low during the programming cycle).

3. Main Request - Article 123(2) EPC

3.1 In claim 1 filed with the statement of grounds of appeal features (D) and (N) have been added. These amendments were reactions to the objections under Article 123(2) EPC in the impugned decision and therefore are admitted under Article 12(4) RPBA 2007. The features are based on Figs. 6A and 6B and paragraphs [0033], [0036] and [0037] of the description as originally filed.

3.2 Features (A)-(C), (E)-(K) and (M) have been added or reformulated during the first instance proceedings.

3.2.1 The amendments are based on original claims 1, 6, 17-21 and 27-28 of the original international application. The amendments are further based on Figs. 5, 6A and 6B and the corresponding description (paragraphs [0030] to [0038]). The amendments are further based on paragraphs [0016] to [0027], where the general concept of the invention is described.

3.2.2 The Examining Division objected that the amendments added new information, i.e. that (decision, section 7.1.3)

(a) the "switch transistor" might be turned on or off by means other than controlling the level of the SEL/address line connected to the gate terminal of the "switch transistor" e.g. by changing the voltage of the source and/or drain terminal relative to a constant voltage on the gate terminal of the "switch terminal";

(b) the power line V_{DD} might be active/on during both the first and second stage of the programming cycle;

(c) the controller so adapted could work with a pixel circuit which did not comprise a capacitor connected between the data line and the gate terminal of the driving transistor.

ad (a)

3.2.3 The Board however comes to the conclusion that the claim in Feature (G) clearly defines that a gate driver is adapted to drive the switch transistor in the pixel circuit via an address line connected to the gate terminal of the switch transistor. The description provides a sufficient basis for this amendment (see e.g. Fig. 6a, paragraph [0033], [0022]). The formulation "adapted to drive" clearly defines that the switch transistor is only driven via the address line and the gate terminal.

ad (b)

3.2.4 Objection (b) is overcome by newly added Feature (N) explicitly defining that the power supply coupled to the driving transistor is low during the programming cycle.

ad (c)

3.2.5 The claim defines that a capacitor is coupled between a data line and a gate terminal of the driving transistor (feature (H)) and that the ramp voltage generator provides the time-variant voltage to the capacitor so that a bias current is provided by the capacitor via the switch transistor (feature (L2)). Therefore the claim defines a capacitor connected between the data line and the gate terminal of the driving transistor.

3.2.6 Feature (L2):

This amendment was a reaction to an objection under Article 123(2) EPC in the communication according to Article 15 RPBA 2020 of the Board and therefore is admitted under Articles 12(4) RPBA 2007 and 13 RPBA 2020. Feature (L2) was amended as indicated in section V. This amendment was present in the Second Auxiliary Request and was considered allowable by the Board in its communication. It was specified that the bias current is provided via the switch transistor (instead of "to the pixel via the data line"). The ambiguous term "pixel" was therefore removed. This is directly and unambiguously disclosed in Fig. 6a and the corresponding description (e.g. paragraph [0036]).

3.3 Corresponding amendments have been performed in method claim 13. Claims 1 and 13 therefore comply with the requirements of Article 123(2) EPC.

4. Clarity

4.1 Removal of the ambiguous term "pixel" in feature (L2) establishes also compliance with the requirements of Article 84 EPC. The description has been adapted to the new independent claims. In particular on pages 3 to 5 the examples not being covered by the scope of amended independent claims 1 and 13 have been identified as such. D1 to D3 are now discussed in the description, claim 1 has been put into the two-part form.

5. Inventive Step – Article 56 EPC

5.1 Closest prior art

D2 is considered as closest prior art. It was introduced by the Examining Division during the examination procedure and discloses a pixel circuit and programming cycle similar to the present invention. D1 and D3 disclose pixel circuits being more remote.

5.2 Differences

5.2.1 D2 (reference signs according to D2) discloses (A) a display system, comprising (B) a pixel circuit (Fig. 11) including a light emitting device (38), (C) a driving transistor (31) for driving the light emitting device (38), (D) the driving transistor (31) being coupled between a power supply (12) and the light emitting device (38), and (E) a switch transistor (32) having a gate terminal (terminal connected to line 18), a first terminal (connected to capacitor 30 and the gate terminal of the driving transistor 31) and a second terminal.

FIG.11

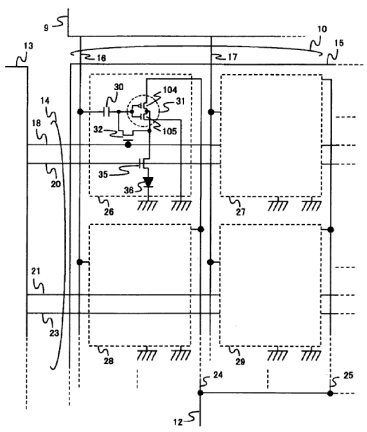
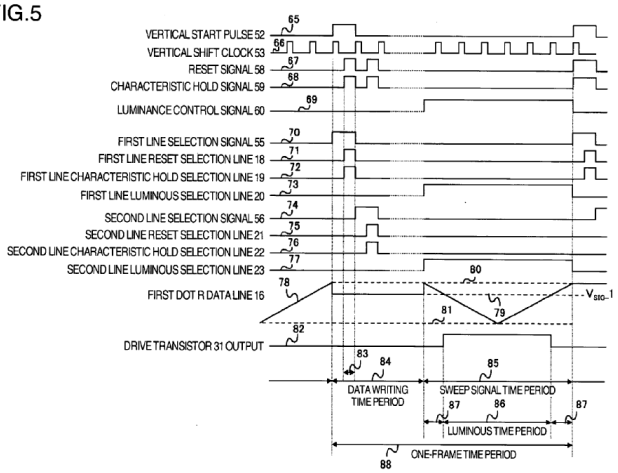


FIG.5



D2

5.2.2 Feature (F): D2 further discloses that a gate driver (driver driving address line 18) is adapted to drive

the switch transistor (32) in the pixel circuit via an address line (18) connected to the gate terminal of the switch transistor (32). D2 discloses that one of the first and second terminals of the switch transistor (32) is coupled to the gate terminal of the driving transistor (31), but D2 does not disclose that the other one of the first and second terminals is connected to a common node (feature (G)) of the driving transistor (31) and the light emitting device (38), because there is a switching transistor 35 arranged between the "common node" and the light emitting device (38).

5.2.3 Feature (L2): D2 discloses that during a first stage the voltage on line 16 ("period 78") is ramped up and the transistors are off, then at a second stage after the ramping, the select transistor 32 is briefly turned on to store the voltage in the capacitor. At the "period 85", the driving cycle, transistor 35 is turned on. In paragraph [0058] of D2 the "period 85" is called "sweep signal time period". "Period 84" is the "data writing time period". The ramp voltage 78 is before this period. At this period, all switching transistors are off. At the driving cycle 85 a ramping is done so that a longer luminous period for deteriorated OLED pixels can be achieved. D2 therefore discloses that during a first stage ("period 78") of a programming cycle of the pixel circuit, the ramp voltage generator provides a time-variant voltage to the capacitor (30). D2 however fails to disclose that during the first stage of the programming cycle the address line (18) is operated to switch the switch transistor (32) on so that a bias current is provided by the capacitor via the switch transistor. D2 therefore fails to disclose feature (L2).

5.2.4 Feature (M): D2 discloses that during a second stage (84 in Fig. 5) of said programming cycle (data writing time period 84) applying a programming voltage (*signal voltage from the first dot R data line 16*) to the data line and operating an address line (20) to switch the switch transistor (35) off so as to store said programming voltage in the capacitor (paragraph [0042]). D2 however fails to disclose that the address line (20) is "the" address line (18) coupled to "the" switch transistor (32). D2 therefore fails to disclose feature (M).

5.2.5 Feature (N): D2 further fails to disclose that the power supply (12) coupled to the driving transistor (31) is low during the programming cycle (Fig. 5 of D2). D2 therefore fails to disclose feature (N).

5.2.6 Claim 1 therefore differs from D2 in features (F), (L2) and (N), i.e. in that

(a) the current bias line and the address line are one and the same line,
(b) the programming and driving cycle are different;
(c) the power supply coupled to the driving transistor is low during the programming cycle.

5.2.7 In D2 the two switching transistors (32, 34, cf. Fig. 11) and capacitor 30 therefore apply different means for a different purpose/effect with respect to the present invention.

5.3 **Effect - Problem**

5.3.1 The effect of the difference is that the pixel current is independent of the variation of the driving transistor threshold and the electric carrier mobility. This is illustrated in Figures 7A and 7B of the

application: despite of varying the driving transistor threshold V_T and carrier mobility, the pixel current is stable for all gray scales.

5.3.2 According to paragraph [0004] of the present description this results in that the lifetime, image uniformity, stability and/or yield of the display is improved such that a high-resolution stable low power display can be provided.

5.3.3 The problem to be solved therefore is to improve lifetime, image uniformity and stability of the display and to provide a high-resolution stable low power display.

5.4 Non-Obviousness

5.4.1 In the present application the capacitor and the switching transistor have a different position and a different function than the capacitor and switching transistors in D2, i.e. in D2 two switching transistors are necessary for the two address/data lines (18, 20), while in the present application only one transistor/ line is used (this however requires that V_{dd} must be kept low during the programming cycle). In the present invention the capacitor is both a storage capacitor to store voltage programming information and a capacitive current source driver in conjunction with the ramp voltage generator. Bias current line and address/data line are shared. In D2 two separate lines (18, 20) are used. In D2 the time-variant voltage 78-81 on data line 16 during the driving cycle is a ramp-down - ramp-up voltage (similar to a Saw-toothed ramp), whereas in the application it is kept constant at Vref2. The programming in D2 is of a different type with respect to the present invention. D2 teaches bias current only

through the drive transistor 31 and a separate power supply line.

5.4.2 In detail, as shown by Fig. 5 of D2, the signal voltage 78 is applied before the data writing time period 84, i.e. before the writing signal voltage level V_{SIG}-1 is applied on the data line 16. The ramp voltage 78 in D2 is not applied during the data writing time period 84, i.e. where the programming data used to drive the electroluminescent organic element is written in the pixel circuit. Therefore, D2 does not teach applying a programming voltage to the data line during a second stage of the programming cycle, while the switch transistor is off so as to store the programming voltage in the capacitor.

5.4.3 As further shown by the operating scheme of Fig. 5 of D2, the ramp voltage 78 is applied to the data line 16 before the data writing time period 84 and while the switch transistors 32 to 35 are set to an off state by the first line reset selection line 18, the first line characteristic hold selection line 19, and the first line luminous selection line 20. Therefore, when the ramp voltage 78 is applied to the node of the capacitor 30 via the data line 16, the capacitor does not provide a continuous bias current to the pixel circuit since all switch transistors 32 to 35 are off. Therefore, D2 neither teaches nor hints at the idea of operating the switch transistors 32 and 35 to be in an ON state during the time period where the ramp voltage 78 is applied to the data line 16 for the purpose of using the capacitor as a capacitive current source for providing a bias current to the pixel circuit.

5.4.4 D2 therefore teaches a different concept of a pixel circuit. Nothing in D2 teaches to share the current

bias line and the voltage data line. D2 is also silent about achieving a bias current behaviour independent of the variation of the driving transistor threshold and the electric carrier mobility.

5.4.5 D1 and D3 cannot provide any further useful teaching because they relate to pixel driver circuit concepts being even more remote to the pixel driver concept proposed in the present invention.

5.4.6 Consequently, the subject-matter of claim 1 of the Main Request is inventive within the meaning of Articles 52(1) and 56 EPC.

5.5 **Claim 13** is related to a method of operating a pixel circuit and comprises the same features in terms of a method claim (see section VI.). Claims 2-12 and 14-15 depend upon claim 1 and 13 respectively. Hence, on the basis of the available prior art, the system defined by claims 1-12 would not be obvious to a person skilled in the art, and nor, by the same reasoning *mutatis mutandis*, would the method defined by claims 13-15. The claimed subject-matter therefore involves an inventive step within the meaning of Articles 52(1) and 56 EPC. As the Main Request is allowable First and Second Auxiliary Request do not need to be assessed.

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the department of first instance with the order to grant a patent in the following version:

   Description: pages 1, 1a, 2-5 as filed with letter dated 26 November 2021, pages 7-38 as published (page 6 deleted);

   Claims: 1-15 as filed with letter dated 26 November 2021,

   Drawings: Sheets 1/30-30/30 as published.

The Registrar: The Chairman:

S. Sánchez Chiquero G. Eliasson

Decision electronically authenticated