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Datasheet for the decision of 22 January 2020

Case Number: T 1264/16 - 3.5.07

Application Number: 07301367.4

Publication Number: 2037585

IPC: H03M7/00

Language of the proceedings: EN

Title of invention:
Method for notch filtering a digital signal, and corresponding electronic device

Applicants:
STMicroelectronics N.V.
STMicroelectronics SA

Headword:
Notch filter/STMICROELECTRONICS

Relevant legal provisions:
EPC Art. 56

Keyword:
Inventive step - (yes)

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Case Number: T 1264/16 - 3.5.07

D E C I S I O N
of Technical Board of Appeal 3.5.07
of 22 January 2020

Appellant: (Applicant 1)	STMicroelectronics N.V. WTC Schiphol Airport, Schiphol Boulevard 265 1118 BH Schiphol Airport Amsterdam (NL)
Appellant: (Applicant 2)	STMicroelectronics SA 29, Boulevard Romain Rolland 92120 Montrouge (FR)
Representative:	Hoffmann Eitle Patent- und Rechtsanwälte PartmbB Arabellastraße 30 81925 München (DE)
Decision under appeal:	**Decision of the Examining Division of the European Patent Office posted on 25 January 2016 refusing European patent application No. 07301367.4 pursuant to Article 97(2) EPC**

Composition of the Board:

Chairman	R. Moufang
Members:	R. de Man
	C. Barel-Faucheux

Summary of Facts and Submissions

I. The applicants (appellants) appealed against the decision of the Examining Division refusing European patent application No. 07301367.4.

II. The decision cited the following documents:

D1: WO 96/15585 A, published on 23 May 1996;

D2: S. Luschas et al.: "Radio Frequency Digital-to-Analog Converter", IEEE Journal of Solid-State Circuits, Vol. 39, No. 9, September 2004, pp. 1462-1467.

The Examining Division decided that claim 1 of the main request (corresponding to the application as filed) and of the first and second auxiliary requests was unclear and that the subject-matter of the independent claims of the main request and claim 1 of the first and second auxiliary requests lacked inventive step in view of document D1.

III. The following additional documents were cited in the European search report:

D3: J. Rode at al: "Transmitter Architecture Using Digital Generation of RF Signals", Proceedings of the Radio and Wireless Conference 2003, August 2003, pp. 245-248;

D4: D. Ribner: "Multistage Bandpass Delta Sigma Modulators", IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing, Vol. 41, No. 6, June 1994, pp. 402-405;

D5: S. Taleie et al.: "A Bandpass ΔΣ RF-DAC with Embedded FIR Reconstruction Filter", 2006 IEEE International Solid State Circuits Conference - Digest of Technical Papers, pp. 2370-2379;

D6: WO 2005/015752 A, published on 17 February 2005.

IV. In their statement of grounds of appeal, the appellants maintained the requests considered in the decision under appeal as the main request and the second and fourth auxiliary requests, and filed new first, third and fifth to eleventh auxiliary requests. They filed copies of the claims of all the requests.

V. In a communication accompanying the summons to oral proceedings, the Board raised objections under Article 84 EPC and expressed the preliminary opinion that the subject-matter of claim 1 of all the requests lacked inventive step over document D1.

VI. In a letter dated 17 December 2019, the appellants filed an amended set of claims of a twelfth auxiliary request.

VII. During oral proceedings held on 22 January 2020, the appellants replaced their requests with a new sole substantive request. At the end of the oral proceedings, the chairman pronounced the Board's decision.

VIII. The appellants requested that the decision under appeal be set aside and that a patent be granted in the following version:

- Description: pages 1 and 3 to 9 of the description as originally filed, and pages 2 and 2a as submitted in the oral proceedings;

- Claims: claims 1 to 9 as submitted in the oral proceedings;
- Drawings: sheets 1/7 to 7/7 as originally filed.

IX. Claim 1 of the sole request as submitted in the oral proceedings reads as follows:

"Electronic device, comprising

sigma-delta modulation means (SDM) adapted to operate with a clock signal and having output means adapted to deliver a digital data signal,

first means (PLL) adapted to deliver a radiofrequency transposition signal,

and a notch filter including at least two identical radiofrequency digital to analog conversion blocks (RDCi),

each radiofrequency digital to analog conversion block having first input means coupled to said output means,

second input means adapted to receive said radiofrequency transposition signal

and second output means adapted to deliver a radiofrequency analog signal (ARFSi),

the notch filter furthermore including digital delay means (DM) controlled by said clock signal and including a delay block connected between the two first input means,

the first input means of a first radiofrequency digital to analog conversion block being directly connected to said output means,

the first input means of the second radiofrequency digital to analog conversion block being connected to said output means through said delay block,

the frequency of a notch of said notch filter being related to the delay value of the delay block,

and the notch filter furthermore including summation means (SM) adapted to sum said radiofrequency analog signals (ARFSi);

wherein the delay value is smaller than 1/(10*BW), where BW is the frequency bandwidth of the summed radio frequency analog signal."

Claims 2 to 5 are directly or indirectly dependent on claim 1.

Claim 6 reads as follows:

"Wireless apparatus, including an electronic device according to any one of the preceding claims."

Claim 7 reads as follows:

"Method for notch filtering a digital signal delivered by sigma-delta modulation means operating with a clock signal to obtain said digital signal, comprising

delaying (40) said digital signal using said clock signal for obtaining at least one delayed digital signal,

processing (41) said digital signal and said delayed digital signal with an identical processing including a radiofrequency transposition and a digital to analog conversion for respectively obtaining radiofrequency analog signals, and

summing (42) all said radiofrequency analog signals;

the frequency of a notch of said notch filtering being related to the delay value,

wherein the delay value is smaller than 1/(10*BW), where BW is the frequency bandwidth of the summed radio frequency analog signal."

Claims 8 and 9 are directly or indirectly dependent on claim 7.

Reasons for the Decision

1. The appeal complies with the provisions referred to in Rule 101 EPC and is therefore admissible.

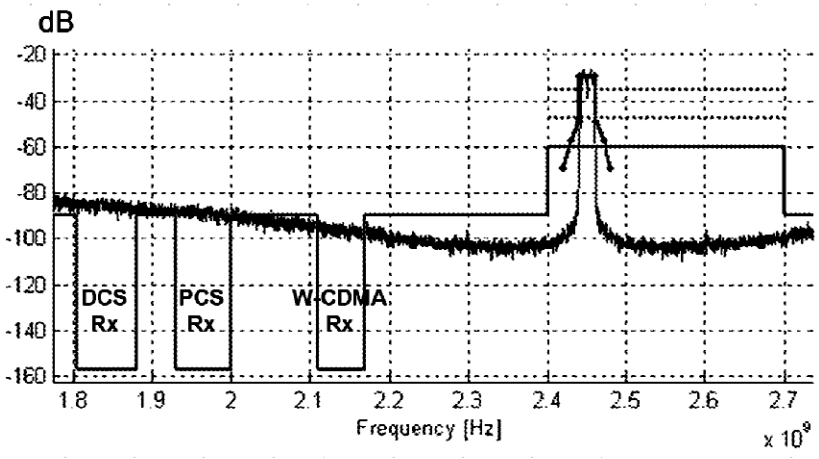
2. *The invention*

2.1 The invention relates to the use of notch filtering to reduce the quantisation noise in certain frequency bands of digital signals delivered by sigma-delta modulation means. This is useful in a wireless apparatus that operates two or more radio systems simultaneously.

2.2 As explained in the application's description on page 1, lines 21 to 26, and on page 6, lines 12 to 22,

with reference to Figures 1 and 2, sigma-delta modulation can be used in digital transmitters to push the quantisation noise that results from digital-to-analog conversion away from, for example, the Wi-Fi emission band. However, in a mobile phone this can cause the quantisation noise to pollute the DCS, PCS or W-CDMA bands:

FIG.2



PRIOR ART

2.3 The invention proposes reducing the quantisation noise in critical frequency bands by applying a notch filter. This notch filter is implemented by combining the sigma-delta modulated and RF-transposed signal with a delayed copy of the same signal. The frequency of a notch of the filter is inversely proportional to the duration of the delay. For the notch to be placed far away from the emission band, e.g. several hundreds of MHz away from the Wi-Fi emission band, the delay needs to be small relative to the inverse of the width of the emission band.

2.4 This is achieved by the electronic device of claim 1, which comprises:

- sigma-delta modulation means (SDM);

- first means (PLL); and
- a notch filter.

The sigma-delta modulation means (SDM) is adapted to operate with a clock signal and has output means adapted to deliver a digital data signal.

The first means (PLL) is adapted to deliver a radiofrequency (RF) transposition signal.

The notch filter includes:
- at least two identical RF digital-to-analog conversion (DAC) blocks;
- digital delay means; and
- summation means.

Each RF DAC block has:
- first input means coupled to the output means;
- second input means adapted to receive the RF transposition signal; and
- second output means adapted to deliver an RF analog signal (ARFSi).

The digital delay means is controlled by the clock signal and includes a delay block.

The first input means of the first RF DAC block is directly connected to the output means of the sigma-delta modulation means. The first input means of the second RF DAC block is connected to the output means of the sigma-delta modulation means through the delay block of the digital delay means. As a result, the delay block is "connected between the two first input means".

The summation means is adapted to sum the RF analog signals (ARFSi).

The frequency of a notch of the notch filter is related to the delay value of the delay block, which is smaller than 1/(10*BW), where BW is the frequency bandwidth of the summed RF analog signal.

2.5 Since the delay value of the delay block is a multiple of the period of the clock signal, the feature specifying that the delay value is smaller than 1/(10*BW) implies a lower limit on the clock frequency at which the sigma-delta modulation means operates.

3. *Added subject-matter - Article 123(2) EPC*

3.1 Claim 1 is based on original claim 1 with the following amendments taken from the description and drawings as originally filed:

The first input means of the first RF DAC block is directly connected to the output means of the sigma-delta modulation means, and the first input means of the second RF DAC block is connected to the output means of the sigma-delta modulation means through the delay block (see page 7, lines 3 to 6, and Figure 3).

The delay value of the delay block is smaller than 1/(10*BW), where BW is the frequency bandwidth of the summed RF analog signal (page 4, lines 3 to 6).

3.2 Independent method claim 7 is based on original claim 7 with the added feature that the delay value of the delay block is smaller than 1/(10*BW), where BW is the frequency bandwidth of the summed RF analog signal (page 4, lines 3 to 6).

3.3 Claims 2 to 6, 8 and 9 correspond to original claims 2 to 6, 8 and 9.

3.4 Hence, the claims of the sole substantive request comply with Article 123(2) EPC.

4. *Clarity - Article 84 EPC*

4.1 The clarity objections raised in the Board's communication no longer apply to the current set of claims.

4.2 In particular, claim 1 now clearly expresses the relationships between the "electronic device", the "sigma-delta modulation means", the "first means", the "notch filter" and the "output means".

4.3 Moreover, the amendments made to claim 1 have clarified the feature "a delay block connected between the two first input means".

4.4 The claims of the sole substantive request therefore meet the requirements of Article 84 EPC.

5. *Inventive step - Article 56 EPC*

5.1 Document D1 relates to an I/Q modulator for an RF transmitter (see title and abstract). Figure 5 shows an I/Q modulator 150, which includes first (156, 135) and second (154, 135) sigma-delta DACs (abstract; page 9, line 11, to page 11, line 11). Figure 2 shows an implementation of a sigma-delta DAC (page 6, line 29, to page 7, line 22).

According to the description on page 8, lines 10 and 11, Figure 3 shows a notch filter that is adapted for use with a sigma-delta DAC. According to the description on page 5, lines 34 to 36, Figure 3 shows an arrangement for adding a notch-filter response to the output of a sigma-delta DAC.

5.2 The description of Figure 3 in document D1 does not state what block 54 represents. As explained below, the Board does not agree with the Examining Division that block 54 is a sigma-delta DAC in the sense of a circuit that converts a digital signal into an analog signal.

5.3 The sigma-delta DAC of Figure 2 consists of a sigma-delta modulator comprised of blocks 11, 12, 13 and 21 and a low-pass filter 15, as described on page 6, line 29, to page 7, line 22. Although document D1, on page 7, lines 12 to 14, refers to the signal 22 produced by the adder 21 as "the DAC output", it is evident that the output of the circuit consisting of blocks 11, 12, 13 and 21 is not an analog signal, but rather a digital signal representing the result of sigma-delta modulation that is yet to be converted to an analog signal by the low-pass filter 15. Indeed, the passage on page 6, lines 10 to 16 confirms that the low-pass filter converts "the digital output D0", which "toggles at a rate much higher than the bandwidth of the analogue signal to be generated" to obtain the analog output waveform 19.

5.4 Figure 3 is a variation on Figure 2 and shows a sigma-delta DAC that incorporates a notch-filter response. Block 54 corresponds to the sigma-delta modulator implemented in blocks 11, 12, 13 and 21 of Figure 2. The output of the modulator is connected directly to the output buffer 34 and indirectly, via the delay

shift register 30, to the output buffer 33 (see page 8, lines 15 to 20). Just as the digital output D0 in Figure 2 is converted to an analog signal by the low-pass filter 15 (page 6, lines 7 to 22), so are the digital outputs of the output buffers 33 and 34 summed and converted to an analog signal by the reconstruction filter 35 (page 8, lines 20 and 21). This combined delay and sum action results in a notch-filter response, with the frequency of the notch being related to the delay of the shift register (page 8, lines 21 to 24).

5.5 The description of the proposed I/Q modulator on page 3, line 24, to page 5, line 12, confirms this understanding. In particular, the passage on page 5, lines 1 to 9, confirms that each sigma-delta DAC includes a notch-filter arrangement and a reconstruction-filter arrangement (see also original claim 5 on page 13). The fact that the output signals 129 and 131 of blocks 154 and 156 in Figure 5 are digital output signals is also clear from page 10, lines 21 to 36.

5.6 The I/Q modulator depicted in Figure 5 includes first (154, 129, 130, 135) and second (156, 131, 132, 135) copies of the sigma-delta DAC shown in Figure 3, the first copy being applied to the Q component of the I/Q signal and the second copy being applied to the I component. Each sigma-delta DAC is connected to an RF modulator (164, 166) which combines the output of the sigma-delta DAC (163, 165) with an RF transposition signal 160 (page 9, line 36, to page 10, line 3; page 10, line 34, to page 11, line 7).

5.7 Hence, document D1 discloses an electronic device including a sigma-delta DAC as shown in Figure 3, which

comprises a sigma-delta modulation means in the form of block 54 and a notch filter in the form of blocks 30 and 35.

The sigma-delta modulation means is adapted to operate with the clock signal 20 and has output means adapted to deliver a digital data signal.

The notch filter comprises:
- a DAC block in the form of the reconstruction filter 35; and
- digital delay means in the form of the delay shift register 30.

The reconstruction filter 35 has:
- a first "first input means" directly coupled to the output means of the sigma-delta modulation means;
- a second "first input means" coupled to the output means of the sigma-delta modulation means via the digital delay means;
- second output means adapted to deliver the analog signal 39.

The reconstruction filter 35 includes summation means adapted to sum the analog signals.

The digital delay means 30 is controlled by the clock signal 20 and includes a delay block connected between the two first input means.

The frequency of a notch of the notch filter is related to the delay value of the delay block.

As shown in Figure 5, the electronic device also includes means 160 adapted to deliver an RF transposition signal. The RF modulator 164 receives

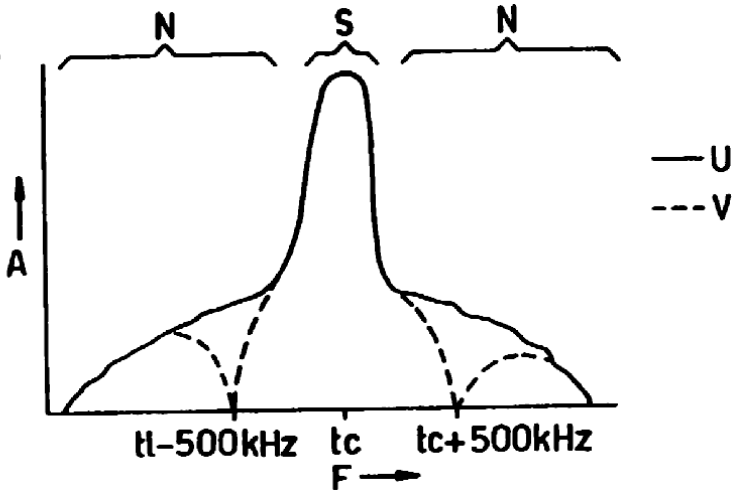
both the RF transposition signal and the analog output 163 of the first copy of the sigma-delta DAC, and performs an RF transposition to deliver an analog RF signal.

5.8 The subject-matter of claim 1 differs from the disclosure of document D1 in that:

- the reconstruction filter 35 (corresponding to the bottom half of the reconstruction filter 135 in Figure 5) and the RF modulator 164 are replaced with two identical RF DACs and a summation means that sums the analog outputs of both RF DACs; and
- the delay value is smaller than 1/(10*BW), where BW is the frequency bandwidth of the summed RF analog signal.

5.9 These differences allow the notch of the filter to be placed far away from the frequency band of the RF analog signal because, in the device of document D1, the reconstruction filter and the delay element produce a notch filter with notches placed close to the carrier frequency to achieve a filtered signal V that, compared with the unfiltered signal U, falls off rapidly to zero at either side of the carrier frequency, as shown in Figure 4 and described on page 8, line 30, to page 9, line 10:

Fig.4.



5.10 Unlike the present application, document D1 does not envisage using the notch filter to reduce quantisation noise in other emission bands far away from the carrier frequency. It therefore does not envisage very small delay values and a corresponding lower limit on the frequency at which the sigma-delta modulation means operates (see point 2.5 above).

5.11 Moreover, starting from the disclosure of document D1 and faced with the problem of reducing quantisation noise in emission bands far away from the carrier frequency, the skilled person would not find any suggestion in the cited prior art to modify the notch filter in document D1 in the claimed manner in order to direct it to a different purpose. Indeed, document D2 was cited by the Examining Division and documents D3, D5 and D6 were cited in the application as filed to show that RF DAC blocks were well known to the skilled person. And document D4 relates to an architecture for analog-to-digital conversion rather than digital-to-analog conversion (see abstract).

5.12 The subject-matter of device claim 1 and its dependent claims 2 to 5 therefore involves an inventive step. By the same reasoning, the same applies to the subject-matter of apparatus claim 6 and method claim 7. Hence, the sole substantive request meets the requirements of Articles 52(1) and 56 EPC.

6. *Conclusion*

Since, moreover, the description has been adapted, the sole substantive request complies with the EPC. The appeal therefore succeeds.

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the department of first instance with the order to grant a patent on the basis of the following documents:
   - Description: pages 1 and 3 to 9 of the description as originally filed, and pages 2 and 2a as submitted in the oral proceedings;
   - Claims: claims 1 to 9 as submitted in the oral proceedings;
   - Drawings: sheets 1/7 to 7/7 as originally filed.

The Registrar: The Chairman:

A. Nielsen-Hannerup R. Moufang

Decision electronically authenticated