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Datasheet for the decision of 15 April 2020

Case Number: T 0450/16 - 3.4.03

Application Number: 06821723.1

Publication Number: 2080228

IPC: H01L29/423, H01L29/778, H01L29/40, H01L29/417

Language of the proceedings: EN

Title of invention:
SINGLE VOLTAGE SUPPLY PSEUDOMORPHIC HIGH ELECTRON MOBILITY TRANSISTOR (PHEMT) POWER DEVICE AND PROCESS FOR MANUFACTURING THE SAME

Applicant:
Selex Sistemi Integrati S.p.A.

Headword:

Relevant legal provisions:
EPC Art. 56, 84, 123(2)

Keyword:
Amendments - allowable (yes)
Claims - clarity (yes)
Inventive step - (yes)

This datasheet is not part of the Decision.
It can be changed at any time and without notice.

Decisions cited:

Catchword:

This datasheet is not part of the Decision
It can be changed at any time and without notice

Beschwerdekammern

Boards of Appeal

Chambres de recours

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Case Number: T 0450/16 - 3.4.03

D E C I S I O N
of Technical Board of Appeal 3.4.03
of 15 April 2020

Appellant: (Applicant)
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Decision under appeal: **Decision of the Examining Division of the European Patent Office posted on 24 September 2015 refusing European patent application No. 06821723.1 pursuant to Article 97(2) EPC.**

Composition of the Board:

Chairman G. Eliasson
Members: A. Böhm-Pélissier
C. Heath

Summary of Facts and Submissions

I. The appeal is against the decision of the Examining Division to refuse European patent application No. 06 821 723. The refusal was based on the ground of lack of inventive step (Article 56 EPC).

II. The Appellant (Applicant) requests that the decision under appeal be set aside and that a patent be granted based on the following version:

Description, pages 1-16, as filed with letter dated 11 February 2020;
Claims 1-33, as filed with letter dated 7 April 2020;
Drawings 1/3-3/3 as published

or alternatively on the basis of the First Auxiliary Request and Second Auxiliary Request filed with the statement of grounds of appeal.

III. In its communication the Board objected to a lack of essential features. The Board was of the opinion that in order to make the pseudomorphic high electron mobility transistor operable in the Ka band as a single voltage transistor the feature that the first electron supply layer has a lower doping concentration than the second electron supply layer (Feature labelled below with (B)) was essential.

IV. Reference is made to the following two documents cited in the decision under appeal:

D1 = US 2002/024057 A1
D2 = US 2003/122152 A1

V. **Claim 1** of the Main Request reads (Board's labelling):

(A1) A Ka Band,
(A2) single-voltage supply
(A3) pseudomorphic high electron mobility transistor (PHEMT) power device (1; 1'; 1") comprising:
- a semi-insulating substrate (2); an epitaxial substrate (3) formed on the semi-insulating substrate (2); the epitaxial substrate (3) comprising a buffer layer (10), a superlattice layer (11), a first electron supply layer (12, 13), a first spacer layer (14), an electron transit layer (15), a second spacer layer (16), a second electron supply layer (17), a Schottky layer (18), and a contact layer (19) sequentially stacked on the semi-insulating substrate (2); wherein
(B) the first electron supply layer (12, 13) has a lower doping concentration than the second electron supply layer (17);
- source and drain electrodes (4, 5) formed on, and in ohmic contact with the contact layer (19); and a gate electrode (6) formed on the Schottky layer (18) to extend through the contact layer (19); wherein the contact layer (19) comprises:
(C) a lightly doped contact layer (20) formed on the Schottky layer (18); and
(D) a highly doped contact layer (21) formed on the lightly doped contact layer (20),
(E) and having a doping concentration higher than the lightly doped contact layer (20);
- wherein the PHEMT power device (1) further comprises: a wide recess (23) formed to penetrate the highly doped contact layer (21) so as to expose a surface of the lightly doped contact layer (20); and a narrow recess (24) formed in the wide recess (23) to penetrate the lightly doped contact layer (20) so as to expose a surface of the Schottky layer (18); wherein the gate

electrode (6) is formed in the narrow recess (24) and in Schottky contact with the Schottky layer (18) to extend from the exposed surface of the Schottky layer (18) through the lightly and highly doped contact layers (20, 21); and wherein the source and drain electrodes (4, 5) are formed on, and in ohmic contact with the highly doped contact layer (21) outside the wide recess (23) so that the wide recess (23) is arranged between the source and drain electrodes (4, 5).

VI. Independent method **Claim 16** reads (Board's labelling):
A process for manufacturing
(A1) a Ka-band,
(A2) single-voltage supply
(A3) pseudomorphic high electron mobility transistor (PHEMT) power device (1; 1'; 1") comprising:
providing a semi-insulating substrate (2);
forming an epitaxial substrate (3) on the semi-insulating substrate (2), wherein forming an epitaxial substrate (3) comprises sequentially stacking a buffer layer (10), a superlattice layer (11), a first electron supply layer (12, 13), a first spacer layer (14), an electron transit layer (15), a second spacer layer (16), a second electron supply layer (17), a Schottky layer (18), and a contact layer (19) on the semi-insulating substrate (2);
(B) wherein the first electron supply layer (12, 13) has a lower doping concentration than the second electron supply layer (17);
- forming source and drain electrodes (4, 5) on, and in ohmic contact with the contact layer (19); and
forming a gate electrode (6) on the Schottky layer (18) to extend through the contact layer (19);
wherein forming a contact layer (19) comprises:

(C) forming a lightly doped contact layer (20) on the Schottky layer (18);
(D) forming a highly doped contact layer (21) on the lightly doped contact layer (20) and
(E) having a doping concentration higher than the lightly doped contact layer (20);
- wherein the manufacturing process comprises:
forming a wide recess (23) to penetrate the highly doped contact layer (21) so as to expose a surface of the lightly doped contact layer (20); and
forming a narrow recess (24) in the wide recess (23) to penetrate the lightly doped contact layer (20) so as to expose a surface of the Schottky layer (18);
wherein the gate electrode (6) is formed in the narrow recess (24) and in Schottky contact with the Schottky layer (18) to extend from the exposed surface of the Schottky layer (18) through the lightly and highly doped contact layers (20, 21); and
the source and drain electrodes (4, 5) are formed on, and in ohmic contact with the highly doped contact layer (21) outside the wide recess (23) so that the wide recess (23) is arranged between the source and drain electrodes (4, 5).

Reasons for the Decision

1. Admissibility of the Appeal

The Appeal is admissible.

2. The Claimed Invention

2.1 The claimed invention relates to a pseudomorphic high electron mobility transistor (PHEMT) which is operable in the Ka band, i.e. in the frequency range of 26.5-40 GHz. In addition to the relatively high frequencies the PHMET is aimed to be operable as single voltage transistor.

2.2 The following features achieve the desired effect:

2.2.1 The formation of a doped contact layer made up of a lower lightly doped lower contact layer and an upper highly doped lower contact layer in ohmic contact with the source and drain electrodes allows the contact resistance in between to be lowered, thus improving voltage characteristics of the PHEMT (see application, page 14, lines 8-17).

2.2.2 Additionally, the formation of a double recess structure made up of an upper wide recess formed in the upper highly doped contact layer and of a lower narrow recess formed in the lower lightly doped contact layer allows for the ohmic contact to be placed on the highly doped contact layer thus improving the overall power characteristics of the PHEMT, in particular significantly increasing the breakdown voltage while maintaining a low knee voltage, and improving linearity and power-added efficiency (see application, page 14, lines 18-27).

2.2.3 Moreover, the combination of the double recess structure with the lightly and highly doped contact layers allows the PHEMT power device to operate with a single voltage supply, without any need for a negative bias voltage to the gate contact (see application, page 14, lines 28-32).

2.2.4 Further, the doping characteristics of the silicon layers makes the transconductance of the PHEMT power device invariant with respect to gate-to-source voltages while the lightly doped layer ensures etching uniformity in wet recess etching performed to manufacture the PHEMT power device, thus making the overall manufacturing process for the PHEMT power device easy and hence improving the productivity (see application, page 15, lines 1-9).

2.2.5 Finally, the claimed T-gate structure allows gate-to-source capacitance and gate finger resistance to be significantly reduced, allowing the PHEMT to achieve operating frequencies up to 40 GHz (see application, page 15, lines 10-13).

3. Amendments - Article 123(2) EPC

3.1 The following amendments have been made to the independent claims to overcome the clarity objections of the Examining Division (cf. point 4 below; striking through and underlining added by the board): "A (process for manufacturing a) Ka Band, single-voltage supply pseudomorphic high electron mobility transistor (PHEMT) power device (1; 1 '; 1 ") ~~designed to operate up to the Ka frequency band~~".

3.2 Feature (B) added in reply to the communication of the Board has a basis on page 15, line 1-3, and meets the requirements of Article 123(2) EPC. The description has been adapted to the claims, and prior art document D2 has been cited in the description.

3.3 The Board therefore is of the opinion that the application documents meet the requirements of Article 123(2) EPC.

4. Clarity - Article 84 EPC

4.1 The Examining Division objected that in claim 1 the expression Ka band was a result to be achieved without claiming the structural features behind this result.

4.2 In the present claim set all the features which are necessary for achieving that the PHEMT is operable in the Ka band have now been defined. The Ka frequency band is well defined and covers the range of 26.5-40 GHz. The Board therefore is of the opinion that by the amendments described in the previous section the clarity objections of the Examining Division have been overcome.

4.3 Feature (B) added in reply to the communication of the Board has overcome the objection of lack of essential features.

4.4 The Board therefore is of the opinion that the claims comply with the requirements of Article 84 EPC.

5. Inventive Step

5.1 Closest Prior Art

5.1.1 D2 discloses a single voltage PHEMT with a structure very similar to the structure defined in claim 1. D1 discloses a PHEMT with a structure similar to the structure defined in claim 1, but fails to disclose a superlattice structure.

5.1.2 The Appellant argued with respect to D1 that it failed to disclose a single-voltage supply PHEMT, namely a PHEMT where in operation the gate and source electrodes are both grounded, and to contain any hint whatsoever that could lead a skilled reader to consider grounding the gate electrode so as to result in the PHEMT operating with a single voltage supply.

5.1.3 The Appellant further argued that the provision of single-voltage supply PHEMTs, where the control gates are grounded, resulted in the saving of a gate electric biasing line for each PHEMT in each T/R Module, which in turn resulted in a significant reduction in area occupancy and integration/wiring/connection complexity.

5.1.4 The Board notes that D1 discloses a multi-voltage supply PHEMT where the source is grounded, a positive Vds is applied to the drain, and a negative Vgs is applied to the gate (see paragraphs [0061] and [0150]).

5.1.5 Hence D1 discloses a transistor for a different mode of operation. This implies structural differences between the PHEMT of D1 and a PHEMT as claimed used in such a way that the source and the gate are connected to ground in operation. The single-voltage supply operation of the PHEMT involves a purposive design of the PHEMT in terms of structural parameters such as barrier thickness and cap-layers doping levels.

5.1.6 The PHEMT disclosed in D1 therefore is of a different type such that the embodiments described in D1 are less suitable starting points than the embodiments described in D2, which discloses a single voltage supply PHEMT. For these reasons, D2 is chosen as closest prior art.

5.2 Difference

5.2.1 D2 discloses in Figure 1 and paragraphs [0030]-[0038] a single voltage PHEMT with a structure very similar to the structure defined in claim 1. D2 however fails to meet the claimed limitation relating to the achievable Ka frequency band, i.e. a purposive design of the PHEMT in order for it to operate efficiently up to operating frequencies that may be as high as 40 GHz. D2 only discloses in paragraph [0053] 5.75 GHz, which is well below the claimed Ka frequency band of 26.5-40 GHz. The Board agrees with the Appellant that the claimed frequency range of the PHEMT is a limiting feature of the PHEMT.

5.2.2 D2 further discloses an undoped contact layer (layer 32) instead of a lightly doped contact layer. Further more, D2 discloses a metallic contact layer (layer 42, 44) instead of a highly doped (semiconductor) contact layer.

5.2.3 D2 also does not disclose Feature (B), i.e. that the first electron supply layer (layer 20) has a lower doping concentration than the second electron supply layer (layer 28).

5.2.4 D2 therefore does not disclose the following Features:
(A1) Ka Band (i.e. purposive design of the PHEMT in order for it to operate efficiently in the range of 26.5-40 GHz);
(B) the first electron supply layer has a lower doping concentration than the second electron supply layer;
(C) a lightly doped contact layer;
(D) a highly doped contact layer;

(E) the highly doped contact layer having a doping concentration higher than the lightly doped contact layer.

5.2.5 In the decision under appeal, the Examining Division also argued starting from D1 as closest prior art. D1 discloses in Figure 1 and paragraphs [0057]-[0066] a single voltage PHEMT with a structure very similar to the structure defined in claim 1. D1 however fails to disclose a single voltage transistor and that the PHEMT is operable in the Ka frequency band.

5.2.6 D1 also does not disclose Feature (B), i.e. that the first electron supply layer has a lower doping concentration than the second electron supply layer. D1 further fails to disclose a superlattice layer between the buffer layer and the first electron supply layer. D1 is completely silent about a superlattice layer.

5.2.7 D1 therefore discloses all the features of claim 1 except Features (A1), (A2), (B) and a superlattice layer.

5.2.8 A reasoning starting from D1 however is, as discussed above, a less promising springboard for the problem-solution-approach, because D1 does not disclose a single voltage transistor.

5.3 Effect

Features (B)-(E) have the effect that the PHEMT is operable in the Ka frequency band (Feature (A1)).

5.4 Problem

The problem may therefore be formulated as how to adapt the PHEMT disclosed in D2 to be effectively operable in the Ka band.

5.5 Obviousness

5.5.1 The Board is of the opinion that the subject-matter of claim 1 of the Main Request is inventive:

5.5.2 In the appealed decision, the Examining Division argued that it was well known and accepted that highly doped semiconductor layers and metal layers may replace one another. The wording "single voltage supply" PHEMT concerned a method of operating and not a structural feature of a PHEMT.

5.5.3 The Board is of the opinion that in order to arrive at Features (C)-(E) the skilled person would inter alia have to implement the layer properties of contact layers 120 and 122 of D1 into the layers 32, 42 and 44 in D2. However, no incentive is given neither in D1, nor in D2 nor by the objective technical problem to be solved. There is no hint in the prior art that contact layers with the property of the layers 120 and 122 would improve the suitability of a PHEMT transistor to be operable in the Ka Band, because these layers have a different purpose.

5.5.4 Furthermore, the PHEMT of D1 has a different layer structure with respect to the PHEMT of D2. The PHEMT of D1 for example does not have a superlattice layer. This further teaches away from using the teachings of D1.

5.5.5 If the skilled person would nevertheless implement Features (C)-(E) relating to the structure of the contact layer, they would still not achieve Feature (B), i.e. that the first electron supply layer has a lower doping concentration than the second electron supply layer. D1 and D2 neither disclose nor teach Feature (B). Combining the teachings of D1 and D2 would therefore not result in a combination of features comprising the feature that the first electron supply layer has a lower doping concentration than the second electron supply layer.

5.5.6 D2 teaches exactly the opposite, i.e that the first electron supply layer has a higher doping concentration than the second electron supply layer (underlining added by the board): "*[0031] The first doped silicon layer 20 has a higher doping concentration than the second doped silicon layer 28. It is preferable that the doping concentration of the first doped silicon layer 20 is twice that of the second doped silicon layer 28*". Against this teaching the skilled person would not invert the concentration of the layers 20 and 28.

5.5.7 A reasoning starting from D1 (no single voltage transistor) as closest prior art would not lead to a different result. For the same reasons as stated above, the skilled person faced with the task of modifying the device of D1 for single voltage use would not consider modifying the contact layers such that the first electron supply layer would have a lower doping concentration than the second electron supply layer.

5.5.8 Consequently, the Board is of the opinion that the subject-matter of claim 1 is inventive over the teachings of D1 and D2.

6. **Other Claims**

Claim 16 relates to a process for manufacturing the device defined in claim 1. Since claim 16 has the same distinguishing features as claim 1, in particular Features (B)-(E), the reasoning for claim 1 applies also for claim 16. All other claims depend upon claim 1 or claim 16. Consequently, the subject-matter of claims 1-34 is inventive.

Order

For these reasons it is decided that:

The decision under appeal is set aside.

The case is remitted to the Examining Division with the order to grant a patent in the following version:

Description, pages 1-16, filed with letter dated 11 February 2020;
Claims 1-33, filed with letter dated 7 April 2020;
Drawings 1/3-3/3 as published.

The Registrar: The Chairman:

S. Sánchez Chiquero G. Eliasson

Decision electronically authenticated