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**Datasheet for the decision
of 3 July 2018**

Case Number: T 0416/16 - 3.5.06

Application Number: 10790095.3

Publication Number: 2443551

IPC: G06F7/483, G06F7/523,
H03K19/177

Language of the proceedings: EN

Title of invention:

PROCESSING WITH COMPACT ARITHMETIC PROCESSING ELEMENT

Applicant:

Singular Computing, LLC
Bates, Joseph

Headword:

Low precision high dynamic range/SINGULAR

Relevant legal provisions:

EPC Art. 83, 84

Keyword:

Claims - clarity (no)
Sufficiency of disclosure - (no)

Decisions cited:

Catchword:



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Case Number: T 0416/16 - 3.5.06

D E C I S I O N
of Technical Board of Appeal 3.5.06
of 3 July 2018

Appellant: Singular Computing, LLC
(Applicant 1) 10 Regent Street
Newton, MA 02465 (US)

Appellant: Bates, Joseph
(Applicant 2) 10 Regent Street
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Representative: CSY St Albans
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Decision under appeal: **Decision of the Examining Division of the
European Patent Office posted on 1 October 2015
refusing European patent application No.
10790095.3 pursuant to Article 97(2) EPC.**

Composition of the Board:

Chairman W. Sekretaruk
Members: M. Müller
A. Teale

Summary of Facts and Submissions

- I. The appeal is against the decision of the examining division, dated 1 October 2015, to refuse European patent application No. 10 790 095.3. For its reasons, the decision referred to the communication dated 10 February 2015, which was annexed to the summons to oral proceedings and in which *inter alia* objections under Articles 83 and 84 EPC were raised.

- II. Notice of appeal was filed on 19 November 2015, the appeal fee being paid on the same day. A statement of grounds of appeal was received on 28 January 2016. The board understands the appellant's request as being that the decision be set aside and a patent be granted on the basis of the application documents subject to the refusal, in particular on the basis of claims 1-15 as filed with the letter dated 10 September 2014.

Claim 1 reads as follows:

"A device comprising:

at least one computing device adapted to control the operation of a plurality of execution units; and

the plurality of execution units, wherein each of the plurality of execution units is adapted to execute a first operation of multiplication, division, addition, or subtraction on a first input signal representing a first numerical value and a second numerical value to produce a first output signal representing a second [sic] third numerical value, and

wherein the dynamic range of the possible valid inputs to the first operation is at least as wide as from 1/65,000 through 65,000 and,

wherein each of the plurality of execution units is adapted to execute the first operation such that for

some $X \geq 5\%$ of the possible valid inputs to the first operation, for each of those inputs V , the statistical mean of the numerical values output over repeated execution of the first operation on V differs by at least $Y = .05\%$ from the result of an exact mathematical calculation of the same first operation on the numerical values of the same input V ."

III. In an annex to a summons to oral proceedings, the board informed the appellant of its preliminary opinion that the claimed invention did not comply with Articles 83 and 84 EPC.

IV. In response to the summons, the appellant filed neither amendments nor arguments and, in its letter dated 14 June 2018, withdrew its request for oral proceedings and stated that it would not attend any oral proceedings. The oral proceedings were then cancelled.

Reasons for the Decision

The invention

1. The application starts from the observation that the computing power of modern microprocessors is not available to or not required for all applications (see, for instance, paragraphs 2, 18, 24, 37 and 88 to 124 of the description as originally filed). In many cases, therefore the prior art microprocessors make inefficient use of their transistors (paragraph 18).

1.1 It is thus proposed to provide the required computing power in a "fundamentally different" manner, namely by

using so-called low precision high dynamic range (LPHDR) processing elements (PE) in a parallel array arrangement (referred to as a "processing element array" PEA; see paragraphs 32, 35 and 36, figure 1, no. 104, and figure 2). The processing elements provide "low precision" primarily by operating on shorter operands than conventional microprocessors (for instance 5 rather than 64 bits) and, optionally, by introducing "noise" and "fabrication errors" (see paragraph 81), and they offer a "high dynamic range", i.e. the ability to represent very small and very large numbers, by using a logarithmic number system (LNS) (see paragraphs 59-61).

- 1.2 In a specific, exemplary embodiment (see paragraph 83), the machine model according to the invention is said to be characterised by (1) being massively parallel, (2) providing LPHDR arithmetic, possibly with noise, (3) providing a small amount of memory local to each arithmetic unit, (4) providing the execution units in a two-dimensional physical layout with only local connections and (5) providing only limited bandwidth communication.

Clarity, Article 84 EPC

2. Claim 1 specifies a device comprising a plurality of execution units under the control of a "computing device", each execution unit carrying out a binary arithmetic operation (multiplication, division, addition or subtraction). The execution units are further defined by their "dynamic range of the possible valid inputs" which is "at least as wide as from 1/65000 through 65000" and the fact that "the statistical mean of" their results "differs by at least

Y=.05%" from the exact mathematical result "for some X \geq 5% of" all "possible valid inputs".

- 2.1 The "dynamic range" feature is meant to subsume the disclosed use of a logarithmic number system (see above, and also the examining division's communication of 10 February 2015, point 3.1.1). Accordingly, the description discloses at least one way of practising this feature, as required by Rule 42(1)(e) EPC.
- 2.2 However, the description does not disclose any other way of implementing the dynamic range feature, nor has the appellant, in response to the board's doubts in this respect (see point 5 of the summons), argued that any such alternative was commonly known in the art. The board therefore considers that the description cannot support, within the meaning of Article 84 EPC, present claim 1 in its full breadth which specifies the desired "dynamic range" without any indication as to how it is meant to be achieved.
3. The feature relating to the accuracy of the execution units is unclear in several respects.
 - 3.1 The minimal difference from the exact mathematical result is specified "for some X \geq 5% of the possible valid inputs to the first operation". That first operation being binary, it is not clear whether the "X" refers to either of the two operands of this operation or both in combination, Article 84 EPC. The appellant argues that it is possible to test whether any given device satisfies the required accuracy specification (see the grounds of appeal, page 4, penultimate paragraph) and thus falls within the scope of the

claim. This may be true, but does not overcome the mentioned clarity problem.

- 3.2 The feature in question specifies that *at least* 5% of the possible inputs should have a *minimal* difference of 0.05% from the exact mathematical result. This is apparently intentional, as it corresponds to the wording in the description (see paragraph 142, sentence bridging pages 44 and 45). It has the consequence, however, that execution units which are a lot less accurate than probably intended fall within the scope of the claim. In particular, an execution unit which deviates considerably from the exact mathematical result for all possible input values satisfies the required inaccuracy. While this may, *per se*, not be a clarity problem, it has makes it virtually impossible to assess any effect of the claimed minimal inaccuracy, for instance on the components of the specified hardware or its computation speed.

Sufficiency of disclosure, Articles 83 EPC

4. The application is concerned with the idea that reducing computation accuracy considerably and replacing this loss by massive parallelism may lead to a useful and affordable new type of hardware. The application discloses that the "degree of precision of" an LPHDR "element may vary from implementation to implementation" (see paragraphs 140 and 142). No explanation is given, however, as to what degree of precisions is desirable under which circumstances, nor does the description specify how the execution units are to be adapted to deliver the specifically claimed "degree of precision".

- 4.1 The appellant refers to paragraph 60 of the description to establish that the skilled person was enabled "to adjust the precision of the execution unit according to the claims" (see grounds of appeal, page 3, paragraphs 3-5). Paragraph 60 of the description, however, cited by the appellant in this regard, talks primarily about *maximal* representation errors in the logarithmic number system depending on the number of available bits and an approximate - presumably *maximal* - multiplicative error. The cited passage thus suggests that the accuracy can be influenced by the number of bits in the LNS representation and that, for any specific number of bits, the resulting maximal error for the representation and the multiplication may be determined. It does not allow a conclusion as to how a *minimal* inaccuracy could be obtained, let alone with the specifically claimed parameters (at least 0.05% for at least 5% of the input values) and for any other operation than multiplication. The appellant did not refer the board to any other disclosure of the required teaching, or argue that it would be obvious from common general knowledge in the art alone.
- 4.2 It must therefore be concluded, that the description does not disclose the invention in a manner sufficiently clear and complete for it to be carried out by a person skilled in the art, Article 83 EPC.

Order

For these reasons it is decided that:

The appeal is dismissed.

The Registrar:

The Chairman:



B. Atienza Vivancos

W. Sekretaruk

Decision electronically authenticated