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Datasheet for the decision of 8 May 2020

Case Number: T 0112/16 - 3.4.03

Application Number: 05856066.5

Publication Number: 1834354

IPC: H01L23/38, H01L35/28

Language of the proceedings: EN

Title of invention:
MICROELECTRONIC ASSEMBLY WITH BUILT-IN THERMOELECTRIC COOLER AND METHOD OF FABRICATING SAME

Applicant:
Intel Corporation

Relevant legal provisions:
EPC Art. 56

Keyword:
Inventive step - (yes)

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Beschwerdekammern

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Case Number: T 0112/16 - 3.4.03

D E C I S I O N
of Technical Board of Appeal 3.4.03
of 8 May 2020

Appellant: (Applicant)	Intel Corporation 2200 Mission College Boulevard Santa Clara, CA 95054 (US)
Representative:	2SPL Patentanwälte PartG mbB Postfach 15 17 23 80050 München (DE)
Decision under appeal:	**Decision of the Examining Division of the European Patent Office posted on 18 June 2015 refusing European patent application No. 05856066.5 pursuant to Article 97(2) EPC.**

Composition of the Board:

Chairman	G. Eliasson
Members:	M. Ley
	W. Van der Eijk

Summary of Facts and Submissions

I. The appeal is against the decision of the examining division to refuse European patent application No. 05 856 066.5.

The examining division decided that the subject-matter of claims 1 to 11 according to the main request and according to the auxiliary request, both filed with the letter of 5 May 2015, did not meet the requirements of Article 56 EPC 1973.

II. In the notice of appeal, the appellant stated that the "subject of the appeal is the entire decision". In the statement of grounds of appeal, the appellant requested "reversal of the Decision to refuse the application, and grant of a patent on the basis of either the Main or the Auxiliary request". He also requested oral proceedings "before any Decision adverse to the applicant".

In a letter dated 11 August 2016, the appellant submitted second and third auxiliary requests and provided further arguments.

III. In a communication of the Board pursuant to Rule 100(2) EPC, the Board informed the appellant that it provisionally agreed with the appellant that an inventive step in the sense of Article 56 EPC 1973 is to be acknowledged for claim 1 of the main request. The Board indicated amendments to be made to the set of claims according to the main request and to the description in order to fulfil, inter alia, the requirements of Article 84 EPC 1973.

IV. With a letter dated 13 January 2020 the appellant submitted a set of amended claims 1 to 11 and amended description pages 3, 5, 6, 13 and 17.

The appellant requests that the decision under appeal be set aside and as a main request, that a patent be granted in the following version:

Claims 1 to 11 according to the main request filed with the letter dated 13 January 2020

Description: pages 1, 2, 4, 7 to 12 and 14 to 16 as published and pages 3, 5, 6, 13 and 17 filed with the letter dated 13 January 2020

Drawings: sheets 1/10 to 10/10 as published.

In the alternative, grant of a patent on the basis of the auxiliary request, filed with the statement of the grounds of appeal, or on the basis of the second or third auxiliary request, filed with letter dated 11 August 2016, is requested.

V. The following documents are referred to:

D1 US 6 800 933 B1
D3 US 6 559 538 B1

VI. Claim 1 of the main request has the following wording:

A method of fabricating a microelectronic assembly including a built-in thermoelectric cooler, TEC, (120) and a microelectronic device (110) coupled to the TEC, the method comprising:
providing the microelectronic device;

fabricating the built-in TEC directly onto the microelectronic device such that there is no mounting material between the built-in TEC and the microelectronic device;
wherein fabricating the built-in TEC comprises:
initially forming a plurality of first conductive elements (124, 128, 132) of the built-in TEC directly on the microelectronic device;
subsequently forming a N-type layer (230) of thermoelectric, TE, material (230) on the plurality of first conductive elements;
subsequently forming an electrode pattern in the N-type layer to yield a plurality of N-type electrodes (116);
subsequently depositing an electrical insulator layer (260) between the N-type electrodes and between the first conductive elements;
forming an electrode pattern in the electrical insulator layer (260) to define vias (265) therein, said vias exposing a portion of said first conductive elements;
forming a plurality of P-type conductivity legs (290) of TE material in the vias defined in the electrical insulator layer; and
etching back the P-type conductivity legs to yield a plurality of P-type electrodes (118);
wherein each P-type electrode is electrically coupled to a corresponding one of the first conductive elements, and an N-type electrode and a P-type electrode are coupled to each given one of the first conductive elements together forming a pair of N-type and P-type electrodes;
providing a plurality of second conductive elements (122, 126, 130, 134) such that each of the second conductive elements is adapted to allow electrical current to flow in series through respective pairs of N-type and P-type electrodes; and

wherein the electrode pattern in the electrical insulator layer (260) corresponds to a pattern of P-type electrodes.

Reasons for the Decision

1. The appeal is admissible.

2. For the Board, the subject-matter of claim 1 according to the main request does involve an inventive step in the sense of Article 56 EPC 1973.

3. The examining division and the appellant both considered D3 as the closest prior art. The Board has no reasons to deviate from this choice.

4. Document D3 discloses a microelectronic assembly including a built-in thermoelectric cooler, TEC, (27, 28, 31) and a semiconductor wafer with active electric circuitry, i.e. a microelectronic device (26b, 23, 22, 21, 26a, Figure 2b), coupled to the TEC, wherein the TEC is directly formed on an insulating barrier layer 26a of the microelectronic device. In D3, the TEC is made by forming an bismuth telluride layer (28, Bi_2Te_3) on patterned first conductive electrodes (27) and by forming N+ and P+ regions by ion implantation therein. Second conductive electrodes 31 are formed on the Bi_2Te_3 layer.

Hence, in the wording of claim 1, D3 discloses (Figures 2a - 2g) a method of fabricating a microelectronic assembly including a built-in thermoelectric cooler, TEC, (27, 28, 31) and a microelectronic device (26b, 23, 22, 21, 26a, Figure 2b) coupled to the TEC (Figure 2g), the method comprising:

providing the microelectronic device (Figure 2b);
fabricating the built-in TEC directly onto the microelectronic device such that there is no mounting material between the built-in TEC and the microelectronic device (Figures 2b - 2g);
wherein fabricating the built-in TEC comprises:
initially forming a plurality of first conductive elements (27) of the built-in TEC directly onto the microelectronic device (Figure 2c);
subsequently forming a N-type layer (28) of thermoelectric TE material (N+, Figure 2e) on the plurality of first conductive elements (27);
subsequently forming an electrode pattern in the N-type layer to yield a plurality of N-type electrodes (N+, Figure 2e);
~~subsequently~~ depositing an electrical insulator layer (28, undoped Bi_2Te_3, Figure 2d) ~~between the N-type electrodes and~~ between the first conductive elements;
~~forming an electrode pattern in the electrical insulator layer to define vias therein, said vias exposing a portion of said first conductive elements;~~
forming a plurality of P-type conductivity legs (P+, Figure 2f) of TE material ~~in the vias defined~~ in the electrical insulator layer (28)~~; and~~
~~etching back the P-type conductivity legs~~ to yield a plurality of P-type electrodes (P+, Figure 2f);
wherein each P-type electrode is electrically coupled to a corresponding one of the first conductive elements (27), and an N-type electrode and a P-type electrode are coupled to each given one of the first conductive elements (27) together forming a pair of N-type and P-type electrodes (Figure 2f);
providing a plurality of second conductive elements (31) such that each of the second conductive elements (31) is adapted to allow electrical current to flow in

series through respective pairs of N-type and P-type electrodes (Figure 2f)~~; and~~
~~wherein the electrode pattern in the electrical insulator layer corresponds to a pattern of P-type electrodes.~~

5. Consequently, D3 does not disclose the claimed way the N-type and P-type electrodes are formed between the first and second conductive elements. In other words, D3 does not disclose:
(a) subsequently depositing an electrical insulator layer between the N-type electrodes and between the first conductive elements;
(b) forming an electrode pattern in the electrical insulator layer to define vias therein, said vias exposing a potion of said first conductive elements;
(c) forming a plurality of P-type conductivity legs of TE material in the vias defined in the electrical insulator layer (28); and
(d) etching back the P-type conductivity legs to yield a plurality of P-type electrodes (P+, Figure 2f);
wherein the electrode pattern in the insulator layer corresponds to a pattern of P-type electrodes.

The Board is of the opinion that the wording of claim 1 requires said method steps in the sequence (a) -> (b) -> (c) -> (d).

In its decision, the examining division argued that D3 did not disclose initially forming a plurality of first conductive elements of the built-in TEC directly onto the microelectronic device. The Board is of the opinion that this feature is disclosed in Figure 2c of D3, as the structure shown in Figure 2b is the microelectronic device with its insulating barrier layer 26a.

In the statement of grounds of appeal, the appellant argued that D3 did not disclose forming an N-type layer and etching this layer to form N-type electrodes. The Board notes however that the wording of claim 1 does not require an etching of the N-type layer of TE material to form N-type electrodes.

6. The Board agrees with the examining division that the objective problem to be solved by the skilled person is to provide N-type and P-type electrodes of the built-in thermoelectric cooler in an alternative way.

In the statement of grounds of appeal, the appellant argued that the method according to claim 1 provided an improved method that involved fewer fabrication steps and greater control and improved performance. The Board is of the opinion that the claimed method does not necessarily involve fewer fabrication steps, greater control and improved performance, when compared to the method already known from D3. Therefore, the Board is of the opinion that the examining division's formulation of the objective technical problem is correct.

7. In the contested decision, the examining division argued that the subject-matter of claim 1 was rendered obvious by a combination of D3 with document D1.

The appellant argued that the skilled person would not consider D1, because it concerned a method with forming the integrated circuit only after forming the thermoelectric cooler.

The Board is not convinced by this argument, because D1 is from the same technical field as D3 and shows ways to form N-type and P-type electrodes for a

thermoelectric cooler. Therefore, the Board agrees with the examining division that the skilled person would consider document D1 in order to solve the objective technical problem, i.e. to provide an alternative way of producing an thermoelectric cooler on a substrate.

8. However, in the Board's judgement, document D1 would not prompt the skilled person to the claimed method for the following reasons:

8.1 D1 discloses (Figure 1) a method of fabricating a microelectronic assembly including a built-in thermoelectric cooler (38, 50, 52, 46, 48, 54, 56, Figure 2) and microelectronic device (10, Figure 1) coupled to the TEC (Figure 2), the method comprising:
fabricating the built-in TEC (38, 50, 52, 46, 48, 54, 56) directly onto a base substrate (32) such that there is no mounting material between the built-in TEC (Figure 2) and the base substrate (32), wherein fabricating the built-in TEC comprises:
initially forming a plurality of first conductive elements (38) of the built-in TEC directly onto the base substrate (32, Figure 3 or 13);.
subsequently forming N-type electrodes (Figure 12: 46, 48; Figure 19: 106, 108) and P-type electrodes (Figure 12: 50, 52; Figure 19: 96, 98) in an insulator layer (Figure 12: 34, Figure 19: 82)
providing a plurality of second conductive elements (54, 56) such that each of the second conductive elements is adapted to allow electrical current to flow in series through respective pairs of N-type and P-type electrodes.

8.2 As acknowledged by the examining division and the appellant, D1 discloses two possible ways of forming

the N-type electrodes and P-type electrodes in an insulator layer.

In the Example shown in Figures 3 - 12, the N-type electrodes and the P-type electrodes are formed by ion implantation of respective n-type regions (46, 48 or 50, 52) and p-type regions (50, 52 or 46, 48) within a semiconductor layer (60), see Figures 5 and 6. The semiconductor layer is then patterned to form n-type and p-type electrodes, see Figure 8. Only then the n-type and p-type electrodes are embedded (Figure 9) in an insulator film (34).

In the alternative Example shown in Figures 13 - 19, an insulator layer (82) is formed, first trenches (90, 92) are formed in the insulator layer (82, Figure 14) and first conductivity type electrodes (96, 98, e.g. N-type electrodes) are formed by depositing a first-conductivity type layer (94, Figure 15) in the first trenches (90, 92) and on the insulator layer (82) and by performing an etchback of the first-conductivity type layer (94, Figure 16). Subsequently, second trenches (102, 104) are formed in the insulator layer (82, Figure 17) and second conductivity type electrodes (106, 108, e.g. P-type electrodes) are formed by depositing a first-conductivity type layer (105, Figure 18) in the first trenches (102, 104) and on the insulator layer (82) and by performing an etchback of the second-conductivity type layer (105, Figure 19).

8.3 Hence, when starting from D3 as closest prior art and wishing to solve the objective technical problem, the skilled person would either implement the solution of the Example of Figures 3 - 12 of D1 or the one of the Example of Figures 13 - 19 of D1 in the method of D3. In both cases, the skilled person would not arrive at

the method as defined in claim 1 according to the main request. When using the steps shown in Figures 3 - 8 of D1, he would not provide an insulator layer with vias and, when using the steps shown in Figures 13 - 18 of D1, he would not form the N-type electrodes prior to forming the electrical insulator layer.

In view of the above, the Board does not agree with the examining division that the skilled person would form the N-type electrodes using the process steps shown in Figures 3 - 8 of D1 and then go on to form the P-type electrodes using the process steps shown in Figures 17 - 18 of D1. There is no indication in D1 that would hint at the possibility of using a method combining some steps from the first Example (Figures 3 - 12) with steps from the second alternative Example (Figure 13 - 19). Hence, the skilled person combining the teaching of D3 with D1 would not arrive at a method according to claim 1 without employing inventive skills.

Hence, the Board is of the opinion that an inventive step in the sense of Article 56 EPC 1973 is to be acknowledged.

There is no reason for the Board to comment on the first to third auxiliary requests.

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the first instance with the order to grant a patent with the following documents:

   Claims 1 to 11 according to the main request filed with the letter dated 13 January 2020

   Description: pages 1, 2, 4, 7 to 12 and 14 to 16 as published and pages 3, 5, 6, 13 and 17 filed with the letter dated 13 January 2020

   Drawings: sheets 1/10 to 10/10 as published

The Registrar: The Chairman:

S. Sánchez Chiquero G. Eliasson

Decision electronically authenticated