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Datasheet for the decision of 8 June 2020

Case Number: T 2253/15 - 3.4.03

Application Number: 04781635.0

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Language of the proceedings: EN

Title of invention:
METHODS FOR CONTROLLING ELECTRO-OPTIC DISPLAYS

Applicant:
E Ink Corporation

Relevant legal provisions:
EPC 1973 Art. 54(1), 56

Keyword:
Novelty - after amendment (yes)
Inventive step - (no) - obvious solution

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Case Number: T 2253/15 - 3.4.03

D E C I S I O N
of Technical Board of Appeal 3.4.03
of 8 June 2020

Appellant: (Applicant)	E Ink Corporation 1000 Technology Park Drive Billerica, MA 01821-4165 (US)
Representative:	Cole, David John 46 Kirkhill Gardens West Greenlees Estate Cambuslang Glasgow G72 8EZ (GB)
Decision under appeal:	**Decision of the Examining Division of the European Patent Office posted on 20 July 2015 refusing European patent application No. 04781635.0 pursuant to Article 97(2) EPC.**

Composition of the Board:

Chairman	G. Eliasson
Members:	M. Ley
	G. Decker

Summary of Facts and Submissions

I. The appeal is against the decision of the examining division to refuse European patent application No. 04 781 635.0.

The examining division decided that the subject-matter of claims 1, 4 - 6 and 8 of the set of claims filed on 5 June 2015 lacked novelty over D1 (Articles 52(1) EPC, 54(1) and (2) EPC 1973), that the subject-matter of claims 3 and 7 lacked an inventive step (Article 56 EPC 1973) and that claim 2 was not clear (Article 84 EPC 1973).

The following document was cited:

D1 US 6 531 997 B1

II. With the statement of grounds of appeal, the appellant filed amended claims.

Neither in the notice of appeal nor in the statement of grounds the appellant requested oral proceedings.

III. On 20 November 2019, the Board issued a summons to attend oral proceedings on 21 April 2020. In a communication pursuant to Article 15(1) RPBA 2007, the Board raised objections under Article 123(2) EPC and Article 56 EPC 1973 against claims 1 and 6.

IV. In a letter dated 16 March 2020, the appellant filed amended claims and explained that the amendments were made to address and overcome the objections under Article 123(2) EPC. It further provided arguments in support of an inventive step.

The appellant requests as a sole request grant of a patent on the basis of claims 1 to 6 filed with letter dated 16 March 2020 and labelled "Auxiliary Request B".

Moreover, the appellant informed the Board that it would not attend the oral proceedings and requested "that the Decision on this appeal be rendered on the basis of the written record, including the present submission".

V. The oral proceedings were subsequently cancelled by the Board.

VI. Claim 1 according of the sole request has the following wording (the labelling (a) to (l) in claim 1 and (i) to (x) in claim 6 has been added by the Board):

An active matrix electro-optic display comprising:
(a) a layer of a bistable electro-optic medium;
(b) a plurality of pixel electrodes disposed on one side of the layer of electro-optic medium;
(c) a plurality of data lines; a plurality of select lines, each pixel being defined uniquely by the intersection of one data line and one select line;
(d) at least one transistor associated with each pixel electrode, the gate electrodes of the transistors in each row of pixel electrodes being connected to the same select line, and each column of pixel electrodes being connected via their respective transistors to the same data line;
(e) pixel drive means arranged to apply voltages to the data lines;
(f) a common electrode on the opposed side of the layer of electro-optic medium from the pixel electrodes; and
(g) common electrode control means (100; 300; 400; 900) arranged to apply voltages to the common electrode,

(h) the display having a writing mode, in which a voltage is applied to each select line in turn, while the voltages on the data lines are adjusted to provide a desired optical response from the pixels in the selected row, so that
(i) the pixel drive means applies at least two different voltages to different ones of the pixel electrodes, thereby writing an image on the electro-optic medium, and
(j) a non-writing mode in which scanning of the select lines ceases, and in which the pixel drive means controls the voltages applied to the pixel electrodes so that any image previously written on the electro-optic medium is substantially maintained,
(k) the display being characterized in that the common electrode control means (100; 300; 900) being arranged to apply to the common electrode a first voltage (VCOM) when the display is in its writing mode and a second voltage (VSM), different from the first voltage (VCOM), when the display is in its non-writing mode,
(l) the display also being arranged so that during the non-writing mode, all of the pixel electrodes are set to the second voltage (VSM), thus creating zero voltage between the pixel electrodes and the common electrode.

Claim 6 of the sole request has the following wording:

A method of operating an active matrix electro-optic display which comprises:
(i) a layer of a bistable electro-optic medium;
(ii) a plurality of pixel electrodes disposed on one side of the layer of electro-optic medium,
(iii) a plurality of data lines; a plurality of select lines, each pixel being defined uniquely by the intersection of one data line and one select line,

(iv) each pixel electrode having at least one transistor associated therewith, the gate electrodes of the transistors in each row of pixel electrodes being connected to the same select line, and the transistors in [sic] each column of pixel electrodes being connected via their respective transistors to the same data line, each pixel being defined uniquely by the intersection of one data line and one select line; and
(v) a common electrode on the opposed side of the layer of electro-optic medium from the pixel electrodes, the method comprising:
(vi) applying a first voltage (VCOM) to the common electrode while a voltage is applied to each select line in turn,
(vii) while the voltages on the data lines are adjusted to provide a desired optical response from the pixels in the selected row, so that
(viii) applying at least two different voltages to different ones of the pixel electrodes, thereby writing an image on the electro-optic medium; the method being characterized by
(ix) ceasing scanning of the select lines and
(x) applying a second voltage (VSM), different from the first voltage (VCOM), to the common electrode and to all the pixel electrodes so that any image previously written on the electro-optic medium is substantially maintained.

VII. The appellant mainly argued that the present invention was directed to a solution to the problem of "gate feedthrough voltage" or "kick back" by the characterizing portion of the independent claims. D1 did not mention any negative effects due to "gate feedthrough voltages" and did not use a first constant voltage during a writing mode and a second, different constant voltage during the non-writing mode.

Reasons for the Decision

1. The appeal is admissible.

2. Procedural matters

Although oral proceedings were not requested, the Board found it appropriate to summon the appellant to attend oral proceedings and informed it about its provisional opinion that the requirements of Article 123(2) EPC and Article 56 EPC 1973 were not met for claims 1 and 6.

In its response, the appellant filed an amended request, explained that the amendments were made to address and overcome the objections under Article 123(2) EPC and provided arguments in support of an inventive step. Moreover, the appellant declared its absence during oral proceedings and requested that a decision be taken "on the basis of the written record".

In view of the appellant's declaration and of the fact that the case is ready for decision on the basis of the appellant's written submissions in the statement of grounds of appeal, the appellant's response of 16 March 2020 and the decision under appeal, the Board has cancelled the oral proceedings and issues this decision in written proceedings in accordance with Articles 12(8) and 15(3) RPBA 2020.

3. The Board is satisfied that the present set of claims complies with Article 123(2) EPC.

However, for the reasons given below, the subject-matter of claims 1 and 6 lacks an inventive step (Article 56 EPC 1973).

4. The invention

The present invention relates to electro-optic displays and, in particular, to reducing the rate of deterioration of display material in such displays.

Each pixel of the display has a bistable electro-optic medium between an individual pixel electrode and a common electrode shared by several or even all pixels. The term "bistable" refers to displays comprising display elements having first and second display states differing in at least one optical property, and such that after any given element has been driven, by means of an addressing pulse of finite duration, to assume either its first or second display state, after the addressing pulse has terminated, that state will persist for at least several times of the addressing pulse required to change the state of the display element, see paragraph [0003].

The pixel electrode is electrically connected to a respective data line via a transistor, whose gate electrode is driven by a select line. In the claimed active matrix display, pixels of each column are connected to the same data line and transistors of each row to a same select line so that a row-by-row writing is possible. Like for known electro-optic displays, it is advantageous to stop scanning the active matrix bistable electro-optic display between image updates to save power.

The problem the present invention addresses is described in paragraphs [0018] and [0019]. After stopping the row-by-row scanning, a voltage might persist between the common electrode and the pixel electrodes and induce a current flowing from the pixel

electrodes through the electro-optic medium to the common electrode and deteriorating the electro-optic medium. The invention proposes to avoid this undesired current by the features of the characterising portion of the independent claims.

5. Novelty - Article 52(1) EPC and Article 54(1) and (2) EPC 1973

5.1 Document D1 is considered closest prior art in the decision under appeal and the board agrees with this assessment.

According to figures 4A, 4B, 9B, col. 26, lines 1 to 4 and lines 40 to 43, col. 30, lines 52 to 54, col. 32, lines 12 to 67, the electrophoretic display of D1 uses a conventional active matrix liquid crystal display backplane with silicon based thin film transistors. The skilled person understands from the above passages that, in this type of device, each pixel is defined by the intersection of one data line and one select line and that each pixel electrode is connected to the one data line via its associated transistor, which has its transistor gate electrode connected to the one select line.

Therefore, document D1 discloses (in the wording of claim 1, underlining and strike-through by the board) an active matrix electro-optic display (figures 4A and 4B, col. 26, lines 1 to 4: "encapsulated electrophoretic display using an active matrix liquid crystal display backplane") comprising:
a layer of a bistable electro-optic medium (figure 9B, 108, 110);
a plurality of pixel electrodes (104, 106) disposed on one side of the layer of electro-optic medium (108,

110);
a plurality of data lines; a plurality of select lines, each pixel being defined uniquely by the intersection of one data line and one select line (implicit as an active matrix structure is used, see col. 26, lines 1 to 4);
at least one transistor (col. 26, lines 1 to 4, col. 32, lines 7 to 44) associated with each pixel electrode (figure 9B), the gate electrodes of the transistors ~~in each row of pixel electrodes~~ being connected to ~~the same~~ a respective select line, and ~~each column of~~ the pixel electrodes being connected via their respective transistors to ~~the same~~ a respective data line (implicit for an active matrix structure, col. 26, lines 1 to 4, col. 32, lines 7 to 44);
pixel drive means arranged to apply voltages (figure 9B, "0", "+V" applied to pixel electrodes 104, 106, figure 12, 128, 130) to the data lines (i.e. to the pixel electrodes via the transistors, col. 26, lines 1 to 4, col. 32, lines 7 to 44);
a common electrode (100, figure 9B, col. 26, lines 4 to 10, "common, transparent front electrode 100") on the opposed side of the layer of electro-optic medium (108, 110) from the pixel electrodes (104, 106, figure 9B); and
common electrode control means arranged to apply voltages to the common electrode (figure 9B, "0", "+V" applied to common electrode 100, figure 12, "R", 128, 130),
the display having a writing mode (figure 12, 128, 130), in which a voltage is applied to each select line in turn (implicit in view of an active matrix pixel array, col. 26, lines 1 to 4, col. 31, lines 24 to 30), while the voltages on the data lines are adjusted to provide a desired optical response from the pixels (implicit in view of col. 26, lines 1 to 4) ~~in the~~

~~selected row~~, so that
the pixel drive means applies at least two different voltages to different ones of the pixel electrodes (figure 12, col. 29, lines 11 to 38 in combination with col. 27, lines 9 to 67), thereby writing an image on the electro-optic medium (figure 12), and
a non-writing mode (figure 12, "R", "resting sub-cycles") in which scanning of the select lines ceases (figure 12, "R", "resting sub-cycles"), and in which the pixel drive means controls the voltages applied to the pixel electrodes so that any image previously written on the electro-optic medium is substantially maintained (figure 12),
the display being characterized in that the common electrode control means (100) being arranged to apply to the common electrode a first voltage ("+V", "E", col. 29, lines 13 to 14) when the display is in its writing mode (figure 12, time intervals 128 and 130) and a second voltage (figure 12, "0", "R"), different from the first voltage ("+V"), when the display is in its non-writing mode (figure 12, "R", col. 29, lines 17 to 19),
the display also being arranged so that during the non-writing mode (figure 12, "R"), all of the pixel electrodes are set to the second voltage ("0", col. 29, lines 17 to 19), thus creating zero voltage between the pixel electrodes and the common electrode (figure 12).

5.2 The appellant argued in the statement of grounds of appeal that the bistable displays according to the present invention had three different modes: a writing scanning mode, a non-writing scanning mode and a non-writing, non scanning mode. For the appellant, D1 did not disclose any "non-scanning" mode.

The Board is of the opinion that the independent claims only define two modes: a writing mode with scanning of the select lines taking place and a non-writing mode with no scanning and, consequently, without writing. A scanning mode without any writing of an image on the electro-optic medium is disclosed neither in the claims nor in the application as a whole.

In the Board's view, D1 also discloses the two modes as defined in claim 1: a writing mode (figure 12, time intervals 128 and 130) and a non-writing mode (see col. 27, lines 13 - 20, col. 28, line 66 to col. 29, line 2). During time intervals 128 and 130 in figure 12, at least a portion of the pixels in the pixel array of D1 change their state and are "written" so that during time intervals 128 and 130 the display is in its writing-mode. As in interval 128, the first voltage +V is applied to the common electrode 100, the common electrode control means (100) in D1 are "arranged to apply to the common electrode a first voltage when the display is in its writing mode".

5.3 The appellant argued that D1 used in figure 12 an "unusual bi-level drive scheme", because only two different voltages were applied to the pixel electrodes and the common electrode (0 or "+V").

This drive scheme is, however, not excluded by the wording of claims 1 or 6.

5.4 The appellant stated that figure 12 showed that zero voltage was applied to the common electrode 100 and during the (driving) interval 130 and the rest intervals R. From this fact, the appellant concluded that either (a) the drive scheme of figure 12 was not used in a active matrix pixel or that (b) the drive

scheme of figure 12 was used in an active matrix pixel, but scanning took place in intervals "R" or that (c) the drive scheme of figure 12 was used in an active matrix pixel and at least a part of interval "R" represented a non-writing, non-scanning mode, but the skilled person was not aware of the problems caused by gate feedthrough voltage when switching from a scanning to a non-scanning mode.

ad (a): Contrary to the appellant's argument, the Board finds that the passage in col. 26, lines 1 to 4 discloses that the device of figure 9B is an active matrix display. Figure 12 discloses a drive scheme for the device of figure 9B, see col. 28, line 66 to col. 29, line 6.

ad (b) and (c): From the wording "resting sub-cycles, designated "R", in which the display is not driven", the skilled person would understand that no scanning takes place during the sub-cycles "R" in figure 12. The sub-cycles therefore define a non-scanning non-writing mode in the sense of claims 1 and 6. The appellant's argument that the skilled person would not be aware of the problems caused by gate feedthrough when switching from a scanning to a non-scanning mode in D1, is not relevant for novelty and will be discussed below in the context of inventive step.

5.5 In the letter dated 16 March 2020, the appellant argued that, according to the wording of feature (k) in claim 1, only one voltage was applied to the common electrode in the writing mode and only one voltage was applied in the non-writing mode, the voltage applied in the non-writing mode being different from that applied in the writing mode. The appellant referred to figure 1 and paragraphs [0099] and [0100]. None of the displays

described in D1 used a first constant voltage during a writing mode and a second, different constant voltage during the non-writing mode. In the embodiment of figure 9B, the common electrode was held at constant voltage of 0, except for part 128 of the writing mode.

The Board does not share the appellant's view. Figure 12 of D1 shows the operation of the device of figure 9B with a writing mode 128, 130 and a non-writing mode "R", wherein during the writing mode 128, 130 a voltage of +V is applied to the common electrode V_{COM} (figure 12, "E") and wherein during the non-writing mode "R" a voltage of 0V is applied to the common electrode V_{COM}. Contrary to the appellant's interpretation of claim 1, the Board opines that its wording does not require a constant voltage applied during the entire duration of the writing mode 128, 130. As presently formulated, feature (k) of claim 1 merely states that the common electrode control means are arranged to apply to the common electrode a first voltage when the display is in its writing mode, which is the case for the writing period 128, 130, when the voltage +V is applied to the common electrode V_{COM}. Voltage +V is different from the voltage of 0V applied during non-writing mode "R".

5.6 Consequently, the subject-matter of claim 1 differs from D1 only in that the gate electrodes of the transistors in each row of pixel electrodes being connected to the same select line, and each column of pixel electrodes being connected via their respective transistors to the same data line and that, as a consequence thereof, in the writing mode, "the voltages on the data lines are adjusted to provide a desired optical response from the pixels in the selected row".

The subject-matter of claim 1 is therefore novel over D1.

Regarding claim 6, the Board understands that, analogously to feature (d) in claim 1, feature (iv) should most probably read "each pixel electrode having at least one transistor associated therewith, the gate electrodes of the transistors in each row of pixel electrodes being connected to the same select line, and ~~the transistors in~~ each column of pixel electrodes being connected via their respective transistors to the same data line".

Hence, for the same reasons, *mutatis mutandis*, the subject-matter of claim 6 is new over D1.

6. Inventive step - Article 56 EPC 1973

6.1 The subject-matter of claims 1 and 6 differs from D1 in the way the transistors (and hence the pixel electrodes) are connected to their respective select and data lines, and therefore in the way the array of pixels and pixel electrodes are addressed during the writing operation, see section 5.6 above. D1 merely discloses that the pixel in the pixel array (D1, figure 4A, 4B) can be addressed sequentially in any order (col. 22, lines 12 to 14). Col. 31, lines 24 to 31 states that the gate pulse timing diagrams are not included in D1.

6.2 In its letter dated 16 March 2020, the appellant argued that a skilled person would not use a first constant voltage during a writing mode and a second different constant voltage during a non-writing mode. The objective technical problem was hence to avoid negative effects related to gate feedthrough voltages. The

skilled person was unaware of the problems caused by gate feedthrough voltages in D1, as the same constant voltage was used in parts 122, 126, 130 of the writing mode and during the non-writing mode "R" (Figures 10 and 12).

For the reasons given in section 5 above, the Board is of the opinion that the mode of operation shown in figure 12 of D1 uses the first and second voltages according to feature (k) and that during the non-writing mode "R", all of the pixel electrodes are set to the second voltage (i.e. 0V), thus creating zero voltage between the pixel electrodes 104, 106 and the common electrode 100. In other words, the display of D1 is arranged so that during the non-writing mode (figure 12, "R"), all pixel electrodes are set to the second voltage ("0", col. 29, lines 17 - 19), thus creating zero voltage between the pixel electrodes and the common electrode (figure 12). Hence, the problem caused by a potential gate feedthrough voltage when switching from a scanning to a non-scanning mode is already solved in D1. The fact that this problem is not mentioned in D1 is not relevant.

Therefore, the objective technical problem solved by the distinguishing features (as defined in sections 5.6 and 6.1 above) must be a different one, namely, to provide a scanning scheme for the active matrix electro-optic display known from D1.

6.3 The skilled person knows from their common general knowledge that, for the conventional "active matrix display" of D1, there are two well-known ways of interconnecting the transistors with their respective data and select lines to perform scanning during a writing operation (see also the present application,

paragraphs [0014] and [0015]): Either the gate electrodes of the transistors in each row of pixel electrodes are connected to the same select line and each column of pixel electrodes are connected via their respective transistors to the same data line so that the writing is performed via row-by-row scanning, i.e. a voltage is applied to the select lines row-by-row. Alternatively, the gate electrodes of the transistors in each column of pixel electrodes are connected to the same select line and each row of pixel electrodes are connected via their respective transistors to the same data line and the writing is done using a column-by-column scanning.

Consequently, a row-by-row scanning is one of two well-known and straightforward implementations for the active matrix display known from D1.

The skilled person, wishing to solve the objective technical problem and using their common general knowledge, would consider implementing a row-by-row scanning for the display of D1. They would therefore provide the display such that the gate electrodes of the transistors in each row of pixel electrodes are connected to the same select line and each column of pixel electrodes is connected via the respective transistors to the same data line. Then, the display has a writing mode, in which a voltage is applied to each select line in turn, while the voltages on the data lines are adjusted to provide a desired optical response from the pixels in the selected row. They would arrive at the subject-matter of claims 1 or 6 without any inventive activity.

Hence, an inventive step (Article 56 EPC 1973) related to the subject-matter of claims 1 and 6 cannot be acknowledged.

7. For the above reasons, the sole request is not allowable so that the appeal must fail.

Order

For these reasons it is decided that:

The appeal is dismissed.

The Registrar: The Chairman:

S. Sánchez Chiquero G. Eliasson

Decision electronically authenticated