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Datasheet for the decision of 20 September 2019

Case Number: T 1988/15 - 3.4.03

Application Number: 09170486.6

Publication Number: 2172977

IPC: H01L29/786, H01L21/77

Language of the proceedings: EN

Title of invention:
Display device

Applicant:
Semiconductor Energy Laboratory Co., Ltd.

Headword:

Relevant legal provisions:
EPC Art. 56

Keyword:
Inventive step - main request (no) - auxiliary request (no)

Decisions cited:

Catchword:

Europäisches Patentamt
European Patent Office
Office européen des brevets

Beschwerdekammern

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Case Number: T 1988/15 - 3.4.03

D E C I S I O N
of Technical Board of Appeal 3.4.03
of 20 September 2019

Appellant: (Applicant)	Semiconductor Energy Laboratory Co., Ltd. 398, Hase Atsugi-shi, Kanagawa 243-0036 (JP)
Representative:	Grünecker Patent- und Rechtsanwälte PartG mbB Leopoldstraße 4 80802 München (DE)
Decision under appeal:	**Decision of the Examining Division of the European Patent Office posted on 6 March 2015 refusing European patent application No. 09170486.6 pursuant to Article 97(2) EPC.**

Composition of the Board:

Chairman	G. Eliasson
Members:	M. Stenger
	W. Van der Eijk

Summary of Facts and Submissions

I. The appeal concerns the decision of the Examining Division to refuse European patent application no. 09170486 in view of the requirements of Articles 123(2) and 84 EPC.

II. In a communication preparing the oral proceedings, the Board referred to the following documents:

D1: US 2002/0043662 A1
patent document 1: JP 2007123861 A1

D1 was cited in the search report and patent document 1 is mentioned in [3] and [4] of the application.

III. At the end of the oral proceedings before the Board, the appellant requested that the decision be set aside and that a patent be granted on the basis of a main request or auxiliary requests 1 or 2, all filed with letter dated 8 August 2019.

IV. Claim 1 of the main request has the following wording (labeling a), b)... added by the Board):

a) *A display device comprising a pixel portion and a driver circuit,*

b) *wherein the pixel portion comprises:*

b1) *a first thin film transistor including at least a first oxide semiconductor layer and a first channel*

protective layer in contact with the first oxide semiconductor layer,

c) *wherein the driver circuit comprises:*

c1) *a second thin film transistor (431) including a second oxide semiconductor layer, a first gate electrode, a gate insulating layer and a second channel protective layer in contact with the second oxide semiconductor layer; and*

c2) *a third thin film transistor (430) including a third oxide semiconductor layer, a second gate electrode, the gate insulating layer and a third channel protective layer in contact with the third oxide semiconductor layer,*

d) *wherein the gate insulating layer is provided on the second gate electrode and the third oxide semiconductor layer is provided on the gate insulating layer,*

e) *wherein a first wiring (411) is in contact with one of a source region and a drain region of the second thin film transistor,*

f) *wherein a second wiring (410) is provided on the gate insulating layer and in direct contact with a top surface of the gate insulating layer and in contact with the other of the source region and the drain region of the second thin film transistor,*

g) *wherein the second wiring is in direct contact with one of a source region and a drain region of the third thin film transistor and in direct contact with the first gate electrode of the second thin film*

transistor through a first contact hole of the gate insulating layer,

h) *wherein a third wiring (409) is in contact with the other of the source region and the drain region of the third thin film transistor,*

i) *wherein a fourth oxide semiconductor layer is provided between the second wiring and the third oxide semiconductor layer or between the third wiring and the third oxide semiconductor layer, the fourth oxide semiconductor layer having a smaller thickness and a higher conductivity than the third oxide semiconductor layer,*

j) and *wherein each of the first thin film transistor, the second thin film transistor and the third thin film transistor is a n-type transistor.*

V. Independent claim 1 of auxiliary request 1 differs from claim 1 of the main request in that it comprises, after feature i), the following additional feature:

k) *wherein the fourth oxide semiconductor layer includes crystal grains in an amorphous structure,*

VI. Independent claim 1 of auxiliary request 2 differs from claim 1 of the main request in that the first "and" of feature j) is missing and in that it comprises at its end the following additional feature:

l) *and wherein an insulating layer covers the first thin film transistor, the second thin film transistor, and the third thin film transistor and is in contact*

with the first channel protective layer, the second channel protective layer, and the third channel protective layer.

VII. The arguments of the appellant may be summarised as follows:

(a) Main request
D1 did not disclose the use of oxide semiconductors.

Further, D1 did not disclose that the second wiring was in direct contact with the first gate electrode of the second thin film transistor through a first contact hole of the gate insulating layer as required by feature g) of claim 1. The second wiring and the first gate electrode could be connected in a different manner.

Finally, D1 also did not disclose that the fourth semiconductor layer had a smaller thickness and a higher conductivity than the third semiconductor layer as required by feature i) of claim 1. This had the advantageous effects of reducing the contact resistance and the height of the TFTs.

(b) Auxiliary request 1
The structure of the fourth semiconductor layer according to additional feature k) of claim 1 was not disclosed in any of the available prior art documents. The additional feature allowed for a higher mobility of charges and thus enabled a shift register circuit operating at higher speed as disclosed in [17] and [18] of the application.

(c) Auxiliary request 2

Although D1 disclosed an insulating layer 1000 in figure 29, this insulating layer was not necessarily in contact with any of the protective layers of the first to third channels. The other documents did not disclose such an insulating layer, either. The insulating layer according to feature l) provided electrical isolation and mechanical protection of the TFTs.

Reasons for the Decision

1. The appeal is admissible.

2. Prior art

2.1 D1

D1 discloses display devices where a pixel portion and a driver circuit are formed on the same substrate ([34], see also figure 29). The thin film transistors (TFTs) used may all be reverse stagger type n-channel TFTs with their gates arranged directly on the substrate (bottom-gate). The channel layer of the TFTs consists mainly of silicon with a small amount of germanium ([92]) and is produced by crystallising an amorphous film ([12]), thereby improving the transport characteristics of the film ([11]).

For details of the device shown in figure 29, D1 refers to embodiment 1 ([269]) which is described in relation to figures 14 to 20 ([149] to [195]). Thus, all these figures effectively relate to the same embodiment. In particular, individual TFTs that can be used for the device shown in figure 29 are described with respect to figure 14 and elements of the driver circuit shown in figure 29 are described in relation to figure 15.

Consequently, the driver circuit shown in figure 29 can comprise an inverter circuit which is implemented using an enhancement and a depletion type TFT (EDMOS circuit) according to figure 15B, wherein further each of the TFTs corresponds to the one shown in figure 14.

2.2 Patent document 1

The applicant of patent document 1 is the appellant. Patent document 1 relates to display devices (figure 12) where TFTs used for the drive circuit and for the pixel part are formed on the same substrate 700 in a bottom-gate configuration ([104] to [106], figure 7). Oxide semiconductors are used for the channel layers of the TFTs instead of silicon ([3] to [7]) and the TFTs may be provided with a channel protective film 407 ([86] to [96], figures 4 and 5).

3. Main request, Article 56 EPC

3.1 Preliminary remark

The Board notes that in the application, for each connection between a wiring layer and a channel forming layer only one single interposed layer (labeled 406a, 406b, 408a and 408b in figure 1A) is provided. Further, one of the single interposed layers 406a and 406b in contact with the channel forming third oxide semiconductor layer (labeled 405 in figure 1A, although this layer is referred to as the *first* oxide semiconductor layer in the description) has to correspond to the fourth (oxide) semiconductor layer as defined in claim 1.

That is, the fourth oxide semiconductor layer according to claim 1 corresponds to a layer *directly adjacent* to the channel forming layer.

In the present case, for the purpose of comparing claim 1 with D1, the (interposed) fourth semiconductor layer of claim 1 thus corresponds to one of the layers directly adjacent to the channel forming layer *21* of D1, i.e., to the impurity regions *19* and *20* shown in figure 14 of D1.
Consequently, for the purpose of comparing claim 1 to D1 in the present case, the n^+-doped impurity regions *17b* and *18b* shown in figure 14 of D1 correspond to parts of the first, second and third wiring defined in claim 1 rather than to the fourth semiconductor layer, irrespective of the terminology used in D1 (see [158]).

3.2 Claim 1, D1, undisputed features

The appellant did not dispute that, in the wording of claim 1, the following features were disclosed by the combination of figures 29, 15B and 14 of D1:

A display device comprising a pixel portion and a driver circuit (figure 29, driver circuit to the left, pixel portion to the right),

wherein the pixel portion comprises:

a first thin film transistor *1003* (figure 29) including at least a first semiconductor layer *21* (figure 14D) and a first channel protective layer *15* (figure 14B) in contact with the first semiconductor layer,

wherein the driver circuit comprises:

a second thin film transistor *1002* (figure 29; this TFT corresponds to TFT *34* in figure 15B) including a second semiconductor layer *21* (figure 14D), a first gate electrode *12* (figure 14A), a gate insulating layer *13a/*

13b (figure 14A) and a second channel protective layer *15* (figure 14B) in contact with the second semiconductor layer; and

a third thin film transistor *1001* (figure 29; this TFT corresponds to TFT *33* in figure 15B) including a third semiconductor layer *21* (figure 14D), a second gate electrode *12* (figure 14A), the gate insulating layer *13a/13b* (figure 14A; see also figure 29 showing that the gate insulating layer of the third thin film transistor *1001* is the same as the one of the second thin film transistor *1002*) and a third channel protective layer *15* (figure 14B) in contact with the third semiconductor layer *21*,

wherein the gate insulating layer *13a/13b* is provided on the second gate electrode *12* and the third semiconductor layer *21* is provided on the gate insulating layer *13a/13b* (see figure 14F),

wherein a first wiring *23, 18b* is in contact with one of a source region *20* and a drain region *19* of the second thin film transistor *1002* (in figure 29, that corresponds to the wiring on the right side of TFT *1002*),

wherein a second wiring *23, 18b, 24, 17b* is provided on the gate insulating layer *13a/13b* and in contact with the other of the source region *20* and the drain region *19* of the second thin film transistor (in figure 29, this corresponds to the wiring connecting the TFTs *1001* and *1002*),

wherein the second wiring *23, 18b, 24, 17b* is in direct contact with one of a source region *20* and a drain region *19* of the third thin film transistor *1001*,

wherein a third wiring *24, 17b* is in contact with the other of the source region *20* and the drain region *19* of the third thin film transistor *1001*,

wherein a fourth semiconductor layer *19, 20* (the impurity regions in Figure 14D directly adjacent to the semiconductor channel *21*) is provided between the second wiring *23, 18b, 24, 17b* and the third semiconductor layer *21* and between the third wiring *24, 17b* and the third semiconductor layer *21*, and

wherein each of the first thin film transistor *1003*, the second thin film transistor *1002* and the third thin film transistor *1001* is a n-type transistor (see [269]).

3.3 Claim 1, D1, disputed features (see section VII.(a) above)

3.3.1 In contrast to the features discussed above, the appellant submitted that D1 did not disclose the part of feature g) that the second wiring is

- *in direct contact with the first gate electrode of the second thin film transistor through a first contact hole of the gate insulating layer*.

However, in order to implement an EDMOS circuit as shown in figure 15B, it is inevitable that the wiring that connects the second thin film transistor *34* (*1002* in figure 29) to the third thin film transistor *33* (*1001* in figure 29) is also connected to the gate of the second TFT *34*.
The appellant alleged that this connection to the gate could be implemented in the device disclosed in D1 in some other manner than the one claimed but did not give

any example of such another manner. The Board is not aware of any such other manner, either.
This finding of the Board is in accordance with the argumentations of the Search Division (ESOP dated 3 March 2010, first paragraph of point 3.1) and the Examining Division (communication dated 27 August 2014, point 4.2, last paragraph).

D1 thus implicitly discloses that the second wiring *23, 18b, 24, 17b* is in direct contact with the first gate electrode *12* of the second thin film transistor *34/1002* through a first contact hole of the gate insulating layer *13a/13b*.
Therefore, D1 discloses feature g) in its entirety.

3.3.2 The appellant further disputed that D1 disclosed the part of feature i) that the layer corresponding to the fourth semiconductor layer defined in claim 1 had
- *a smaller thickness and a higher conductivity than the third semiconductor layer*.

The Board concurs with the appellant with respect to the thickness, since D1 is silent about the thicknesses of the different layers with respect to each other.

However, the Board does not agree with the appellant with respect to the conductivity, since the impurity regions *17b* and *18b* shown in figure 14D of D1 are n^+-doped while the channel-forming region *21* is an intrinsic semiconductor region (see [158] and [159]). Thus, the regions *17b* and *18b* have a higher conductivity than the region *21*.

3.4 Differences:
It follows from the above that the subject-matter of claim 1 of the main request differs from D1 by the

following parts of features b1), c1), c2), d) and i) that

1) the channel forming first, second and third semiconductor layers are made from *oxide* semiconductors,

2) the interposed fourth semiconductor layer is made from an *oxide* semiconductor,

3) the fourth semiconductor layer has a *smaller thickness than the third oxide semiconductor layer.*

3.5 Technical effects

The technical effect of feature 1) is that the channel is simpler to manufacture than if it was made from polycrystalline silicon while providing a higher carrier mobility than amorphous silicon. The Board notes that this corresponds to the problem the application aims to solve (see [2] of the description).

The technical effect of feature 2) is linked to the one provided by feature 1) and consists of adapting the material of the layer adjacent to the channel forming layer to the material of the latter layer.

The Board acknowledges that a *reduced overall height* could be considered to be an advantageous technical effect for a TFT, as submitted by the appellant. The absolute thickness of an electrically conductive layer will also have an effect on the electrical resistance of that layer.

In the present case, however, the thickness of the fourth semiconductor layer which is the high conductivity interlayer is not defined in absolute

terms, but only in relation to the thickness of the third oxide semiconductor layer, i.e., the channel forming layer.
A certain *relationship of the thicknesses* of the channel forming layer and the high conductivity interlayer as defined by differentiating feature 3) does not necessarily reduce the overall height of the TFT. Likewise, since differentiating feature 3) does not define the thickness of the fourth semiconductor layer in absolute terms, it does not necessarily influence the electrical resistance of the fourth semiconductor layer.
The Board is also not aware of any other credible technical effect for solving a technical problem achieved by the *relationship of the thicknesses* of the channel forming layer and the high conductivity interlayer.

At the general level and in the relative manner claimed, differentiating feature 3) thus does not per se have a technical effect (as already argued by the Search Division, see ESOP dated 3 March 2010, point 3.2; see also Case Law of the Boards of Appeal, 9th edition 2019, I.D.9.5.).

3.6 Objective technical problem to be solved
The objective technical problem solved by features 1) and 2) can then be formulated as how to provide a TFT with a channel forming layer material that has advantages over silicon.

Feature 3) does not have a technical effect as argued above and therefore does not solve a technical problem.

3.7 Inventive step

As mentioned above, patent document 1 relates to display devices (figure 12) where TFTs that are used for the drive circuit and for the pixel part are formed on the same substrate 700 in a bottom-gate configuration (figure 7) and are provided with a channel protective layer 407 (figures 4 G and 5). Patent document 1 is thus very similar to document D1.

Starting from D1, the skilled person would therefore have consulted this document in order to solve the objective technical problem defined above.

Further, patent document 1 suggests to replace a silicon channel forming layer by an oxide semiconductor channel forming layer ([3] to [7]). The skilled person would thus have been incited by the teaching of this document to replace the silicon semiconductors of the channel forming regions 21 of the various TFTs shown in the figures of D1 by oxide semiconductors as defined in differentiating feature 1).

In addition, the skilled person would have learnt from patent document 1 that an oxide semiconductor (ZnO or IZO) could be used advantageously for forming an electrically conductive layer 411 (1st electrically conductive film) interposed between a channel forming region 409 consisting of an oxide semiconductor and the wiring 412 (2nd electrically conductive film; see [92] and figure 5) according to differentiating feature 2).

Thus, the skilled person, starting from D1, would have considered the teaching of patent document 1 and would have been incited by that teaching to implement differentiating features 1) and 2) into the display device disclosed in figures 29, 14 and 15B of D1.

Feature 3) does not solve a technical problem as argued above and is therefore not taken into account for the purpose of assessing inventive step.

As a side remark, the Board notes that in a vertical arrangement of layers as the one suggested in patent document 1 (figures 5 B and C), the skilled person would have been incited to make the electrically conductive layer 411/415B (first electrically conductive film) in absolute terms as thin as possible in order to reduce its electrical resistance.

It follows from the above that the subject-matter of claim 1 of the main request lacks an inventive step within the meaning of Article 56 EPC.

4. Auxiliary request 1 (see section VII.(b) above)

The Board acknowledges that feature k) is not explicitly mentioned in the available prior art documents, as submitted by the appellant.

However, it was already at the priority date of the present application part of the general knowledge of the skilled person that crystalline semiconductor films are more suitable for use in TFTs than amorphous films (see, for example [4] of patent document 1).

In line with this general knowledge, an originally amorphous semiconductor film is treated such that it crystallises in both D1 (see [6] and [156]) and patent document 1 (see [16]) to make it suitable for use in the TFTs disclosed.
It was further generally known that the electrical properties of a film improve when it is treated such

that its crystallinity improves. This is exemplified in D1 (see [11]) and explicitly disclosed for oxide semiconductors in patent document 1 (see [13]).
It was equally commonly known that low contact resistances were generally beneficial to TFTs; in particular, the aim of lowering the contact resistance is explicitly mentioned in patent document 1 in relation to the layer interposed between the channel forming layer and the wiring (see [90]).

It would thus have been obvious for the skilled person to treat the layer interposed between the channel forming layer and the wiring of any TFT such that it attained a degree of crystallinity and thus conductivity favorable for its purpose. In practice, such a treatment would have resulted in a layer including *crystal grains in an amorphous structure* as required by the additional feature k) of claim 1 of auxiliary request 1.

Concerning the argument of the appellant relating to paragraphs [17] and [18] of the description of the application, the Board notes that these paragraphs relate to the material of the channel forming layer. The argument thus does not apply to the fourth oxide semiconductor layer, which is mentioned in the description only from [22] on.

The additional feature k) of claim 1 of auxiliary request 1 can thus not be considered as justifying the acknowledgement of an inventive step.

Consequently, the subject-matter of claim 1 of auxiliary request 1 is not inventive according to Article 56, either.

5. Auxiliary request 2 (see section VII.(c) above)

The Board acknowledges that the insulating layer 1000 shown in figure 29 of D1 is not in contact with the channel protective layers of the TFTs shown, as submitted by the appellant. However, according to figure 29, the interlayer insulating film 22 (see figure 14E and [161]) corresponding to the layer with the vias arranged on the other side of the TFTs is in contact with all channel protective layers. Thus, contrary to the arguments of the appellant, D1 does disclose feature l) as well.

Further, it is acknowledged that the particular *insulating layer* according to additional feature l) of claim 1 of auxiliary request 2 has the effect that the TFTs arranged beneath that layer are protected from various influences (electrical, mechanical, etc.), as submitted by the appellant.
However, providing such a layer for that very purpose does not go beyond the general knowledge of the skilled person.

Moreover, contrary to the arguments of the appellant, the provision of an insulating layer (passivation films 740 and 741) for this purpose is explicitly disclosed in patent document 1 for TFTs without a channel protective layer (see figure 7 and [113]). Applying such an insulating layer to the TFTs with a channel protective layer as shown in figure 5 of the same document would inevitably bring this insulating layer in contact with the channel protective layers.

It follows from the above that the additional feature l) of claim 1 of auxiliary request 2 is disclosed in D1

and suggested by patent document 1 and therefore does not justify the acknowledgement of an inventive step.

Thus, the subject-matter of claim 1 of auxiliary request 2 does not fulfill the requirements of Article 56 EPC.

6. In view of the above, none of the requests on file fulfills the requirements of the EPC. Consequently, the appeal must fail.

Order

For these reasons it is decided that:

The appeal is dismissed.

The Registrar: The Chairman:

S. Sánchez Chiquero G. Eliasson

Decision electronically authenticated