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Datasheet for the decision of 14 November 2019

Case Number: T 1331/15 - 3.4.03

Application Number: 03800265.5

Publication Number: 1579509

IPC: H01L29/778, H01L21/60, H01L23/36

Language of the proceedings: EN

Title of invention:
GROUP III NITRIDE BASED FLIP-CHIP INTEGRATED CIRCUIT AND METHOD FOR FABRICATING

Applicant:
Cree, Inc.

Headword:

Relevant legal provisions:
EPC 1973 Art. 54(2), 56
EPC Art. 52(1), 123(2)
RPBA Art. 12, 13(1)

Keyword:
Inventive step - (no)
Late-filed auxiliary requests - admitted (no)

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It can be changed at any time and without notice.

Decisions cited:
T 0122/10

Catchword:

This datasheet is not part of the Decision.
It can be changed at any time and without notice.

Beschwerdekammern

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Case Number: T 1331/15 - 3.4.03

D E C I S I O N
of Technical Board of Appeal 3.4.03
of 14 November 2019

Appellant: (Applicant)	Cree, Inc. 4600 Silicon Drive Durham, NC 27703 (US)
Representative:	Elkington and Fife LLP Prospect House 8 Pembroke Road Sevenoaks, Kent TN13 1XR (GB)
Decision under appeal:	**Decision of the Examining Division of the European Patent Office posted on 27 January 2015 refusing European patent application No. 03800265.5 pursuant to Article 97(2) EPC.**

Composition of the Board:

Chairman	G. Eliasson
Members:	S. Ward
	T. Bokor

Summary of Facts and Submissions

I. The appeal is against the decision of the Examining Division refusing European patent application No. 03 800 265 on the grounds that the claimed subject-matter did not meet the requirements of Article 123(2) EPC.

II. At the end of the oral proceedings held before the Board the appellant requested that the decision under appeal be set aside and that a patent be granted on the basis of Claims 1-7 of the main request filed with letter dated 14 October 2019 and re-filed with letter dated 12 November 2019, with the proviso that the feature "through a bonding pad (43)" in line 12 of claim 1 should be considered to be deleted, as discussed during the oral proceedings. Alternatively, the appellant requested that a patent be granted on the basis of any of the first to third auxiliary requests, all filed with letter dated 12 November 2019, or the fourth auxiliary request filed during oral proceedings before the Board.

III. The following documents are referred to:

D3: Ultra-Broadband, Efficient, Microwave Power Amplifiers in Gallium Nitride HEMT Technology; Karthikeyan Krishnamurthy, Dissertation, University of California, Santa Barbara, May 2000; https://www.ece.ucsb.edu/Faculty/rodwell/publications_and_presentations/theses/karthik's_thesis.pdf

D4: EP 0 938 139 A2

D5: Integrated Circuit, Hybrid, and Multichip Module Package Design Guidelines; Michael Pecht; John Wiley and Sons, Inc, 1994, title page, bibliographic page and pages 67-70.

IV. (a) Claim 1 of the main request reads as follows:

"A flip-chip integrated circuit comprising:
a circuit substrate (51, 71, 81, 91) with drive electronics comprising passive components (52, 56, 58, 94, 96) and interconnects (53) on one surface thereof;
an active semiconductor device (32) comprising a substrate (30) with layers of semiconductor material (34, 36) and a plurality of terminals (38, 40, 42), each of said terminals (38, 40, 42) being in electrical contact with one of said layers of semiconductor material (34, 36), said active semiconductor device (32) being flip-chip mounted on said circuit substrate (51, 71, 81, 91), at least one of said terminals (38, 40, 42) being in electrical contact with said passive components and interconnects (52, 53);
a conductive via (61, 62; 88, 86) through said circuit substrate, the conductive via being in electrical contact with one of said plurality of terminals (38, 40, 42) through the bonding pad (43) and comprising a hole through said circuit substrate, the surface of the hole being covered by a first layer (62, 86) of conductive material;
a first heat sink base plate coupled to a first heat sink;
and a second layer (89) of conductive material, on the surface of said circuit substrate opposite said passive components and interconnects (52, 53), arranged adjacent to said first heat sink base plate and in electrical and thermal contact with said first layer

(86) of conductive material, said second layer of conductive material forming a ground for said via and for dissipating heat from said active semiconductor device."

As noted above, the phrase "through a bonding pad (43)" which appeared in line 12 of the claim as filed has been deleted, in accordance with the request of the appellant at oral proceedings.

(b) Claim 1 of the first auxiliary request adds to claim 1 of the main request the features:

"wherein the first and second layers of conductive material are arranged so that heat from said first and second layers flows into the first heat sink base plate; and
the first heat sink base plate is arranged so that heat from the first heat sink base plate flows into the first heat sink where it is dissipated."

(c) Claim 1 of the second auxiliary request adds to claim 1 of the main request the feature:

"wherein the conductive via further comprises a plug (84) of conductive material at the top of said via."

(d) Claim 1 of the third auxiliary request adds to claim 1 of the main request both of the features mentioned under (b) and (c), above.

(e) In claim 1 of the fourth auxiliary request (compared to claim 1 of the main request) the following features have been deleted:

"at least one of said terminals (38, 40, 42) being in electrical contact with said passive components and interconnects (52, 53)"; and

"the surface of the hole being covered by a first layer (62, 86) of conductive material";

and the following feature has been added:

"wherein the conductive via further comprises a plug (84) of conductive material at the top of said conductive via with the top surface of the plug being at the top surface of the circuit substrate 81, wherein the first layer (62, 86) of conductive material covers the inside of the hole and the bottom surface of the plug".

V. The appellant's arguments, insofar as they are relevant to the present decision, may be summarised as follows:

The principal distinguishing features of the main request over the closest prior art (D3) were as follows: a thermally and electrically conductive via coupled to one of the bonding pads used for the flip-chip bonding and to a ground plane on the opposite side of the circuit substrate, the ground plane being positioned adjacent to a heat sink base plate and a heat sink, so that the conductive via dissipated heat through the heat sink.

The invention thus allowed the dissipation of heat from flip-chip mounted active semiconductor devices. D3 did not disclose the formation of a via, nor the use of vias to assist in thermal dissipation, which made sense in the case of D3 because of the low impedance thermal path of the AlN substrate.

The electrical grounding arrangement set out in claim 1 was not disclosed in D3, in which the grounding of the source was by means of ground plates on the opposite side of the circuit substrate to that of the heat sink. The heat sink of D3 would presumably be grounded in some other way.

The invention defined in claim 1 therefore solved two problems: dissipating heat from flip-chip mounted active semiconductor devices, and providing effective grounding for the flip-chip integrated circuit.

The skilled person might have a general knowledge of electrically conductive vias for forming ground and signal connections through substrates, and of thermal vias providing both electrically and thermally conductive paths through a substrate, but it would have taken an inventive step to apply this knowledge to the solution of the problem in the case of the flip—chip device of document D3, in which there was no hint of vias nor of a heat sink in the end product providing heat dissipation.

There was also no indication in the other prior art that a conductive via could simultaneously act as both an electrical connection to ground and a thermal connection to a heat sink. D4 did not disclose using a thermally conductive via to dissipate heat. Document D5 also failed to disclose the feature of a conductive via that acts both to dissipate heat to a heat sink and to electrically connect to ground. The phrase "low resistance" (page 70, second paragraph, final sentence) did not unambiguously refer to electrical resistance as opposed to thermal resistance.

D3 did not in fact disclose that the device as manufactured had a heat sink; the Cu heat sink was only provided for testing purposes and not as part of the eventual production process; it was not disclosed that such a device would incorporate a heat sink in operation.

VI. The Board sent a communication under Article 15(1) RPBA setting out its provisional views on the main and auxiliary requests then on file.

Reasons for the Decision

1. The appeal is admissible.

2. *Main Request: Inventive Step*

2.1 Both the Examining Division and the appellant have based their analyses of inventive step on D3, and the Board also sees this document as a suitable starting point. In the terminology of claim 1 of the present application, D3 discloses:

a flip-chip [section 4.2.8] integrated circuit comprising:
a circuit substrate [section 4.2] with drive electronics comprising passive components [sections 4.2.1 and 4.2.3] and interconnects [section 4.2.2] on one surface thereof;
an active semiconductor device [section 4.1 and Fig. 4.1] comprising a substrate with layers of semiconductor material [Fig. 4.1] and a plurality of terminals [sections 4.1.2 and 4.1.3], each of said

terminals being in electrical contact with one of said layers of semiconductor material, said active semiconductor device being flip-chip mounted [section 4.2.8] on said circuit substrate, at least one of said terminals being in electrical contact with said passive components and interconnects [sections 4.2.1 to 4.2.4, and 4.2.8].

2.2 Moreover, D3 discloses [section 4.2.8, final sentence, and the passage bridging pages 167, 168] a Cu block acting as a heat sink which is bonded to the AlN circuit substrate by means of a "thin layer of silver epoxy" (which is well known to be conductive). It is implicit that the Cu block is bonded to the side of the AlN substrate opposite that to which the GaN die is bonded. Hence, in the terminology of claim 1, D3 also discloses:

a first heat sink base plate [the Cu block] ... and a second layer of conductive material [the layer of silver epoxy], on the surface of said circuit substrate opposite said passive components and interconnects, arranged adjacent to said first heat sink base plate.

2.3 The Board is not persuaded by the appellant's argument that D3 fails to disclose a device comprising a heat sink, since the heat sinking Cu block is (in the appellant's view) present only in a testing phase, and not in the final product.

D3 is a doctoral dissertation describing *inter alia* the manufacture and testing of microwave power amplifiers. There appears to be no indication in D3 whether the disclosed devices have been created only as part of an academic project or whether they are intended to be developed into "final products", and if so, whether

such final products would differ from those actually disclosed. For present purposes, however, this is irrelevant.

According to Article 54(2) EPC 1973, the state of the art comprises "everything made available to the public ... before the date of filing of the European patent application". D3 makes available to the public a flip-chip integrated circuit having the features recited above, including a Cu block acting as a heat sinking means.

2.4 In the light of the above, claim 1 of the main request differs from D3 in the following respects:

(a) providing "a conductive via (61, 62; 88, 86) through said circuit substrate, the conductive via being in electrical contact with one of said plurality of terminals (38, 40, 42) through the bonding pad (43) and comprising a hole through said circuit substrate, the surface of the hole being covered by a first layer (62, 86) of conductive material";

(b) the first heat sink base plate being "coupled to a first heat sink";

(c) the second layer being "in electrical and thermal contact with said first layer (86) of conductive material";

(d) "said second layer of conductive material forming a ground for said via"; and

(e) the second layer being "for dissipating heat from said active semiconductor device".

2.5 According to the application, features (a) and (d) taken together provide two technical effects, in that "the vias form a conductive path to ground for an active semiconductor device that is flip-chip mounted ... and they also promote the device's heat dissipation" (page 11, lines 1-5; page 16, lines 11-18). The appellant therefore argues that the claimed vias solve two problems: one thermal and the other electrical.

2.6 The Board cannot agree with this analysis. In the description, the heat dissipation provided by the conductive vias is said to be "particularly useful for GaAs and Si substrates that have relatively low thermal conductivity" (page 16, lines 16-18, and see also page 9, lines 25-29). Claim 1, however, does not specify any particular material for the circuit substrate, and hence includes materials having a high thermal conductivity, such as the AlN substrate disclosed in D3 (see page 39, first paragraph).

Moreover, the claimed conductive via comprises "a hole through said circuit substrate, the surface of the hole being covered by a first layer of conductive material". This includes embodiments in which the hole comprises mainly air (as depicted, for example, in Fig. 5). The Board sees no reason to believe that a via comprising a through-hole filled mainly with air would improve the thermal conductivity of a substrate made of AlN; the opposite would appear to be more likely.

2.7 In the problem-solution approach, the objective problem should be one which is plausibly solved over essentially the entire breadth of the claim. In the present case, the Board is of the view that the

invention, in the manner in which it is defined in claim 1, does not represent a plausible solution to the problem of providing a circuit substrate with improved thermal conduction or heat dissipation.

2.8 Concerning the proposed electrical problem, the appellant did not challenge the point made in the Board's communication (point 4.2) that a heat sink would, in practice, be maintained at ground potential, but argued that, starting from D3, it would not be obvious to provide such grounding in the claimed manner. The problem can therefore be seen as providing a suitable electrical ground connection for the Cu block.

2.9 At the priority date of the present application the skilled person would have been well aware that conductive vias were commonly used for extending a ground connection from a conductive element on one side of a dielectric substrate to a conductive element on the opposite side, as shown, for example, in Fig. 1B of D4.

Hence, starting from D3, and faced with the above objective problem, it would be obvious for the skilled person to extend a conductive via from a ground plane on the surface of the circuit substrate having the passive components and interconnects through the AlN substrate to make an electrical connection with the Cu block, or at least with the layer of silver epoxy which is in electrical connection with the Cu block. In this way the layer of silver epoxy ("said second layer of conductive material") would form a ground "for said via" (i.e. the second layer of conductive material would be at ground potential and connected to the via).

2.10 Various types of conductive vias were known at the priority date, and the choice of a via in which the internal surface of the via hole is covered by conductive material, as opposed to, for example, a completely solid conductive via, is not seen as inventive, nor has this been argued by the appellant.

2.11 In the circuits of D3 the source is grounded (see e.g. Figs. 2.1, 2.3, 2.6, 5.2 etc.), being connected to a ground plane on the side of the circuit substrate having the passive components and interconnects (see section 4.2.4, Fig. 4.7). This was not disputed by the appellant. Moreover, the active semiconductor terminals, or at least the source terminal (see page 45, section 4.1.6, third bullet point) are flip chip bonded to the circuit substrate via bonding pads, hence the source terminal is connected to a ground plane via a bonding pad.

The Board concluded above that it would be obvious for the skilled person to provide a conductive via extending through the substrate and connected to a ground plane on the surface of the circuit substrate having the passive components and interconnects, and it therefore follows that such a via would be in (grounded) electrical contact with the source terminal of the active device through the bonding pad.

2.12 The Board accepts that the use of a conductive via would not be the only obvious solution to the problem of grounding the Cu block. A separate external ground lead or some form of grounding via the probe station (page 52, section 4.2.8, final sentence) would also be evident possibilities. However, the choice of one known measure (in this case, a conductive via) from among a

limited number of obvious possibilities cannot be considered to involve an inventive step.

2.13 On the basis of the above considerations the Board concludes that, starting from D3, and faced with the problem of providing a suitable ground connection for the Cu block, it would be obvious for the skilled person, to arrive at features (a) and (d).

2.14 Features (c) and (e) would then follow naturally from such a choice: the conductive material covering the surface of the via hole (the "first layer of conductive material") would be in electrical (and thermal) contact with the layer of silver epoxy (the "second layer of conductive material"), and the second layer (being in electrical, and hence thermal, contact with the source) would, in practice, dissipate a certain amount of heat (i.e. be *suitable* "for dissipating heat") from the active semiconductor device.

2.15 The remaining distinguishing feature is (b), i.e. the first heat sink base plate being "coupled to a first heat sink". In the application, no clear technical or functional distinction is made between the "heat sink base plate" (which clearly has a heat-sinking function), and the "heat sink" *per se*. The "heat sink" is not depicted in any drawing and the description merely notes: "Heat from the first base plate 114 then flows into an external heat sink (not shown) where it is dissipated" (page 19, lines 11-13).

2.16 A typical heat sink may comprise a thermally conductive plate, to be set in contact with the surface to be cooled, and an arrangement of fins or other protrusions attached on the opposite side of the plate, to facilitate heat dissipation. Providing the Cu block of

D3 with such an arrangement of fins would therefore be a routine measure for the skilled person to improve heat dissipation. Given that the application does not define precisely what is meant by a "heat sink" (as opposed to a "heat sink base plate"), such an arrangement of fins could perfectly plausibly be referred to as the "heat sink", which would be coupled to the heat sink base plate (i.e. the Cu block). Hence it would be obvious for the skilled person to arrive at feature (b).

2.17 In the light of the above considerations, the Board judges that the subject-matter of claim 1 of the main request does not involve an inventive step within the meaning of Article 52(1) EPC and Article 56 EPC 1973.

3. *Auxiliary Requests*

The first to third auxiliary requests were filed with the letter dated 12 November 2019, hence two days before the oral proceedings. The fourth auxiliary request was filed during the oral proceedings. These amendments to the appellant's case may only be admitted and considered at the Board's discretion according to Article 13(1) RPBA, which states the following:

"Any amendment to a party's case after it has filed its grounds of appeal or reply may be admitted and considered at the Board's discretion. The discretion shall be exercised in view of inter alia the complexity of the new subject matter submitted, the current state of the proceedings and the need for procedural economy."

4. *First Auxiliary Request*

4.1 In deciding whether to admit late-filed requests into the procedure the boards routinely apply the criterion of "clear allowability", which is to say that a request will only be admitted if it can be quickly ascertained that it overcomes all outstanding objections under the EPC and does not give rise to new objections (see *Case Law of the Boards of Appeal*, 9th edition, 2019, IV.E. 4.4.2a)).

4.2 In the present case, claim 1 of the first auxiliary request comprises the following features additional to those of claim 1 of the main request:

"wherein the first and second layers of conductive material are arranged so that heat from said first and second layers flows into the first heat sink base plate; and
the first heat sink base plate is arranged so that heat from the first heat sink base plate flows into the first heat sink where it is dissipated."

4.3 It is not immediately apparent that these features overcome the objection of lack of inventive step, or even that they represent any further technical limitation. In fact, they simply appear to define technical effects (in terms of heat flows) which would be expected to arise from the arrangement defined in claim 1 of the main request.

4.4 Furthermore, the basis given by the appellant for this feature (page 19, lines 8-13) is from a passage describing the embodiment depicted in Fig. 10. It is not immediately apparent that this feature can be incorporated into claim 1 while omitting other features of the disclosed embodiment (for example, the material

of the substrate) without contravening the requirements of Article 123(2) EPC.

4.5 The Board therefore judges that claim 1 of the first auxiliary request does not meet the criterion set out above under point 4.1, and hence this request is not admitted into the procedure pursuant to Article 13(1) RPBA.

5. *Second Auxiliary Request*

5.1 The feature in claim 1 as filed with the statement of grounds of appeal that "said at least one conductive via comprises a plug of conductive material at a top end of said conductive via to enhance heat dissipation" was seen as key to establishing an inventive step over the prior art (see page 2 of the statement, "Response to Paragraph 16 of the Decision"). In the procedure before the department of first instance, the corresponding "plug" feature in the independent claims as refused was also seen as crucial (see the letter dated 17 December 2014, page 2, "Inventive Step").

Following the Board's communication, a new request was filed with the letter dated 14 October 2019, the letter stating that the new "sole request replaces the previous main and auxiliary requests." The independent claims of this request omitted any mention of a plug, the appellant choosing to define the invention in terms of other features.

5.2 Given that the appellant chose, at this point of the procedure, to withdraw all previous requests in which a plug was defined in the independent claims, the Board does not consider that it is consistent with the requirement for procedural economy pursuant to Article

13(1) RPBA to admit a new request filed two days before oral proceedings in which the plug feature is reinstated into the independent claims.

5.3 Although not specifically raised by the appellant, the Board has considered the argument that an appellant should be allowed to return to its original appeal case by virtue of the provisions of Article 12 RPBA. Whatever the merits of such an argument in general, it does not, for the following reasons, apply in the present case.

Firstly, the independent claims of the present second auxiliary request are not identical to any filed with the grounds of appeal. Secondly, to the extent that Article 12(4) RPBA requires the Board to take into account everything presented with the grounds of appeal (including any requests), this provision can only be understood to apply if such requests have not previously been withdrawn in the course of the proceedings; once the appellant elects to withdraw its earlier filed requests, the provisions of Article 13(1) RPBA apply (see T 122/10, Reasons, point 3.7).

5.4 The second auxiliary request is therefore not admitted into the proceedings pursuant to Article 13(1) RPBA.

6. *Third and Fourth Auxiliary Requests*

Claim 1 of the third auxiliary request comprises the feature "wherein the conductive via further comprises a plug (84) of conductive material at the top of said via". Claim 1 of the fourth auxiliary request comprises essentially the same feature (the word "conductive" being inserted before the final "via").

6.1 The third and fourth auxiliary requests are therefore not admitted into the proceedings pursuant to Article 13(1) RPBA for the reasons explained above in relation to the second auxiliary request, *mutatis mutandis*.

7. The main request being judged not to meet the requirements of Article 52(1) EPC and Article 56 EPC 1973, and the first to fourth auxiliary requests not being admitted into the proceedings pursuant to Article 13(1) RPBA, the appeal must fail.

Order

For these reasons it is decided that:

The appeal is dismissed.

The Registrar: The Chairman:

S. Sánchez Chiquero G. Eliasson

Decision electronically authenticated