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Datasheet for the decision of 19 February 2020

Case Number: T 1265/15 - 3.5.06

Application Number: 03717501.5

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Language of the proceedings: EN

Title of invention:
AN ADDRESS GENERATION UNIT FOR A PROCESSOR

Applicant:
Telefonaktiebolaget LM Ericsson (publ)

Headword:
Processor address generation unit/ERICSSON

Relevant legal provisions:
EPC 1973 Art. 54, 56, 111(1)
RPBA 2020 Art. 11

Keyword:
Novelty - (yes)
Inventive step - (yes)
Remittal to the department of first instance - (yes)
Special reasons for remittal - (yes)

Decisions cited:

Catchword:

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Beschwerdekammern

Boards of Appeal

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Case Number: T 1265/15 - 3.5.06

D E C I S I O N
of Technical Board of Appeal 3.5.06
of 19 February 2020

Appellant: (Applicant)	Telefonaktiebolaget LM Ericsson (publ) 164 83 Stockholm (SE)
Representative:	Ericsson Patent Development Torshamnsgatan 21-23 164 80 Stockholm (SE)
Decision under appeal:	**Decision of the Examining Division of the European Patent Office posted on 9 February 2015 refusing European patent application No. 03717501.5 pursuant to Article 97(2) EPC.**

Composition of the Board:

Chairman	M. Müller
Members:	A. Teale
	A. Jimenez

Summary of Facts and Submissions

I. This is an appeal against the decision, dispatched with reasons on 9 February 2015, to refuse European patent application No. 03 717 501.5 on the basis that the subject-matter of claim 1 according to a main and two auxiliary requests was not new, Article 54(1,2) EPC, in view of the following document:

D1: WO 99/14663 A2.

II. A notice of appeal and the appeal fee were received on 8 April 2015. The appellant requested that the decision be set aside and that a patent be granted.

III. With a statement of grounds of appeal, received on 8 June 2015, the appellant submitted claims according to a main and five auxiliary requests and requested that the decision be set aside and that the application be granted based on said main or one of said auxiliary requests. The appellant also requested oral proceedings if the board was minded to uphold the decision.

IV. The application is thus being considered in the following form:

Description (all requests):
page 1, received on 6 February 2009,
pages 2, 2a and 4, received on 16 October 2009, and
pages 3 and 5 to 22, as originally filed.

Claims (all received with the grounds of appeal):
Main request: claims 1 to 10.
First auxiliary request: claims 1 to 10.
Second auxiliary request: claims 1 to 10.

Third auxiliary request: claims 1 to 9.
Fourth auxiliary request: claims 1 to 9.
Fifth auxiliary request: claims 1 to 9.

Drawings (all requests):
Pages 1/4 to 4/4, as originally filed.

V. Claim 1 of the main request reads as follows:

"A processor (120) including: a memory port for accessing a physical memory (410) under control of an address; at least one processing unit (450) for executing instructions stored in the memory (410) and/or operating on data stored in the memory (410); at least one address generation unit (420) for generating an address for controlling access to the memory (410); the address generation unit (420) being associated with at least a first set of a plurality of N registers (710-717), where the set of registers enables the address generation unit (420) to generate the address under control of an address generation mechanism; characterised in that: a memory unit (400) operative to save/load k of the N registers (710-717) that are used for address generation, where 2<=k<=N, triggered by one operation, where the memory unit (400) includes a concatenator for concatenating the k registers to one memory word to be written to the memory through the memory port and a splitter for separating a word read from the memory (410) through the memory port into the k registers; wherein the processor (120) is operative to operate on operands with a smallest size of one processor word and the memory word has a width of a multiple of the processor word size; and the concatenator is operative to map the registers to boundaries in the memory that correspond to the processor word."

In view of the board's decision, the wording of claim 1 according to the auxiliary requests is immaterial.

Reasons for the Decision

1. The admissibility of the appeal

In view of the facts set out at points I to III above, the appeal fulfills the admissibility requirements under the EPC and is consequently admissible.

2. A summary of the invention

2.1 The invention relates to a processor having a memory for storing instructions and/or data; see figure 1; 120. The width of a memory word is sufficient to hold several processor words, each being suitable, for instance, for storing an operand. As shown in figure 3, the processor supports a variety of different word sizes, the data and memory width preferably being 32 (single) words (W), but could, for example, also be sixteen double words (DW) or eight quad words (QW).

2.2 The memory address is produced by an address generation unit (AGU), also termed an address computation unit (ACU); see figure 4; 420 and page 7, lines 1 to 3. The AGU is associated with a plurality of N registers (see figure 6; 610 and figure 7; 710 to 717), the values in k of the registers being concatenated to yield a memory address, where $2 \leq k \leq N$. A splitter is also provided for separating a word read from the memory into input words for the registers. Thus the concatenator and splitter map a plurality of AGU registers to one memory word; see figure 5 and page 14, lines 15 to 22.

2.3 The invention addresses the problem that, as the performance of such processors increases, the time required to configure the AGU registers is becoming a bottleneck; see page 2a, lines 3 to 5. Page 13, lines 3 to 4, defines "configuring" the ACU/AGU as initialising the set of registers, for instance prior to a program loop. The invention reduces the number of clock cycles required to configure the AGU registers; see page 14, lines 3 to 10.

3. Document D1

3.1 As illustrated in figure 1 (see also page 3, line 28, to page 4, line 19), D1 relates to a CPU (Central Processing Unit) comprising a memory (1) having a first 64-bit data bus composed of two 32-bit words connected to a "register load and store buffer" (also termed the "register file") (2) containing a plurality of registers (2b, D0-D15). According to the sentence bridging pages 3 and 4, D1 uses the term "word" to mean 32 bits, "half-word" to mean 16 bits and "byte" to mean 8 bits.

3.2 The registers are organized in two groups referred to as "even" registers (D0, D2, ... D14) and "odd" registers (D1, D3, ... D15). The CPU also comprises a load/store control unit (2d) for addressing the memory and selecting the respective registers (2b) during data transfers (read or write) between the register file (2) and the memory (1).

3.3 The connection between the memory and the registers is managed by a first buffer/select logic (2a), whilst the connection between the registers and a second bus (3) is managed by a second buffer/select logic (2c). Thus

an even and an odd register can be accessed simultaneously; see page 4, lines 17 to 19. Figure 2 illustrates the structure of the buffer/select logic (2a) which provides memory access to two consecutive words at a time (e.g. 1e/1f, or 1f/1g); see page 5, last line, to page 6, line 16. The board understands figure 2 to contain an error, since, taken at face value, no data reaches the input of multiplexer/ splitter unit 9. The board understands D1 in the sense that, like the arrow (1a) from the bottom left of the memory to the input of multiplexer/splitter unit 8, there should also be an arrow (1d) from the bottom right of the memory to the input of multiplexer/ splitter unit 9. This interpretation is confirmed by the references on page 4, lines 23 to 29, to the "first" (1a) and "second" (1d) sets of data output lines.

3.4 Either of the two 32-bit memory words can be routed via the multiplexer/splitters (8,9) and the alignment units (12,13) to any one of the even or odd registers. Equally, in the other direction, any one of the even or odd registers can be connected via the concatenation units (11,14) and the multiplexers (7,10) to either of two consecutive 32-bit memory words; see page 4, line 20, to page 5, line 2.

3.5 The description refers to the "store double word from data registers" instruction; see page 7, line 28, to page 8, line 4. This instruction corresponds to the "load double word to a register" instruction (see page 5, lines 14 to 28) and causes the 32-bit content of an even and an odd register to be routed to consecutive 32-bit memory locations. According to page 5, lines 3 to 13, the use of a single memory in this way allows two 32-bit data words to be transferred per clock

cycle, the only proviso being that they are stored in consecutive order in memory (1).

3.6 Figure 7 relates to the use of certain registers as a circular buffer for filter calculations, three further registers (31a-c) being used by a circular buffer control unit (32) coupled to a load/store control unit (33) to select the next register to be addressed; see page 10, line 7, to page 11, line 23. The address of the selected register is derived by adding an incremented index (31b), which resets to zero when it reaches the buffer length (31a), to the fixed base address (31c).

3.7 Figure 8 shows a modified circular buffer arrangement adapted for FFT (Fast Fourier Transform) calculations which steps through the circular buffer in increments of varying size; see page 12, lines 4 to 13. Figure 9 illustrates a circular buffer structure adapted for implementing a FIR (Finite Impulse Response) filter; see page 13, lines 5 to 22.

4. Novelty, Article 54(1,2) EPC 1973, in view of D1

4.1 According to the appealed decision, the subject-matter of claim 1 according to *inter alia* the main request is not new, Article 54(1,2) EPC, in view of D1. Claim 1 of the present main request is the same as that of the main request in the decision.

4.2 The reasons given in the decision (points 12 to 12.4) regard the "LOAD/STORE CONTROL UNIT" (2d) in figure 1 of D1 as the "processing unit ... for executing instructions stored in the memory and or operating on data stored in the memory" set out in claim 1. The "CIRCULAR BUFFER CONTROL UNIT" (32) in figure 7 of D1

and the adders (36, 38) in figure 8 of D1 are regarded as the "address generation unit for generating an address for controlling access to the memory" set out in claim 1. The reasons (see point 12.3) also point to registers 31a and 31b in figure 7 as being address registers forming part of an "address generation unit", set out in claim 1. The register file (2) in figure 2 of D1 (the board understands this as "2b" in figure 2) is regarded as a first set of a plurality of registers set out in claim 1. The select/concatenate units (11,14) and multiplexers (7,10) shown in figure 2 of D1 are regarded as the concatenator set out in claim 1, whilst the multiplexer/splitter units (8,9) and alignment units (12,13) are regarded as the splitter set out in the claim.

4.3 The appellant has argued that the expression "address generation unit" in claim 1 does not cover the circular buffer control unit 32 in D1 because the "address generation unit" (AGU/ACU) in the application forms part of a CPU. The board does not accept that this is a technical difference. The application relates to an address generation unit for a processor (see page 1, line 3), claim 1 of the main request setting out a "processor". D1 discloses a DSP (Digital Signal Processor), a type of processor, comprising the circular buffer control unit; see page 10, lines 17 to 25.

4.4 D1 does not however disclose the feature in claim 1 of the main request that the address generation unit is "for generating an address for controlling access to the memory", since in D1 the register file (2), which is addressed according to the output of the buffer control unit (32) (see figure 7), is distinct from the memory (1).

4.5 Claim 1 of the main request sets out a memory unit operative to save/load k of the N registers that are used for address generation, where $2 \leq k \leq N$. This feature is known from D1 which discloses sixteen registers (N=16) in figure 1 (D0-D15) and, regarding the circular buffer control unit 32 in D1 as an "address generation unit", registers 31a-c form a first set of three registers (k=3), thus satisfying the restriction $2 \leq k \leq N$. The skilled person would recognise that each of the registers 31a-c in D1 must be either read from or written to either before or during the operation of the circular buffer.

4.6 However, as the appellant has argued (see grounds, page 3, lines 8 to 5 from the bottom), there is no disclosure in D1 of the content of the registers (31a-c) used for address generation being stored in or loaded from the memory (1). Furthermore the content of the three registers 31a-c is neither concatenated nor split in D1. Hence D1 does not disclose the feature in claim 1 of the main request that

"the memory unit (400) includes a concatenator for concatenating the k registers to one memory word to be written to the memory through the memory port and a splitter for separating a word read from the memory (410) through the memory port into the k registers".

4.7 Hence the subject-matter of claim 1 of the main request is novel, Article 54(1,2) EPC 1973, with regard to the disclosure of D1.

5. Inventive step, Article 56 EPC 1973, in view of D1

5.1 The objective technical problem starting from D1 can be seen as "configuring", in other words "initialising", the values in the three registers (31a-c) used for register address generation. The board is unaware of what would have led the skilled person starting from D1 to the subject-matter of claim 1 of the main request in an obvious manner. In particular, D1 provides no hint at storing the content of registers 31a-c in memory. Alternatively, one might consider the more specific problem of configuring the three registers when switching between sub-tasks, as mentioned in the application (page 2, line 9), this problem not being specifically mentioned in D1. While it would have been obvious when addressing this problem to store the content of these registers in memory, D1 still does not disclose or suggest using dedicated concatenation and splitter hardware to speed up register initialisation. The board also considers that, while D1 discloses instructions and associated hardware for concatenating register content before storing it in memory and for splitting it on retrieval, D1 does not disclose or suggest using these on the content of registers 31a-c.

5.2 Consequently the subject-matter of claim 1 of the main request involves an inventive step, Article 56 EPC 1973, in view of D1.

6. Remittal, Article 111(1) EPC 1973

6.1 As set out above, the subject-matter of claim 1 of the main request is novel in view of the disclosure of D1, thus overcoming the reasons for refusal given in the decision. The board also finds that claim 1 involves an inventive step in view of D1.

6.2 As the board bases these findings on a different interpretation of D1 to that in the decision, the board judges it appropriate to remit the case to the examining division for further prosecution, so that it has the opportunity to reassess the invention in view of the other prior art on file. These circumstances constitute special reasons within the meaning of Article 11 RPBA 2020.

Order

For these reasons it is decided that:

The decision is set aside.
The case is remitted to the department of first instance for further prosecution.

The Registrar: The Chairman:

L. Stridde M. Müller

Decision electronically authenticated