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Case Number: T 2312/14 - 3.4.03

Application Number: 10196317.1

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Language of the proceedings: EN

Title of invention:
Methods of fabricating silicon carbide devices having channel regions with a smooth surface

Applicant:
Cree, Inc.

Headword:

Relevant legal provisions:
EPC 1973 Art. 56, 76(1)
EPC Art. 52(1), 123(2)

Keyword:
Inventive step - after amendment - (yes)

Decisions cited:

Catchword:

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Case Number: T 2312/14 - 3.4.03

D E C I S I O N
of Technical Board of Appeal 3.4.03
of 22 November 2018

Appellant: (Applicant)	Cree, Inc. 4600 Silicon Drive Durham, NC 27703 (US)
Representative:	Boult Wade Tennant LLP Verulam Gardens 70 Gray's Inn Road London WC1X 8BT (GB)
Decision under appeal:	**Decision of the Examining Division of the European Patent Office posted on 23 July 2014 refusing European patent application No. 10196317.1 pursuant to Article 97(2) EPC.**

Composition of the Board:

Chairman	G. Eliasson
Members:	S. Ward
	C. Heath

Summary of Facts and Submissions

I. The appeal is against the decision of the Examining Division refusing European patent application No. 10 196 317 on the grounds that the claimed subject-matter did not involve an inventive step within the meaning of Article 56 EPC (main request) and did not meet the requirements of Article 76(1) EPC (auxiliary request).

II. At the end of the oral proceedings held before the Board the appellant requested that the decision under appeal be set aside and that a patent be granted based on the main request, filed with letter dated 22 October 2018, or on the "New 1st Auxiliary Request" (claims 1-10 and an amended description comprising pages 1-5 and 9-21, pages 6-8 being deleted) filed during oral proceedings, or on the 1st or 2nd Auxiliary Request filed with letter dated 22 October 2018 (which now form the current 2nd and 3rd auxiliary requests).

III. The following documents are referred to:

D1: US 6 573 534 B1
D2: EP 1 306 890 A2
D4: JP 2000 082812 A
(a computer generated translation of D4, a copy of which was sent to the appellant, has been used to interpret this document)
D7: Modern Power Devices; B Jayant Baliga; John Wiley & Sons, 1987; title page, bibliographic page, pages 12-15.
D8: US 6 107 142 A

IV. (i) Claim 1 of the main request reads as follows:

"A silicon carbide power device, comprising:
an n^--type silicon carbide drift layer (10, 12);
a p-type conductivity silicon carbide well region (14) on the n^--type silicon carbide drift layer (10, 12);
a buried p^+ conductivity silicon carbide region (18) in the p-type conductivity silicon carbide well region (14);
an n^+ conductivity silicon carbide region (20) directly on the buried p^+ conductivity silicon carbide region (14);
a channel region (29) of the power device comprising a first portion that is adjacent the buried p^+ conductivity silicon carbide region (18) and n^+ conductivity silicon carbide region (20) and a second portion comprising an n^- silicon carbide region (19') on the first portion of the channel region (29);
wherein the channel region (29) of the power device has a root mean square (RMS) surface roughness of less than 0.1 nm (1.0 Å)".

(ii) Claim 1 of the 1st auxiliary request is the same as that of the main request except for the following additional feature:

"the n^- silicon carbide region (19') being not present on the n^+ conductivity silicon carbide region".

V. The appellant's arguments, insofar as they are relevant to the present decision, may be summarised as follows:

The SiC power device of claim 1 of the main request had a channel region with an RMS surface roughness of less than 0.1 nm, which served to decrease the on resistance and increase the reliability of the device.

Even if it were considered to be common general knowledge that a low surface roughness would lead to such an effect (which the appellant disputed), no suitable method for achieving such a roughness in a SiC power device was known. The skilled person would therefore look to other ways of improving the reliability/on resistance of a SiC power device.

A roughened surface comprised "peaks" and "valleys". In order to smooth a roughened surface there were two alternative options: (1) remove the peaks (e.g. by grinding, polishing etc.), or (2) "fill in" the valleys and then smooth the final surface. The prior art used "peak removal" techniques ("Option 1"), which required the removal of a large amount of material. For example, as discussed on page 19, lines 4-8 of the description, CMP typically removed several microns of film. Such techniques were not appropriate to smooth a channel region in a SiC power device, because various device layers, would have a thickness of only a few angstroms, and would therefore be completely removed, rendering the device non-functional.

According to the present invention, the low roughness value was achieved by the use of a "two step" smoothing process (i.e. "Option 2"), with an n^- region being formed on the channel region and then smoothed by the use of a "peak removal" technique (e.g. chemical mechanical polishing) capable of achieving the low roughness value claimed.

Reasons for the Decision

1. The appeal is admissible.

2. *Main request: Article 76(1) EPC 1973 and 123(2) EPC*

2.1 Claim 1 of the present main request is essentially the same as claim 1 of the main request on which the contested decision was based. The Examining Division found (Grounds for the decision, point 1) that this subject-matter did not extend beyond the contents of the parent application as filed (EP 06 738 542, derived from the PCT application published as WO 2006/127093 A2), and therefore met the requirements of Article 76(1) EPC 1973. The Board sees no reason to question this finding. Dependent claims 2-10 are also considered to be fairly based on the parent application as filed.

2.2 In the present case, the original claims were filed after the date of filing of the application (Rule 68(4) EPC). However, claims 1-31 of the parent application are included in the description of the application as filed, being referred to as "clauses". The remainder of the description is essentially identical to that of the parent application, and the drawings are also identical. Hence, the entire contents of the parent application as filed is comprised in the present application as filed. In view of the findings of the previous paragraph, the requirements of Article 123(2) EPC are considered to be met.

3. *Main request: Inventive step*

3.1 Both the examining division and the appellant considered that the closest prior art for claim 1 of the main request was the fourth embodiment (Figs. 7-10) of document D4 (JP 2000 082812 A), and the Board sees no reason to differ (it is noted that this document was

referred to as D5 in the procedure relating to the parent application).

3.2 The appellant does not dispute the finding of the Examining Division that the subject-matter of claim 1 differs from the closest prior art only in that the channel region has a root mean square surface roughness of less than 1.0 Å.

3.3 The problem may be seen as improving the device performance, for example in terms of on-resistance (see e.g. page 3, lines 8-11).

3.4 In the opinion of the Board, it was common general knowledge in the art at the priority date of the present application that, in a MOSFET device such as that of D4, reducing the surface roughness of the interface between the channel region and the gate oxide layer served to increase the carrier mobility in the channel and thereby improved device performance (for example, the on-resistance). This is reflected in, for example, document D7 (an excerpt from a well-known textbook in the field, published in 1987), which describes the influence of the surface roughness of a metal oxide-semiconductor interface on the free carrier mobility in an inversion region.

As a result, the Board is of the opinion that it would be obvious to the skilled person that reducing the roughness of the upper surface of the "surface channel layer" 5 in D4 would represent a solution to the above problem.

3.5 The claimed value of "less than about 1.0 Å" represents a very low, and hence desirable, value for the surface roughness. The Board finds nothing in the appellant's

submissions which would indicate that any particular technical effects occur in this range, other than the well-known beneficial effects which are associated with low surface roughness.

Whilst the upper surface of the surface channel layer in D4 would already be relatively smooth (having been deposited on a planarized substrate by epitaxy, as set out in paragraphs [0125] and [0130]), it is unlikely that a layer manufactured in this way would display the extremely low level of roughness claimed without further measures, and hence the skilled person would be motivated to further reduce the surface roughness to improve the carrier mobility.

3.6 Furthermore, the implementation of this solution would not require any inventive skill. On the contrary, according to the paragraph bridging pages 18 and 19 of the description, the invention may be carried out using the well known technique of chemical mechanical polishing (CMP), and "any conventional CMP process may be used as the CMP process discussed herein".

3.7 The appellant pointed out that the surface channel layer 5 in D4 has a thickness of "0.3 µm or less" (paragraph [0130]), and argued that since "conventional CMP processes remove several microns of film during the CMP process to obtain the desired result" (page 19, lines 1-3), the skilled person would be unable to achieve the claimed result starting from D4.

However, what is stated in the description is that CMP processes *which remove several microns of film* are unsuitable for implementing the invention (page 19, lines 6-8), as they "would remove all of the implanted

region rendering the device non-functional", and that CMP processes performed for short periods (e.g. "from about half an hour to about an hour") may suitably be used to remove an appropriate amount of material (page 19, lines 9-16). As stated on page 12, lines 21-27, the thickness of material removed according to the invention may be "from about 1200 Å to about 1400 Å" (120 nm to 140 nm).

3.8 In the opinion of the Board, the fact that the thickness of material removed in a CMP process can range from a few hundred nanometres (or less) up to several microns (and can be regulated by, *inter alia*, the duration of the process) would be part of the common knowledge of the skilled person.

In practice, starting from D4, the skilled person would have in mind a final thickness for the surface channel layer (for example, 300 nm), and would be aware of the amount to be removed to achieve the desired surface roughness (which apparently may be of the order of 140 nm). It would therefore be obvious to the skilled person to deposit an appropriate layer of n^- silicon carbide to a thickness equal to the sum of these two values (approximately 440 nm in this example) and then reduce the thickness over a time period sufficient to remove 140 nm of material.

3.9 In summary, the distinguishing feature of claim 1 of the main request represents a solution to the posed problem which would be obvious to the skilled person on the basis of common general knowledge, and which could be implemented without difficulty using conventional means. The Board therefore judges that the subject-matter of claim 1 of the main request does not involve

an inventive step within the meaning of Article 52(1) EPC and Article 56 EPC 1973.

4. *1st auxiliary request: Article 76(1) EPC 1973 and 123(2) EPC*

Compared to the main request, the 1st auxiliary request differs only in the modification referred to in section IV(ii), above, which is based on page 14, lines 2-7, and page 19, lines 20-23. The requirements of Article 123(2) EPC and 76(1) EPC 1973 are therefore met.

5. *1st auxiliary request: Inventive step in relation to D4*

5.1 Claim 1 of the 1st auxiliary request comprises the following additional feature:

"the n^- silicon carbide region (19') being not present on the n^+ conductivity silicon carbide region".

The term "not present on" can only be taken to mean that the n^- silicon carbide region 19' does not touch any part of the surface of the n^+ conductivity silicon carbide region, and hence these regions are not directly electrically connected.

5.2 As explained above for the main request, the claimed n^- silicon carbide region 19' may be identified with the n^- type surface channel layer 5 of D4, and the claimed n^+ conductivity silicon carbide region may be identified with the n^+ type source region 4 of D4.

5.3 In the silicon carbide vertical power MOSFET disclosed in D4, the n^- layer 5 ("surface channel layer") forms the channel. As explained in relation to the embodiment of Fig. 1 (see paragraphs [0077]-[0080] and [0088]-

[0091]), the thickness of the surface channel layer 5 is such that, in the OFF state, the ends of the surface channel layer adjacent the p-type base region 3 are entirely depleted due to the built-in voltage of the PN junction formed by the surface channel layer 5 and the p-type base region 3 (also taking into account the work function of the gate electrode 8). Current from the source to the drain region is therefore blocked.

When a positive bias is applied to the gate electrode 8, the device switches to its ON state, and current flows from the n^+ type source region 4 via the surface channel layer 5 to the n^+ type drain region 1 (see paragraph [0090]).

5.4 Hence, according to the operational principle on which the devices disclosed in D4 are based, it is absolutely indispensable that the n^+ type source region 4 should be in electrical connection with the n^- type surface channel layer 5, as shown, for example, in Fig. 7.

Such an electrical connection is explicitly excluded by the additional feature of claim 1 of the 1st auxiliary request. Hence, starting from the device of Fig. 7 of D4, the skilled person would never consider incorporating such a feature, as it would render the device non-functional. For this reason, the Board cannot regard D4 as a promising starting point for discussing inventive step in relation to claim 1 of the 1st auxiliary request.

6. *1st auxiliary request: Inventive step in relation to D8*

6.1 Document D8, which was cited as prior art in the description, discloses examples of double diffused MOSFETs (DMOSFETs) which are somewhat similar to the

arrangement of Fig. 1 of the present application. In the opinion of the Board, the device depicted in Fig. 3G, and manufactured according to the steps depicted in Figs. 3A-3G, represents a suitable choice of closest prior art for the invention defined by claim 1 of the 1st auxiliary request.

In Fig. 3G, the regions 150a, 150b at the surface of the p-type implants 136a, 136b form "a pair of channel regions" (column 9, lines 17-20; in fact these regions are the physical channels). In the terminology of claim 1 of the 1st auxiliary request, regions 150a, 150b represent (or at least form part of) the "first portion of the channel region".

6.2 The subject-matter of claim 1 differs from the closest prior art in that:

(a) the channel region comprises a second portion comprising an n^- silicon carbide region on the first portion of the channel region; and

(b) the channel region (29) of the power device has a root mean square (RMS) surface roughness of less than 0.1 nm (1.0 Å).

In D8, the gate insulating region 148 is formed directly on the channel regions 150a, 150b, and no surface roughness values are cited.

6.3 As with the main request, the problem solved by these differences is to improve the device performance, in particular the on-resistance.

6.4 For the reasons given above in connection with the main request, the Board considers that the skilled person,

starting from D8, would find it obvious to reduce the roughness of the upper surface of the channel 150a, 150b to solve the problem.

However, this would correspond to reducing the roughness of the claimed "first portion of the channel region", whereas the solution according to the present invention is to ensure that the channel region as a whole, including a second portion lying on the first portion of the channel region, has an RMS surface roughness less than 0.1 nm. The claimed solution therefore differs from that which would routinely occur to the skilled person.

6.5 The Board can accept that, as suggested by the appellant, forming an n^- region on the physical channel (regions 150a, 150b in D4), and ensuring that this n^- region has a very low surface roughness, represents a solution to the posed problem which offers advantages compared to the alternative of simply providing a low surface roughness channel. The deposited n^- region may be provided solely to be reduced in thickness to thereby improve the surface smoothness of the channel region. Accordingly, it can be deposited by any convenient method to a thickness which may be optimised to allow removal of a desired amount of material to achieve a target value for the surface roughness. The channel *per se* can be formed without being subject to any constraints imposed by surface roughness requirements.

6.6 Hence, the Board judges that the subject-matter of claim 1 of the 1st auxiliary request involves an inventive step within the meaning of Article 52(1) EPC and Article 56 EPC 1973.

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the department of first instance with the order to grant a patent in the following version:

   - Claims 1-10 of the New 1st Auxiliary Request filed during oral proceedings;

   - Description: pages 1-5 and 9-21 as filed during oral proceedings;

   - Figures: sheets 1-10 as filed with letter dated 28 March 2011.

The Registrar: The Chairman:

S. Sánchez Chiquero G. Eliasson

Decision electronically authenticated