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# Datasheet for the decision of 7 November 2018

**Case Number:** T 1228/14 - 3.5.05

**Application Number:** 11181181.6

**Publication Number:** 2458494

**IPC:** G06F3/06, G06F12/02

**Language of the proceedings:** EN

**Title of invention:**
Electronic devices with improved flash memory compatibility and methods corresponding thereto

**Applicant:**
HTC Corporation

**Headword:**
Virtual memory pages in a NAND memory/HTC

**Relevant legal provisions:**
EPC Art. 56

**Keyword:**
Inventive step - (no)

**Decisions cited:**

**Catchword:**

Europäisches Patentamt
European Patent Office
Office européen des brevets

**Beschwerdekammern**

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**Case Number: T 1228/14 - 3.5.05**

# D E C I S I O N
# of Technical Board of Appeal 3.5.05
# of 7 November 2018

| | |
|---|---|
| **Appellant:** (Applicant) | HTC Corporation<br>No. 23, Xinghua Road<br>Taoyuan District<br>Taoyuan City 330 (TW) |
| **Representative:** | 2K Patentanwälte Blasberg Kewitz & Reichel<br>Partnerschaft mbB<br>Schumannstrasse 27<br>60325 Frankfurt am Main (DE) |
| **Decision under appeal:** | **Decision of the Examining Division of the European Patent Office posted on 24 January 2014 refusing European patent application No. 11181181.6 pursuant to Article 97(2) EPC.** |

**Composition of the Board:**

| | |
|---|---|
| **Chair** | A. Ritzka |
| **Members:** | P. Cretaine |
| | F. Blumer |

## Summary of Facts and Submissions

I. This appeal is against the decision of the examining division, posted on 24 January 2014, refusing European patent application No. 11181181.6 on the grounds of lack of inventive step (Article 56 EPC) having regard to the disclosure of:

**D1**: US 2009/287956.

Further documents have been used in examination, in particular:

**D2**: US 2005/231515 and

**D6**: US 2008/195810.

II. Notice of appeal and a statement setting out the grounds of appeal were received on 12 March 2014 and the appeal fee was paid on 14 March 2014. The appellant requested that the decision under appeal be set aside and that a patent be granted based on the claims of the main request on which the decision was based, or on the claims of the first and second auxiliary requests filed with the statement setting out the grounds of appeal. Alternatively, oral proceedings by videoconference were requested.

III. A summons to oral proceedings was issued on 1 August 2018. In an annex to this summons, the board gave its preliminary opinion, which was that it considered **D2**, rather than **D1**, as the closest prior art, that the independent claims of the main request and of the first auxiliary request did not involve an inventive step (Article 56 EPC) having regard to the disclosure of **D2**, and that the independent claims of

the second auxiliary request did not involve an inventive step (Article 56 EPC) having regard to the disclosure of **D2** in combination with **D6**. The board further pointed out that as, according to the established case law (see e.g. T 1266/07, T 1930/12, or T 2313/12), it was not foreseen to hold oral proceedings before the boards of appeal by video conferencing, the appellant's request in that respect could not be granted.

IV. By letter of reply dated 22 October 2018, the appellant informed the board that it would not attend the scheduled oral proceedings.

V. Oral proceedings were held on 7 November 2018 in the absence of the appellant. The appellant requested in writing that the decision under appeal be set aside and that a patent be granted on the basis of the main request as filed by letter dated 17 September 2013 (main request on which the decision under appeal is based), or, in the alternative, on the basis of the first or second auxiliary request, both filed with the statement setting out the grounds of appeal dated 12 March 2014. After due deliberation on the basis of the written submissions, the board announced its decision at the end of the oral proceedings.

VI. Independent claim 1 according to the main request reads as follows:

"An electronic device (100) with improved flash memory compatibility, comprising:
a NAND flash (102), including a plurality of physical blocks, wherein each of the physical blocks (B1,B2 ...Bn) is further divided into a plurality of physical pages;

a processing unit (104); and
a program memory (106), storing application software (110) and codes of an operating system (112), wherein:
the application software executed by the processing unit requests for NAND flash access in accordance with a specific page size; and
the operating system run by the processing unit acts as an intermediary between the application software and the NAND flash and provides a device driver (208) which allocates a number of the physical pages of the NAND flash to each virtual page of the specific page size for responding to NAND flash access requests from the application software by referring to these virtual pages;
characterised in that the device driver (208) provided by the operating system and run by the processing unit further transforms one virtual page read/write instruction requested by the application software into same type of separate physical page read/write instructions to separately read/write the physical pages allocated to form the virtual page that the virtual page read/write instruction wants to access."

Independent claim 1 of the first auxiliary request adds to claim 1 of the main request, after the wording "An electronic device with improved flash memory compatibility", the wording "to be compatible with NAND flash of different page size".

Independent claim 1 of the second auxiliary request reads as follows:

"An electronic device (100) with improved flash memory compatibility to be compatible with NAND flash of different page size, comprising:

a NAND flash (102), including a plurality of physical blocks, wherein each of the physical blocks (B1,B2 ...Bn) is further divided into a plurality of physical pages;
a processing unit (104); and
a program memory (106), storing application software (110) and codes of an operating system (112), wherein:
the application software executed by the processing unit requests for NAND flash access in accordance with a specific page size; and
the operating system run by the processing unit acts as an intermediary between the application software and the NAND flash and provides a device driver (208) which allocates a number of the physical pages of the NAND flash to each virtual page of the specific page size for responding to NAND flash access requests from the application software by referring to these virtual pages;
wherein in that the device driver (208) provided by the operating system and run by the processing unit further transforms one virtual page read/write instruction requested by the application software into same type of separate physical page read/write instructions to separately read/write the physical pages allocated to form the virtual page that the virtual page read/write instruction wants to access;
wherein the device driver (208) provided by the operating system and run by the processing unit further allocates a number of physical blocks of the NAND flash as one virtual block accessible to the application software,
wherein the device driver (208) provided by the operating system and run by the processing unit further transforms one virtual block Erase or Get Status or Set Status instruction into same type of separate physical block Erase or Get Status or Set Status instructions to

separately Erase or Get Status or Status the physical blocks that are allocated to form the virtual block that the virtual block Erase or Get Status or Set Status instruction wants to access."

Each request contains a further independent claim (claim 9 of the main and first auxiliary request; claim 5 of the second auxiliary request) directed to a corresponding method.

## Reasons for the Decision

1. Admissibility of the appeal

The appeal complies with Articles 106 to 108 EPC (see point II above) and is therefore admissible.

2. Non-attendance at the oral proceedings

The appellant decided not to attend the oral proceedings scheduled. Pursuant to Article 15(3) RPBA, the board is not obliged to delay any step in the appeal proceedings, including its decision, by reason only of the absence at the oral proceedings of any party duly summoned who may then be treated as relying only on its written case.

Hence, the board was in a position to announce a decision at the end of the oral proceedings.

3. Prior art

**D1** discloses a storage device comprising banks of storage elements, e.g. NAND flash memories (see paragraph [0091], Figures 2 and 4A). Each storage

element is partitioned into physical erase blocks, and each erase block is partitioned into pages (see paragraph [0079]). A group of pages in a bank of storage elements may be grouped into a logical or virtual page. Similarly, erase blocks in a bank of storage elements may be grouped to form a logical or virtual erase block (see paragraph [0080] and Figure 4A). **D1** further discloses that an entire logical page is accessed with a read command but that the read command may be broken into subcommands (see paragraph [0082]).

**D2** discloses a data processing system with a memory, such as a flash memory card, organised into pages having a first size (see paragraphs [0007] and [0048]). While the memory is accessed based on these first-sized real pages, the operating system operates on larger, second-sized virtual memory pages (see the abstract and paragraph [0060]). Application programs executed by the system access the memory through the operating system, and thus based on the operating system virtual pages (see paragraph [0062]. A driver in the operating system creates and maintains a mapping between the virtual pages, on which the operating system and the application operates, and the real, i.e. physical, pages of the memory (see paragraphs [0057], [0060], and [0063] to [0067]).

**D6** discloses a NAND flash array organised into physical pages and physical blocks (see paragraphs [0006] and [0007]). A write command sends data in the form of logical pages grouped into logical blocks, which are transformed into physical pages and physical blocks by the memory control module (see paragraph [0022]).

4. Main request

4.1 The board agrees with the appellant that a logical, or virtual, page in **D1** is not equivalent to a virtual page within the meaning of claim 1. In that respect, **D1** discloses that a logical, or virtual, page, is related to a partitioning of the memory that is performed independently of the requirements of the operating system or of the application software running on it. In contrast, a virtual page in claim 1 has a size specific to the application software.

Therefore, the board holds that **D2**, rather than **D1** as stated in the decision, represents the closest prior art to the subject-matter of claim 1.

4.2 The physical pages in claim 1 can be seen in the physical pages of **D2**. The virtual pages of a size specific to the memory access requests of the application software in claim 1 can be seen in the virtual pages of **D2**.

Thus, the differences between the subject-matter of claim 1 and the disclosure of **D2** are that:

a) the flash memory is a NAND flash, with physical pages grouped in physical blocks, and

b) the device driver provided by the operating system transforms one virtual page read/write instruction requested by the application software into same type of separate physical page read/write instructions to separately read/write the physical pages allocated to form the virtual page that the virtual page read/write instructions want to access.

Distinguishing features a) and b) are clearly juxtaposed in the claims in that their combination in claim 1 does not provide a technical effect going beyond the mere addition of their respective technical effects. Their potential contributions in respect of inventive step can thus be analysed separately.

NAND flash memories having physical pages grouped in physical blocks, as per feature a), are well known in the art (see **D6** for instance). Using these kinds of memories in the storage device of **D2** represents an obvious choice for the skilled person, with no inventive merit in itself.

Feature b) merely makes it clear that read/write instruction of a virtual page formed by several physical pages is implemented by separately reading/ writing each physical page. The board agrees with the decision under appeal (see Reasons 1.1.3) in that such a separation of the read/write process in individual read/write processes is an obvious (see for instance breaking a read command into sub-commands in **D1**, paragraph [0082]) and straightforward way to ensure access to the physical pages mapped by the virtual page.

For these reasons the board judges that the subject-matter of claim 1 does not involve an inventive step, having regard to the disclosure of **D2** and the common general knowledge of the skilled person (Article 56 EPC).

5. First auxiliary request

Claim 1 adds to claim 1 of the main request the feature that the device is compatible with NAND flash memories of different page sizes.

The device disclosed in **D2** is not restricted to using a flash memory having a particular physical page size but rather to a flash memory having physical pages of a first size, smaller than the page size of the access request from the operating system. Therefore, the above-mentioned feature is already known from **D2**.

Thus, the board judges that the subject-matter of claim 1 does not involve an inventive step (Article 56 EPC) having regard to the disclosure of **D2**.

6. Second auxiliary request

Claim 1 adds to claim 1 of the first auxiliary request the features that:

a) a number of physical blocks of the NAND flash are grouped as a virtual block accessible to the application software, and

b) the device driver transforms one virtual block Erase or Get Status or Set Status instruction into the same type of separate physical block Erase or Get Status or Set Status_instructions to separately Erase or Get Status or Status the physical blocks that are allocated to form the virtual block.

Feature a) is known from **D6** (see paragraph [0010]).

Feature b), like feature b) in claim 1 of the main request (see point 4.2 above), merely makes it clear that an operation on a virtual block formed by several

physical blocks is implemented by separately operating on each physical block. The board agrees with the decision under appeal (see Reasons 1.1.3) that such a separation of a process in individual processes is an obvious (see, for instance breaking a read command into sub-commands in **D1**, paragraph [0082]) and straightforward way to ensure access to the physical blocks mapped by a virtual block.

Thus, the board judges that the subject-matter of claim 1 does not involve an inventive step, having regard to the disclosure of **D2** in combination with **D6** (Article 56 EPC).

7. The board further notes that, in its statement setting out the grounds of appeal, the appellant did not provide any argument in respect of the objections raised by the board, and no arguments in respect of the first and second auxiliary requests

8. Conclusion

The main request and the first and second auxiliary requests are not allowable for lack of inventive step (Article 56 EPC).

**Order**

**For these reasons it is decided that:**

The appeal is dismissed.

The Registrar: The Chair:

K. Götz-Wein A. Ritzka

Decision electronically authenticated