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Datasheet for the decision of 9 July 2019

Case Number: T 1205/14 - 3.4.03

Application Number: 08170802.6

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Language of the proceedings: EN

Title of invention:
Trench-gate MOSFET

Applicant:
Cree, Inc.

Headword:

Relevant legal provisions:
EPC Art. 56
EPC R. 115(2)
RPBA Art. 15(3)

Keyword:
Inventive step - (no)

Decisions cited:

Catchword:

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Case Number: T 1205/14 - 3.4.03

D E C I S I O N
of Technical Board of Appeal 3.4.03
of 9 July 2019

Appellant: (Applicant)	Cree, Inc. 4600 Silicon Drive Durham, NC 27703 (US)
Representative:	FRKelly 27 Clyde Road Dublin D04 F838 (IE)
Decision under appeal:	**Decision of the Examining Division of the European Patent Office posted on 27 November 2013 refusing European patent application No. 08170802.6 pursuant to Article 97(2) EPC.**

Composition of the Board:

Chairman	G. Eliasson
Members:	T. M. Häusser
	C. Heath

Summary of Facts and Submissions

I. The appeal concerns the decision of the examining division refusing the European patent application No. 08 170 802 for added subject-matter (Article 123(2) EPC) in relation to the main request then on file. The examining division did not admit former first and second auxiliary requests into the proceedings (Rule 137(3) EPC).

II. Reference is made to the following document:

D1: US-A-6 057 558.

III. In a telephone conversation with the chairman of the board dated 8 July 2019, the appellant's (applicant's) representative had enquired about the board's preliminary opinion, whereupon the chairman had replied that the preliminary opinion of the board tended to be negative, yet that all relevant issues could be discussed during the oral hearing.

Oral proceedings took place on 9 July 2019 before the board in the absence of the appellant, of which the board had been informed beforehand.

In writing the appellant had requested that the decision under appeal be set aside and a patent be granted based on the set of claims filed with letter dated 30 May 2019.

IV. The wording of independent claim 1 is as follows:

"1. A silicon carbide transistor (50) having an insulated control contact (61) within a trench (56) in a silicon carbide structure, the transistor comprising:

a pair of semiconductor mesas (65) each having a top surface and defining the trench, said semiconductor mesas each comprising at least one p-n junction;

a buried channel layer (72) extending across portions of top surfaces of said semiconductor mesas and at least partially covering walls of the trench such that said buried channel layer provides a conductive path across a $11\bar{2}0$ plane of the silicon carbide structure;

an n^+ type current spreading layer (55) extending beneath the trench to reduce junction field effect resistance in the transistor; and

a p^+ type doped well (77) extending from a top surface of at least one of said semiconductor mesas to a depth within said current spreading layer that is greater than a depth of the trench within said silicon carbide structure, wherein one of said at least one p-n junctions within said mesas comprises:

a p^+ type semiconductor epitaxial layer positioned in at least one of the pair of semiconductor mesas and under the buried channel layer and between the trench and said doped well;

an n^+ type source region in at least one of the pair of semiconductor mesas and on said p^+ type semiconductor epitaxial layer between the trench and said doped well; and

an n^+ type epitaxial buffer layer (73) positioned in at least one of the pair of semiconductor mesas and extending from said doped well to the trench, wherein said p^+ type semiconductor epitaxial layer, said n^+ type epitaxial buffer layer, and said p^+ type doped well are sufficiently doped to protect a trench corner (80) in an off state."

V. The appellant argued essentially as follows in relation to inventive step:

The cited state of the art documents, in particular document D1, did not disclose a doped well extending from a top surface of the mesa to a depth that exceeds the depth of the trench. Moreover, the examining division had equated the n-type epitaxial layer 2 in the device of D1 with several claimed layers, i. e. the "current spreading layer" and the "buffer layer".

Reasons for the Decision

1. Procedural matters

As announced in its letter dated 7 July 2019 the appellant did not attend the oral proceedings before the board.

In accordance with Rule 115(2) EPC and Article 15(3) RPBA, the oral proceedings were held without the appellant. By its decision not to attend the oral proceedings, the appellant has chosen not to make any further submissions during such proceedings and is treated as relying only on its written case.

2. Inventive step

2.1 Closest state of the art

The appellant regarded document D1 as the most pertinent document of the state of the art. Indeed, document D1 discloses - as detailed below - subject-matter that is conceived for the same purpose as the claimed invention, namely for providing a silicon carbide transistor having an insulated control contact within a trench in a silicon carbide structure, and has the most relevant

technical features in common with it. This document is therefore considered the closest state of the art.

2.2 Distinguishing features

2.2.1 Document D1 discloses (see column 1, lines 16-21; column 9, line 41 - column 10, line 46; column 13, lines 38-47; column 21, lines 14-63; Figures 1 and 37) silicon carbide semiconductor devices, in particular vertical type trench gate power MOSFETs with an n^--type epitaxial layer 2, a p-type epitaxial layer 3, an n^+-type source region 5, and a trench 7 formed in a predetermined region of the n^+-type source region 5. The trench 7 has a side face 7a perpendicular to the surface of the semiconductor substrate 4 and a bottom face 7b parallel with the surface of the semiconductor substrate 4. An n-type thin film semiconductor layer 8 extends over the surfaces of the n^+-type source region 5, the p-type epitaxial layer 3 and the n^--type epitaxial layer 2 at the side face 7a of the trench 7. A gate oxide film 9 is formed on the surface of the n-type thin film layer 8 and the bottom face 7b of the trench 7. The inside of the gate oxide film 9 in the trench 7 is filled with a gate electrode layer 10.

The surface orientation of the surface of the thin film semiconductor layer 8 formed on this side face 7a is an approximate $\{11\bar{2}0\}$ face. Since the channel is formed in the thin film layer 8, the channel-forming region surface is an approximate $\{11\bar{2}0\}$ face.

The particular device shown in Figure 37 of document D1 comprises a structure wherein a p-type embedded silicon carbide layer 14 away from the trench 7 and in contact with the p-type epitaxial layer 3 is formed in the n^--type epitaxial layer 2. With this construction, at the

bottom of the junction between the p-type embedded layer 14 and the n^--type epitaxial layer 2, a corner 14a of a sharp curvature is formed. As a result, the electric field strength at the corner 14a is made higher than the maximum electric field strength at the section B-B in Figure 37 and avalanche breakdown is made to occur in the pn^--diode formed by the p-type embedded layer 14 and the n^--type epitaxial layer 2, so that destruction of the gate oxide film 9 is prevented.

If the p-type embedded layer 14 is formed deeper than the trench 7, a depletion layer extending from the p-type embedded layer 14 under a reverse bias can cover the trench bottom and can moderate the electric field strength of the trench bottom. As a result, it is possible to raise the reliability of the gate oxide film 9 still further.

2.2.2 The appellant argued that document D1 did not disclose a doped well extending from a top surface of the mesa to a depth that exceeds the depth of the trench and that the n-type epitaxial layer 2 in the device of D1 could not be identified with two claimed layers, i. e. the "current spreading layer" and the "buffer layer".

In the decision under appeal the examining division pointed out under the heading "Further comments" that the current spreading layer and the buffer layer of the transistor according to the invention were both formed by epitaxial growth and that claim 1 of the former main request covered also transistors in which the buffer layer and the drift layer were portions of one epitaxial layer (see the decision, "Further comments", penultimate paragraph of point 2).

The board agrees with the examining division in this respect. Indeed, not only the current spreading layer and the buffer layer, but also the n^+ type source region and the p^+ type semiconductor layer are described as being formed by epitaxial growth (see the description of the application, respective paragraph 1 of pages 8 and 14). In relation to the buffer layer and the p^+ type semiconductor layer it is even explicitly specified in present claim 1 that they are epitaxial layers. Furthermore, due to the geometry of the layer arrangement the p^+ type semiconductor layer can only be formed by epitaxial growth if the doped well is also formed in this way. Hence, all these layers are not separated by layer boundaries originating from different methods of fabrication and cannot be distinguished by reference to such boundaries. Rather, they merely refer to regions of the epitaxially grown semiconductor material having specific doping types and concentrations.

Therefore, the claimed expressions "n^+ type current spreading layer", "p^+ type doped well", "p^+ type semiconductor epitaxial layer", "n^+ type source region", and "n^+ type epitaxial buffer layer" have to be read within the above meaning.

Consequently, the combination of the part of the p-type epitaxial layer 3 of the transistor shown in Figure 37 of D1 which is beneath the surface region 4a (where the p-type layer 3 is in contact with the source electrode layer 12) and the p-type embedded layer 14 can be considered the claimed doped well.

Moreover - as pointed out by the the examining division - the top portion of the n^--type epitaxial layer 2 located between the p-type embedded layer 14 and the

thin film layer 8 can be considered the claimed buffer layer, whereas the lower part of the n^--type epitaxial layer 2 can be considered the claimed current spreading layer.

2.2.3 Hence, using the wording of claim 1 document D1 discloses a silicon carbide transistor having an insulated control contact (gate electrode layer 10) within a trench (7) in a silicon carbide structure, the transistor comprising:

a pair of semiconductor mesas (regions of the p-type epitaxial layer 3 and the n^+-type source region 5) each having a top surface and defining the trench (7), said semiconductor mesas each comprising at least one p-n junction (formed by the p-type epitaxial layer 3 and the n^+-type source region 5);

a buried channel layer (formed in the thin film semiconductor layer 8) extending across portions of top surfaces of said semiconductor mesas and at least partially covering walls of the trench (7) such that said buried channel layer provides a conductive path across a $11\bar{2}0$ plane of the silicon carbide structure (surface of the channel-forming region is an approximate $\{11\bar{2}0\}$ face);

an n^- type current spreading layer (lower part of n^--type epitaxial layer 2) extending beneath the trench (7) to reduce junction field effect resistance in the transistor; and

a p type doped well (part of p-type epitaxial layer 3 and p-type embedded silicon carbide layer 14) extending from a top surface (4a) of at least one of said semiconductor mesas to a depth within said current spreading layer (lower part of n^--type epitaxial layer 2) that is greater than a depth of the trench (7) within said silicon carbide structure (the p-type embedded layer 14 is described as being formed deeper than the

trench 7), wherein one of said at least one p-n junctions within said mesas comprises:

a p type semiconductor epitaxial layer (p-type epitaxial layer 3) positioned in at least one of the pair of semiconductor mesas and under the buried channel layer (formed in the thin film semiconductor layer 8) and between the trench (7) and the doped well (part of p-type epitaxial layer 3 and p-type embedded layer 14); and

an n^+ type source region (n^+-type source region 5) in at least one of the pair of semiconductor mesas and on said p type semiconductor epitaxial layer (p-type epitaxial layer 3) between the trench (7) and the doped well (part of p-type epitaxial layer 3 and p-type embedded layer 14);

the transistor further comprising:

an n^- type epitaxial buffer layer (top portion of n^--type epitaxial layer 2) positioned in at least one of the pair of semiconductor mesas and extending from said doped well (part of p-type epitaxial layer 3 and p-type embedded layer 14) to the trench (7), wherein said p type semiconductor epitaxial layer (p-type epitaxial layer 3), said n^- type epitaxial buffer layer (top portion of n^--type epitaxial layer 2), and said p type doped well (part of p-type epitaxial layer 3 and p-type embedded silicon carbide layer 14) are sufficiently doped to protect a trench corner in an off state (avalanche breakdown occurs first at the pn^- diode formed by the p-type embedded layer 14 and the n^--type epitaxial layer 2 thereby protecting the trench corner region).

2.2.4 The subject-matter of claim 1 differs from the transistor of document D1 in that the current spreading layer, the doped well, the semiconductor epitaxial

layer, and the epitaxial buffer layer are of n^+ type, p^+ type, p^+ type, and n^+ type, respectively (rather than n^- type, p type, p type, and n^- type, respectively, in the device of D1).

2.3 Objective technical problem

2.3.1 The board notes that the distinguishing features only concern the doping levels of the layers mentioned under point 2.2.4 above but not the doping type. Moreover - as described above - the claimed purpose of the layer arrangement and the doping levels, namely to protect the trench corner in an off state is already disclosed in document D1.

2.3.2 In the description of the application the following precise values of the doping levels of the various layers of the transistor according to the invention are disclosed by way of example (see the paragraph bridging pages 9 and 10):

- source region: $1*10^{20}cm^{-3}$,
- current spreading layer: $5*10^{15}cm^{-3}$,
- doped well: $1*10^{19}cm^{-3}$,
- semiconductor epitaxial layer: $5*10^{17}cm^{-3}$,
- epitaxial buffer layer: $1*10^{16}cm^{-3}$.

Hence, the doping levels of these layers cover a range of five orders of magnitude including doping levels which would conventionally not be considered high doping levels. On the other hand, all of these layers are claimed as having high doping levels indicated by the plus sign ("n^+", "p^+"). Therefore, the claimed doping levels have to be understood as being merely a broad indication of the respective impurity concentrations.

2.3.3 In view of the above the board is of the opinion that it is the objective technical problem of the invention to provide an alternative silicon carbide transistor.

2.4 Obviousness

Adjusting the doping levels of the various layers of a semiconductor device belongs to the standard considerations of the skilled person working in the art of semiconductor device technology.

In order to provide an alternative transistor the skilled person would consider starting from the doping levels disclosed in relation to the simulation model shown in Figure 17 of document D1, namely a doping concentration of $2*10^{17}cm^{-3}$ for the p-type epitaxial layer 3 and the p-type embedded layer 14 and a doping concentration of $4.3*10^{15}cm^{-3}$ for the n^--type epitaxial layer 2. In the board's opinion, the skilled person would then adjust the doping concentrations of these layers without exercising inventive skills in such a manner as to arrive at the claimed subject-matter, especially since the claimed doping concentrations have to be understood in broad terms (see point 2.3.2 above) and are close to the starting concentrations mentioned above.

Consequently, the subject-matter of claim 1 does not involve an inventive step (Articles 52(1) and 56 EPC).

3. Conclusion

Since the claimed subject-matter does not involve an inventive step, the examining division's decision refusing the application is confirmed. Consequently the appeal has to be dismissed (Articles 97(2) and 111(1) EPC).

Order

For these reasons it is decided that:

The appeal is dismissed.

The Registrar: The Chairman:

S. Sánchez Chiquero G. Eliasson

Decision electronically authenticated