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Datasheet for the decision of 28 May 2019

Case Number: T 1054/14 - 3.4.03

Application Number: 06767745.0

Publication Number: 1908118

IPC: H01L29/78, H01L29/267, H01L21/04, H01L29/772, H01L29/24

Language of the proceedings: EN

Title of invention:
METHOD FOR PRODUCING SEMICONDUCTOR DEVICE

Applicant:
Nissan Motor Company Limited
ROHM CO., LTD.

Headword:

Relevant legal provisions:
EPC 1973 Art. 56
EPC Art. 52(1)

Keyword:
Inventive step - (yes)

This datasheet is not part of the Decision.
It can be changed at any time and without notice.

Decisions cited:

Catchword:

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It can be changed at any time and without notice.

Beschwerdekammern

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Case Number: T 1054/14 - 3.4.03

D E C I S I O N
of Technical Board of Appeal 3.4.03
of 28 May 2019

Appellant: (Applicant 1)
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Decision under appeal:
Decision of the Examining Division of the European Patent Office posted on 17 December 2013 refusing European patent application No. 06767745.0 pursuant to Article 97(2) EPC.

Composition of the Board:

Chairman G. Eliasson
Members: S. Ward
W. Van der Eijk

Summary of Facts and Submissions

I. The appeal is against the decision of the Examining Division refusing European patent application No. 06 767 745 on the grounds that the claimed subject-matter did not involve an inventive step within the meaning of Article 56 EPC.

II. At the end of the oral proceedings held before the Board the appellant confirmed its request that the decision under appeal be set aside and that a patent be granted on the basis of auxiliary request 3, filed with letter of 22 May 2019. This request is based on the following documents:

Claims:
claims 1-3 of auxiliary request 3, filed with letter of 22 May 2019;

Description:
- page 1, as filed during oral proceedings before the Board;
- pages 2, 4, 5, 8, 9, as filed on 8 May 2009;
- pages 3, 6, 7, 10, as in the published application;

Drawings:
sheets 1/7-7/7, as in the published application.

III. The following documents are referred to:

D1: US 2004/0217358 A1

D2: AGARWAL A ET AL: "Large Area 4H-SiC Power MOSFETs", PROCEEDINGS OF THE 2001 INTERNATIONAL SYMPOSIUM ON POWER SEMICONDUCTOR DEVICES & ICS, OSAKA, JAPAN,

JUNE 4-7, 2001; IEEE, NEW YORK, NY, US, pages 183-186

D3: CHUNG G Y ET AL: "Effect of nitric oxide annealing on the interface trap densities near the band edges in the 4H polytype of silicon carbide", APPLIED PHYSICS LETTERS, AIP, AMERICAN INSTITUTE OF PHYSICS, MELVILLE, NY, US, vol. 76, no. 13, 27 March 2000, pages 1713-1715

IV. Claim 1 of the sole request reads as follows:

"A method for producing a semiconductor device (20) of a type in which carriers are passed between a drain electrode and a source electrode by means of a tunnel current which is controlled by a voltage applied to a gate electrode and which flows between the drain electrode and the source electrode via a drive point, the semiconductor device (2) including:

a semiconductor substrate (1, 2) made of at least one selected from the group consisting of silicon carbide, gallium nitride and diamond,

a semiconductor region (3) made of at least one selected from the group consisting of single crystal silicon, polycrystal silicon, amorphous silicon, germanium and gallium arsenide, said semiconductor region (3) being configured to contact a first main face (2A) of the semiconductor substrate (1, 2) and different from the semiconductor substrate (1, 2) in band gap,

the gate electrode (7) contacting, via a gate insulating film (6) made of silicon dioxide, a part of

a junction part (13) between the semiconductor region (3) and the semiconductor substrate (1, 2),

the source electrode (8) configured to connect with the semiconductor region (3), and

the drain electrode (9) configured to make an ohmic connection with the semiconductor substrate (1, 2),

the method comprising the following sequential operations:

forming the semiconductor region (3) on the first main face (2A) of the semiconductor substrate (1, 2);

etching a part of the semiconductor region (3); and

forming the gate insulating film (6) both on the semiconductor region (3) that is etched and the semiconductor substrate (1, 2) that is exposed after the etching,

characterized by

nitriding the gate insulating film (6), after having formed the gate insulating film (6), to improve electron mobility on a first interface (11), a second interface (12), and a third interface (13) in the vicinity of the drive point (10), wherein said first interface (11) is defined between the gate insulating film (6) and the semiconductor substrate (1, 2), said second interface (12) is defined between the gate insulating film (6) and the semiconductor region (3), and said third interface (13) is defined between the semiconductor substrate (1, 2) and the semiconductor region (3), and wherein the first interface (11), the

second interface (12), and the third interface (13) in combination define said drive point (10),

wherein the nitriding is a high temperature annealing in an atmosphere containing at least one selected from the group consisting of N20, NO and NOx."

Reasons for the Decision

1. The appeal is admissible.

2. *Article 123(2) EPC*

2.1 Claim 1 of the sole request (i.e. the third auxiliary request, filed with letter of 22 May 2019) is based on claims 1, 3 and 4 as originally filed plus features taken from page 6, lines 6-9 and 15-16; page 4, line 20 to page 5, line 24; page 4, lines 2-4; and Figs. 3 and 4. Claims 2 and 3 are based on claims 2 and 5 as originally filed. The description has been satisfactorily adapted to the amended claims. The requirements of Article 123(2) EPC are therefore met.

3. *Inventive Step*

3.1 The appellant accepts that the preamble of claim 1 is disclosed in D1. The characterising part, i.e. the step of nitriding the gate insulating film by performing high temperature annealing in an atmosphere containing nitrogen oxide, is not disclosed in D1.

The principal technical effect provided by this feature is stated to be low ON resistance (see e.g. page 1,

lines 17-19; page 9, lines 21-23), and thus the technical problem can be seen as reducing the ON resistance of the device.

The Examining Division argued that both D2 and D3 (these documents disclose broadly similar information, and were sometimes referred to collectively by the Examining Division as "D2/D3") disclose the essence of the characterising part (annealing the gate oxide layer in a nitrogen atmosphere), and concluded that starting from D1, the teaching of D2/D3 would lead the skilled person, in an obvious manner, to the claimed subject-matter. In order to assess this conclusion, the Board will first briefly review the contents of these documents.

3.2 The starting point in document D1 (paragraph [0006]) is a discussion of the known drawbacks of SiC MOSFETs, in particular the high ON-state resistance due to imperfections in the channel region which act as electron traps and limit the carrier mobility in the channel. D1 therefore proposes discarding the MOSFET architecture completely and replacing it with a design based on a hetero-junction. For example, the embodiment of Fig. 1 comprises an N^+ type SiC substrate 10, an N^- SiC epitaxial region 20, an N^- type polycrystalline layer 60, a gate electrode 40 and a gate insulator (oxide) layer 30, whereby the "polycrystalline silicon layer 60 forms a hetero junction with the epitaxial region 20" and an "energy barrier is generated at the junction interface by the junction electric field" (paragraph [0030]).

When "a positive voltage is applied to the gate electrode 40, an electric field acts on the hetero junction interface between the N^- type polycrystalline

silicon layer 60 and the SiC epitaxial region 20 so that the concentrated electric field makes the energy barrier formed at the hetero junction interface thinner. As a result ... a current flow starts by the tunneling phenomenon" (paragraph [0031]; see also paragraph [0045]). Methods for manufacturing such devices are also disclosed.

3.3 By contrast, D2 and D3 concern conventional MOSFET devices based on SiC with SiO_2 gate insulation layers. These documents also discuss the known drawback mentioned above:

"the development of SiC metal-oxide-semiconductor field effect transistors (MOSFETs) has been impeded by the low effective carrier mobility in the FET channel. The low mobilities are directly linked to interface defects that either trap or scatter carriers. For SiO2/SiC, such defects are present in much higher concentrations compared to the corresponding SiO2/Si interface" (D3, page 1713, left-hand column, lines 4-10).

3.4 Unlike D1, however, the MOSFET design is retained in D2/D3, and both documents propose a solution to the channel carrier mobility problem involving a step of annealing the device in a nitric oxide (NO) atmosphere. In D3 it is noted that "nitric oxide (NO) annealing has a net positive effect on interface traps ... The total density of interface defects is significantly reduced with the NO treatment, implying that the interface states that degrade mobility are amenable to passivation" (page 1713, right-hand column, first paragraph). A similar teaching is found in D2: "Recently, annealing of the gate oxide layer using nitric oxide (NO) was shown to be very effective in reducing the surface states near the conduction band in

4H-SiC (4), which resulted in higher effective channel mobility on lightly doped p-type epilayers (6)" (page 184, right-hand column, first paragraph).

3.5 Against this background the appellant argues that a skilled person looking to further reduce the ON resistance of the device of D1, which is based on a hetero-junction and a tunneling phenomenon, and does not possess a channel, would not look to the teachings of D2 and D3, in which the stated aim is to increase channel carrier mobility in a MOSFET. In the opinion of the Board, this argument has considerable merit and raises serious doubts about the plausibility of the combination of documents proposed by the Examining Division.

3.6 The Examining Division acknowledged (Grounds for the decision, point 2.6) "that the physical mechanisms responsible for the switching between ON and OFF states are different for MOSFETs like the device of D2 and hetero-junction tunnel transistors of the type disclosed in D1 and the present application". Nevertheless, it argued that despite this difference, the skilled person would be led to conclude that the measure proposed in D2/D3 would provide the same benefits if used in the device of D1, the argument being essentially as follows:

In D1 it is the gate electrode that switches the current on and off (see e.g. D1, paragraph [0045]), and since "the gate action on the tunnel barrier and the carriers is evidently highest at the interface between the semiconductor and the gate insulator, most of the current has to flow, when travelling from the source electrode down to the drain electrode, along the sidewalls of the gate trenches" (Grounds for the

decision, point 2.6). Since D2 and D3 disclose a means (annealing in a nitrogen atmosphere) for improving carrier mobility (and hence lowering the ON resistance) in the region directly adjacent to the gate oxide layer, and since (it was argued) the current in D1 would flow mainly in this region, the skilled person would adapt the solution disclosed in D2 and D3 to the device of D1, and thereby be led to the claimed subject-matter.

3.7 The starting points for the Examining Division's argument are "Figs. 1, 8-10, 12 and associated text" (Grounds, point 2.1). Looking first at the embodiment of Fig. 1, the source-drain current flows essentially vertically throughout the device. The Examining Division appears to argue that, starting at the source electrode S, the current would flow through layer 60 very close to the sidewall of the gate oxide 30, finally tunnelling through the hetero-junction and passing through the SiC layers 20 and 10 on the way to drain electrode D.

3.8 However, even if this were true, it would mean that it is only the current in the polysilicon layer 60 which flows close to the interface with the gate oxide layer. D2 and D3, however, address the problem of interface defects at SiO_2/SiC interfaces, not at SiO_2/polysilicon interfaces. Even if there were a defect problem at SiO_2 /Si interfaces (and it is doubtful that this is the case - see point 3.3, above), a solution to such a problem is not disclosed in D2 or D3.

3.9 The embodiment of Fig. 8 appears, at first sight, a more promising starting point, in that there is at least a vertical SiC/gate oxide interface (between the N^- SiC layer 20 and the gate oxide 30). However, the

argument of the Examining Division that the source-drain current would follow a path which hugs this sidewall goes beyond what is explicitly disclosed in D1, which is silent on the precise path taken by the ON current.

A minimum requirement for this argument to succeed is that it would have to be implicit to the skilled person that the current in the N^- SiC region 20 of the embodiment of Fig. 8 would flow vertically downwards along, and very close to, the gate oxide interface, in a similar manner to the current flowing in the channel of a MOSFET. For the reasons given in the following, the Board does not believe that this has been plausibly demonstrated in the contested decision.

3.10 The device of Fig. 8 includes a hetero-junction formed between the polycrystalline silicon layer 50 and the epitaxial SiC region 20. In the ON state "where a positive voltage is applied to the gate electrode 40, an electric field acts on the hetero junction interface between the N^+ type polycrystalline silicon layer 50 and the SiC epitaxial region 20 so that the concentrated electric field makes the energy barrier formed at the hetero junction interface thinner" and hence current flows by the tunneling phenomenon (paragraph [0103]).

The point at which this hetero-junction meets the gate oxide corresponds to the claimed "drive point", and the electric field produced by an applied gate voltage would presumably be most effective at reducing the hetero-junction energy barrier in the region close to the drive-point. As a result, the current density at the plane of the hetero-junction might be expected to be higher close to the drive point than in the central

region. Conceivably, it might even be accurate to describe the current as flowing along the gate oxide interface "in the vicinity of the drive point" (as in the description of the present application, page 6, lines 9-12). However, above and below the hetero-junction, the Board sees no reason to expect that the current would flow "along the sidewalls" of the gate oxide as suggested by the Examining Division, and therefore no reason for the skilled person to look to documents D2 or D3, or to conclude that the solution proposed therein (reducing defects in a MOSFET channel region by annealing in a nitrogen atmosphere) would be effective in the device of D1.

3.11 Of the other proposed starting points (Figs. 9, 10 and 12), Fig. 9 shows an arrangement very similar to that of Fig. 8, Fig. 10 shows a production process for the device of Fig. 1, and Fig. 12 shows a production process for the device of Fig. 8. Hence, starting from any of these drawings, the same conclusions would be reached on inventive step as when starting from Figs. 1 or 8.

3.12 On the basis of the available prior art, the Board is not persuaded that it would be obvious to the skilled person to arrive at the subject-matter of claim 1, which consequently is considered to involve an inventive step within the meaning of Article 52(1) EPC and Article 56 EPC 1973.

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the examining division with the order to grant a patent as follows:

   Claims:
   claims 1-3 of auxiliary request 3, filed with letter of 22 May 2019;

   Description:
   - page 1, as filed during oral proceedings before the Board;
   - pages 2, 4, 5, 8, 9, as filed on 8 May 2009;
   - pages 3, 6, 7, 10, as in the published application;

   Drawings:
   sheets 1/7-7/7, as in the published application.

The Registrar: The Chairman:

S. Sánchez Chiquero G. Eliasson

Decision electronically authenticated