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Datasheet for the decision of 20 December 2017

Case Number: T 1009/14 - 3.5.04

Application Number: 03007266.4

Publication Number: 1351512

IPC: H04N7/50

Language of the proceedings: EN

Title of invention:
Video decoding system supporting multiple standards

Applicant:
Broadcom Corporation

Headword:

Relevant legal provisions:
EPC 1973 Art. 84
EPC Art. 123(2)

Keyword:
Claims - clarity (no) - main, first, second and fourth to ninth auxiliary requests
Amendments - added subject-matter (yes) - third auxiliary request

Decisions cited:

Catchword:

Europäisches Patentamt
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Beschwerdekammern

Boards of Appeal

Chambres de recours

Boards of Appeal of the
European Patent Office
Richard-Reitzner-Allee 8
85540 Haar
GERMANY
Tel. +49 (0)89 2399-0
Fax +49 (0)89 2399-4465

Case Number: T 1009/14 - 3.5.04

D E C I S I O N
of Technical Board of Appeal 3.5.04
of 20 December 2017

Appellant: (Applicant)	Broadcom Corporation 5300 California Avenue Irvine, CA 92617 (US)
Representative:	Jehle, Volker Armin Bosch Jehle Patentanwaltsgesellschaft mbH Flüggenstraße 13 80639 München (DE)
Decision under appeal:	**Decision of the Examining Division of the European Patent Office posted on 11 December 2013 refusing European patent application No. 03007266.4 pursuant to Article 97(2) EPC.**

Composition of the Board:

Chairman	C. Kunzelmann
Members:	M. Paci
	B. Müller

Summary of Facts and Submissions

I. The appeal is against the decision of the examining division refusing European patent application No. 03007266.4, published as EP 1 351 512 A2.

II. In the decision under appeal the following document *inter alia* was cited:

D2: Bose S. et al., "A Single Chip Multistandard Video Codec", Custom Integrated Circuits Conference, 1993, Proceedings of the IEEE 1993, San Diego, CA, USA, 9-12 May 1993, pages 11.4.1-11.4.4, XP010222103, ISBN: 0-7803-0826-3.

III. The decision under appeal was based on the grounds that claim 1, according to each of the then main and first to seventh auxiliary requests, did not meet the requirement of clarity of Article 84 EPC and that the subject-matter of claim 1 according to the then first auxiliary request did not involve an inventive step (Article 56 EPC) in view of prior-art document D2.

IV. With the statement of grounds of appeal, the appellant filed sets of amended claims according to a main request and first to sixth auxiliary requests replacing all the previous claims on file. It requested that the decision under appeal be set aside and that a patent be granted on the basis of the sets of claims filed with the statement of grounds of appeal. As a precaution, the appellant also requested oral proceedings.

V. In a letter dated 25 August 2017, the appellant requested accelerated processing of the appeal.

VI. The board sent a summons to oral proceedings dated 5 October 2017 and a communication dated 16 October 2017.

In its communication, the board informed the appellant that it had granted accelerated processing. The board explained why it was of the provisional view that the claims according to all requests on file did not meet the requirements of Articles 83 and 84 EPC 1973 and that the subject-matter of claim 1 according to those requests did not involve an inventive step in view of prior-art document D2 and common general knowledge, as well as in view of the prior art disclosed on page 3, lines 3 to 6, of the application as filed.

VII. With a letter dated 20 November 2017, the appellant filed two sets of amended claims according to new first and second auxiliary requests and renumbered the previous first to sixth auxiliary requests as third to eighth auxiliary requests.

VIII. The board held oral proceedings on 20 December 2017, during which the appellant filed a set of claims according to a new third auxiliary request, renumbered the previous third to eighth auxiliary requests as fourth to ninth auxiliary requests and filed an amended description page 30 for the third to ninth auxiliary requests.

The appellant's requests at the end of the oral proceedings were that the decision under appeal be set aside and a European patent be granted on the basis of the claims according to the main request filed with the statement of grounds of appeal, or the first and second auxiliary requests filed with the letter dated 20 November 2017, or the third auxiliary request filed

during the oral proceedings of 20 December 2017, or the fourth to ninth auxiliary requests, filed as first to sixth auxiliary requests with the statement of grounds of appeal, for the third to ninth auxiliary requests with an amended description page 30 filed during the oral proceedings of 20 December 2017.

At the end of the oral proceedings, the chairman announced the board's decision.

IX. Claim 1 according to the appellant's **main request** reads as follows:

"Video decoding system comprising:
a processor (302) adapted to control a decoding process; and
a plurality of hardware accelerators (306, 308, 309, 310, 312) coupled to the processor, each accelerator adapted to perform a decoding function on a video data stream,
wherein each of the accelerators are configurable to perform their associated decoding functions according to a plurality of decoding methods;
characterized in that
the plurality of hardware accelerators comprise:
a programmable entropy decoder (306) adapted to perform entropy decoding on the data stream;
an inverse quantizer (308) adapted to perform inverse quantization on the data stream;
an inverse transform accelerator (309) adapted to perform inverse transform operations on the data stream;
a pixel filter (310) adapted to perform pixel filtering on the data stream; and
a motion compensator (312) adapted to perform motion compensation on the data stream,

wherein the programmable entropy decoder (306) is a programmable variable length decoder, PVLD."

X. Claim 1 according to the appellant's **first auxiliary request** reads as follows (additions to claim 1 of the **main request** are underlined and deletions are ~~struck-through~~):

"Video decoding system comprising:
a processor (302) adapted to control a decoding process; and
a plurality of hardware ~~accelerators~~ blocks (306, 308, 309, 310, 312) coupled to the processor, each ~~accelerator~~ hardware block adapted to perform a decoding function on a video data stream,
wherein each of the ~~accelerators~~ hardware blocks are configurable to perform their associated decoding functions according to a plurality of decoding methods;
characterized in that
the plurality of hardware ~~accelerators~~ blocks comprise:
a programmable entropy decoder (306) adapted to perform entropy decoding on the data stream;
an inverse quantizer (308) adapted to perform inverse quantization on the data stream;
an inverse transform accelerator (309) adapted to perform inverse transform operations on the data stream;
a pixel filter (310) adapted to perform pixel filtering on the data stream; and
a motion compensator (312) adapted to perform motion compensation on the data stream,
wherein the programmable entropy decoder (306) is a programmable variable length decoder, PVLD."

XI. Claim 1 according to the appellant's **second auxiliary request** reads as follows (additions to claim 1 of the

main request are underlined and deletions are ~~struck-through~~):

"Video decoding system comprising:
a processor (302) adapted to control a decoding process; and
a plurality of hardware accelerators (306, 308, 309, 310, 312) coupled to the processor, each accelerator adapted to perform a decoding function on a video data stream,
wherein each of the accelerators are configurable to perform their associated decoding functions according to a plurality of decoding methods;
~~characterized in that~~
wherein the processor (302) is adapted to program registers in each of the accelerators to modify the operational behavior of the accelerator; and
wherein the plurality of hardware accelerators comprise:
a programmable entropy decoder (306) adapted to perform entropy decoding on the data stream;
an inverse quantizer (308) adapted to perform inverse quantization on the data stream;
an inverse transform accelerator (309) adapted to perform inverse transform operations on the data stream;
a pixel filter (310) adapted to perform pixel filtering on the data stream; and
a motion compensator (312) adapted to perform motion compensation on the data stream,
wherein the programmable entropy decoder (306) is a programmable variable length decoder, PVLD."

XII. Claim 1 according to the appellant's **third auxiliary request** reads as follows (additions to claim 1 of the **second auxiliary request** are underlined):

"Video decoding system comprising:
a processor (302) adapted to control a decoding process; and
a plurality of hardware accelerators (306, 308, 309, 310, 312) coupled to the processor, each accelerator adapted to perform a decoding function by hardware on a video data stream,
wherein each of the accelerators are configurable to perform their associated decoding functions according to a plurality of decoding methods;
wherein the processor (302) is adapted to program registers in each of the accelerators to modify the operational behavior of the accelerator; and
wherein the plurality of hardware accelerators comprise:
a programmable entropy decoder (306) adapted to perform entropy decoding on the data stream;
an inverse quantizer (308) adapted to perform inverse quantization on the data stream;
an inverse transform accelerator (309) adapted to perform inverse transform operations on the data stream;
a pixel filter (310) adapted to perform pixel filtering on the data stream; and
a motion compensator (312) adapted to perform motion compensation on the data stream,
wherein the programmable entropy decoder (306) is a programmable variable length decoder, PVLD."

XIII. Claim 1 according to the appellant's **fourth auxiliary request** reads as follows:

"Video decoding system comprising:
a processor (302) adapted to control a decoding process; and

a plurality of hardware accelerators (308, 309, 310, 312) coupled to the processor, each accelerator adapted to perform a decoding function on a video data stream, wherein each of the accelerators are configurable to perform their associated decoding functions according to a plurality of decoding methods;
characterized in that
the video decoding system further comprises a programmable variable-length decoder, PVLD, module (306) designed as a coprocessor to the processor (302); and
the plurality of hardware accelerators comprise:
an inverse quantizer (308) adapted to perform inverse quantization on the data stream;
an inverse transform accelerator (309) adapted to perform inverse transform operations on the data stream;
a pixel filter (310) adapted to perform pixel filtering on the data stream; and
a motion compensator (312) adapted to perform motion compensation on the data stream; and
the PVLD module (306) comprises:
a PVLD hardwired to perform decoding according to MPEG2 and
a PVLD engine comprising a code random access memory, RAM, to hold variable-length coding tables for media coding formats other than MPEG2."

XIV. Claim 1 according to the appellant's **fifth auxiliary request** reads as follows (additions to claim 1 of the **main request** are underlined, and deletions are ~~struck-through~~):

"Video decoding system comprising:
a processor (302) adapted to control a decoding process; and

a plurality of hardware accelerators (306, 308, 309, 310, 312) coupled to the processor, each accelerator adapted to perform a decoding function on a video data stream,
wherein each of the accelerators are configurable to perform their associated decoding functions according to a plurality of decoding methods;
~~characterized in that~~
wherein the processor (302) is adapted to configure each of the accelerators to perform the decoding function according to a format of the video data stream to be decoded;
wherein the plurality of hardware accelerators comprise:
a programmable entropy decoder (306) adapted to perform entropy decoding on the data stream;
an inverse quantizer (308) adapted to perform inverse quantization on the data stream;
an inverse transform accelerator (309) adapted to perform inverse transform operations on the data stream;
a pixel filter (310) adapted to perform pixel filtering on the data stream; and
a motion compensator (312) adapted to perform motion compensation on the data stream,
wherein the programmable entropy decoder (306) is a programmable variable length decoder, PVLD."

XV. Claim 1 according to the appellant's **sixth auxiliary request** reads as follows (additions to claim 1 of the **fifth auxiliary request** are underlined and deletions are ~~struck-through~~):

"Video decoding system comprising:
a processor (302) adapted to control a decoding process; and

a plurality of hardware accelerators (306, 308, 309, 310, 312) coupled to the processor, each accelerator adapted to perform a decoding function on a video data stream,
wherein each of the accelerators are configurable to perform their associated decoding functions according to a plurality of decoding methods;
wherein the processor (302) is adapted to configure each of the accelerators to perform the decoding function according to a format of the video data stream to be decoded~~;~~ through register read/write, wherein the processor (302) programs registers in each of the accelerators to modify the operational behavior of the module; and
wherein the plurality of hardware accelerators comprise:
a programmable entropy decoder (306) adapted to perform entropy decoding on the data stream;
an inverse quantizer (308) adapted to perform inverse quantization on the data stream;
an inverse transform accelerator (309) adapted to perform inverse transform operations on the data stream;
a pixel filter (310) adapted to perform pixel filtering on the data stream; and
a motion compensator (312) adapted to perform motion compensation on the data stream,
wherein the programmable entropy decoder (306) is a programmable variable length decoder, PVLD."

XVI. Claim 1 according to the appellant's **seventh auxiliary request** reads as follows (additions to claim 1 of the **fifth auxiliary request** are underlined):

"Video decoding system comprising:

a processor (302) adapted to control a decoding process; and
a plurality of hardware accelerators (306, 308, 309, 310, 312) coupled to the processor, each accelerator adapted to perform a decoding function on a video data stream,
wherein each of the accelerators are configurable to perform their associated decoding functions according to a plurality of decoding methods;
wherein the processor (302) is adapted to configure each of the accelerators to perform the decoding function according to a format of the video data stream to be decoded;
wherein each of the accelerators includes one of a set of registers or memory coupled to an internal processor, that dictates operational parameters of the accelerator and wherein the processor (302) programs the registers or the memory in order to configure the accelerator and wherein the processor (302) reads the registers or the memory in order to derive operational status of the accelerator; and
wherein the plurality of hardware accelerators comprise:
a programmable entropy decoder (306) adapted to perform entropy decoding on the data stream;
an inverse quantizer (308) adapted to perform inverse quantization on the data stream;
an inverse transform accelerator (309) adapted to perform inverse transform operations on the data stream;
a pixel filter (310) adapted to perform pixel filtering on the data stream; and
a motion compensator (312) adapted to perform motion compensation on the data stream,
wherein the programmable entropy decoder (306) is a programmable variable length decoder, PVLD."

XVII. Claim 1 according to the appellant's **eighth auxiliary request** reads as follows (additions to claim 1 of the **main request** are underlined and deletions are ~~struck-through~~):

"Video decoding system comprising:
a processor (302) adapted to control a decoding process; and
a plurality of hardware accelerators (306, 308, 309, 310, 312) coupled to the processor, each accelerator adapted to perform a decoding function on a video data stream,
wherein each of the accelerators are configurable to perform their associated decoding functions according to a plurality of decoding methods;
~~characterized in that~~
wherein the processor (302) is adapted to configure each of the accelerators to perform the decoding function according to a format of the video data stream to be decoded;
wherein the plurality of hardware accelerators comprise:
a programmable entropy decoder (306) adapted to perform entropy decoding on the data stream;
an inverse quantizer (308) adapted to perform inverse quantization on the data stream;
an inverse transform accelerator (309) adapted to perform inverse transform operations on the data stream;
a pixel filter (310) adapted to perform pixel filtering on the data stream; and
a motion compensator (312) adapted to perform motion compensation on the data stream~~,~~;
wherein the programmable entropy decoder (306) is a programmable variable length decoder, PVLD;

wherein actions of the plurality of hardware accelerators are arranged in an execution pipeline comprising a plurality of stages;
wherein the hardware accelerators operate concurrently with the processor (302) while decoding a series of macroblocks of the video data stream; and
wherein the processor (302) controls the execution pipeline, initiates decoding of each macroblock, and controls operation of each of the plurality of hardware accelerators."

XVIII. Claim 1 according to the appellant's **ninth auxiliary request** reads as follows (additions to claim 1 of the **main request** are underlined and deletions are ~~struck-through~~):

"Video decoding system comprising:
a processor (302) adapted to control a decoding process; and
a plurality of hardware accelerators (306, 308, 309, 310, 312) coupled to the processor, each accelerator adapted to perform a decoding function on a video data stream,
wherein each of the accelerators are configurable to perform their associated decoding functions according to a plurality of decoding methods;
~~characterized in that~~
wherein the processor (302) is adapted to configure each of the accelerators to perform the decoding function according to a format of the video data stream to be decoded;
wherein the plurality of hardware accelerators comprise:
a programmable entropy decoder (306) adapted to perform entropy decoding on the data stream;

an inverse quantizer (308) adapted to perform inverse quantization on the data stream;
an inverse transform accelerator (309) adapted to perform inverse transform operations on the data stream;
a pixel filter (310) adapted to perform pixel filtering on the data stream; and
a motion compensator (312) adapted to perform motion compensation on the data stream;
wherein the programmable entropy decoder (306) is a programmable variable length decoder, PVLD;
wherein actions of the plurality of hardware accelerators are arranged in an execution pipeline comprising a plurality of stages;
wherein the pipeline scheme supports one pipeline stage per hardware accelerator, wherein any hardware accelerator that depends on the result of another hardware accelerator is arranged in a following pipeline stage;
wherein the execution pipeline is optimized by hardware balancing each hardware accelerator in the execution pipeline according to the format of the data stream."

XIX. The examining division's reasons for the decision under appeal which are relevant to the present decision may be summarised as follows:

The examining division understood the term "hardware accelerator" to refer to dedicated hardware which performed a function (in this case a decoding function) faster than was possible in software executed on a general-purpose processor. As opposed to a general-purpose processor, which was fully programmable, a hardware accelerator was dedicated to a particular function, e.g. IDCT or Huffman coding.

However, claim 1 further defined that each of the hardware accelerators were "configurable to perform their associated decoding functions according to a plurality of decoding methods". According to the description, these "plurality of decoding methods" were various public and private video coding standards which had some decoding functions in common but also fundamental differences between them, in particular for entropy decoding. Claim 1 thus implied that the hardware accelerators, rather than being dedicated hardware, were fully programmable. This contradiction in terms and the resulting uncertainty as to what the "hardware accelerators" actually were, thus caused a lack of clarity in claim 1.

XX. The appellant's main arguments regarding the issues relevant to the present decision may be summarised as follows:

Arguments for the main and second to ninth auxiliary requests:

(a) Each of the "hardware accelerators" of claim 1 were adapted to perform a particular decoding function and were configurable to perform this particular decoding function according to a plurality of decoding methods. They thus each performed only a fixed decoding function, but in a flexible manner by being configurable to perform this function according to different decoding methods. The "hardware accelerators" were thus not "fully programmable" as alleged in the reasons for the decision because there was no software running on them, which excluded that they could be general-purpose processors (CPU) or digital signal processors (DSP).

(b) The term "hardware accelerator" had no well-defined meaning in the art. Thus, a hardware accelerator could be considered as a device that speeds up processing or transmission, in particular, to reduce the load of a (general-purpose) processor, which was in line with the use of "hardware accelerator" in the present application.

Arguments for the first auxiliary request:

By replacing the term "hardware accelerator" with the term "hardware block" in claim 1 of the first auxiliary request, it had been made clear that the "hardware block" could also run software. This was further supported by the sentence on page 30, lines 22 to 25, of the application as filed stating that "(i)n another illustrative embodiment, some or all of the hardware accelerators comprise programmable processors which are configured to operate according to different encoding/ decoding formats by changing the software executed by those processors, in addition to programming registers as appropriate to the design".

Additional arguments for the third to ninth auxiliary requests:

The deletion of the above sentence on page 30, lines 22 to 25, of the application as filed, made it unambiguously clear that the "hardware accelerators" did not run any software.

Reasons for the Decision

1. The appeal is admissible.

Main request - clarity (Article 84 EPC 1973)

2. The video decoding system of claim 1 comprises *inter alia* "a plurality of hardware accelerators [...], each accelerator adapted to perform a decoding function on a video data stream, wherein each of the accelerators are configurable to perform their associated decoding functions according to a plurality of decoding methods". Claim 1 further states that the plurality of hardware accelerators comprise a programmable variable length decoder, an inverse quantizer, an inverse transform accelerator, a pixel filter and a motion compensator.

3. In the reasons for the decision (under points 2.1.1 and 3.3), the examining division held that the meaning of "hardware accelerator" in claim 1 was unclear because of the following contradictions:
   (1) on the one hand, the term itself would be construed as referring to hardware dedicated to a particular function (in this case a decoding function) which was performed faster than possible in software executed on a general-purpose processor;
   (2) however, on the other hand, claim 1 also stated that each hardware accelerator was configurable to perform its associated decoding function according to a plurality of decoding methods, with said plurality of decoding methods comprising fundamentally different decoding methods according to the description. This

implied that the hardware accelerators had to be "fully programmable", i.e. that they may also include a programmable processor running software as mentioned on page 30, lines 22 to 25, of the description of the application.

4. The board concurs with the above reasons given by the examining division.

5. The appellant did not dispute that the term "hardware accelerator" had no well-defined meaning in the art (see letter of 20 November 2017, page 4, second paragraph). Instead, the appellant argued during the appeal proceedings that it was clear to the skilled person that a "hardware accelerator" was purely hardware, i.e. that it was not running software, and that the description of the application explained how each hardware accelerator could be configured by way of read/write registers to perform its dedicated decoding function according to a plurality of decoding methods.

6. These arguments did not persuade the board for the following reasons:

(a) In the application as filed, there is neither any definition of the term "hardware accelerator", nor any detailed example of its internal structure. However, on page 30, lines 22 to 25, it is stated that "(i)n another illustrative embodiment, some or all of the hardware accelerators comprise programmable processors which are configured to operate according to different encoding/decoding formats by changing the software executed by those processors, in addition to programming registers as appropriate to the design". Hence, at least this last sentence puts into question the validity of the appellant's assertion that there

was no inherent contradiction in claim 1 because it was clear to the person skilled in the art that a "hardware accelerator" did not run software.

(b) According to the description of the application, the plurality of decoding methods of claim 1 includes all existing and future video decoding standards, both public and private (see, for instance, from page 1, line 28, to page 2, line 8; from page 6, line 23, to page 7, line 10; and page 23, lines 22 to 25). When asked by the board how a given hardware accelerator dedicated to a particular decoding function could perform two or more widely different algorithms for this same function only by changing some operational parameters in some registers, i.e. **without running software**, the appellant explained that it could be done by having multiple instances of hardware in a hardware accelerator, each dedicated to a single algorithm, and by using a read/write register to select the right instance of hardware. The appellant referred in particular to page 18, line 24, to page 20, line 2, of the description which explains how to select either the loop filter 313 or the post filter 315 inside the filter module 314. However, this explanation did not persuade the board because the application as filed clearly states on page 3, lines 3 to 10, that providing multiple instances of hardware, each dedicated to a single algorithm, is an inefficient and expensive prior-art solution which does not form part of the present invention. As to the prior art mentioned on page 3, lines 3 to 6, the appellant argued (despite the sentence starting with "Yet others in the industry") that it was not describing publicly available prior-art, but non-public internal art known only to the inventor and that it should thus be ignored. In the board's view, it does not matter in the present case,

and thus can be left unanswered, whether the solution described on page 3, lines 3 to 6, is prior art under Article 54(2) EPC 1973, because what matters is that there is a clear disclosure in the application that the invention seeks to improve upon, not use, this solution, be it prior art or not.

(c) The mere fact that a "hardware accelerator" can be configured by writing operational parameters into registers does not exclude that the accelerator is also capable of running software.

7. For the above reasons, the board considers that the term "hardware accelerator" does not have a clear meaning in the context of claim 1. Hence, claim 1 according to the main request does not meet the requirement of clarity of Article 84 EPC 1973 and the appellant's main request is not allowable.

First auxiliary request - clarity (Article 84 EPC 1973)

8. Claim 1 according to the first auxiliary request differs from claim 1 according to the main request only in that the expression "hardware block" is used instead of "hardware accelerator" throughout the claim.

9. The appellant argued that "hardware block", contrary to "hardware accelerator", did not exclude that the block could also comprise a programmable processor running software, as mentioned on page 30, lines 22 to 25, of the application as filed.

10. The board notes that the expression "hardware block" (in singular or plural form) is used several times in the application as filed (namely on page 10, line 29, on page 12, lines 8 and 9, on page 14,

line 20, on page 22, line 28, on page 23, lines 1, 2 and 14, and on page 24, lines 20 and 24) to refer to the same items 306, 308, 309, 310, 312, 314 of figures 3 and 4a which are also referred to elsewhere in the application as "hardware accelerator". These two expressions in the context of the present application are synonyms referring to the same items. Neither of the terms "hardware accelerator" or "hardware block" are explicitly defined in the application, and there is no indication that the term "hardware block" could have a different meaning than the unclear term "hardware accelerator". The board thus considers that the appellant's argument that "hardware accelerator" would exclude software, while "hardware block" would not, is not supported by the disclosure of the application as filed. In fact, the board regards these two mutually exclusive interpretations of two terms which designate the same items as a further indication that the second term ("hardware block") also has no clear meaning in the context of claim 1 of the first auxiliary request, essentially for the same reasons as those given above with regard to the main request.

As to the sentence on page 30, lines 22 to 25, of the description, it does not help the appellant's case because it refers to "hardware accelerators", not "hardware blocks", and the appellant argued that these do not have the same meaning.

11. For the above reasons, the board considers that claim 1 according to the first auxiliary request does not meet the requirement of clarity of Article 84 EPC 1973. Hence the appellant's first auxiliary request is not allowable.

Second and fourth to ninth auxiliary requests - clarity (Article 84 EPC 1973)

12. Claim 1 according to each of the second and fourth to ninth auxiliary requests differs from claim 1 according to the main request by one or more additional features (see points XI and XIII to XVIII *supra*). In addition, for the fourth to ninth auxiliary requests, page 30 of the description has been amended by deleting the sentence in lines 22 to 25.

13. However, none of these additional features in claim 1 clarifies whether the "hardware accelerator" may or may not also run software. As to the deletion of the sentence on page 30, lines 22 to 25, of the description of the application in the fourth to ninth auxiliary requests, it removes the explicit contradiction with the appellant's interpretation of "hardware accelerator" that it does not run software. However, the thus modified description does not clarify either whether the "hardware accelerator" can also run software.

14. Hence, claim 1 according to each of the second and fourth to ninth auxiliary requests lacks clarity essentially for the same reasons as claim 1 according to the main request. Accordingly, these requests are not allowable.

Third auxiliary request - added subject-matter (Article 123(2) EPC)

15. Claim 1 according to the third auxiliary request differs from claim 1 according to the second auxiliary request by the insertion of "by hardware" immediately

after "each accelerator adapted to perform a decoding function".

16. The appellant argued that this amendment had a basis in the use of the word "hardwired" on page 9, lines 14 to 18, of the application as filed, which reads as follows:

"Also, in an illustrative embodiment, the PVLD module 306 includes two variable-length decoders. Each of the two programmable variable-length decoders can be hardwired to efficiently perform decoding according to a particular video compression standard, such as MPEG2 HD.".

17. The board notes that in the above sentence only the two variable-length decoders of the PVLD module 306 are "hardwired" and that it is stated in the immediately preceding sentence of the description on page 9, lines 11 to 14, that the PVLD module is not a "hardware accelerator". Although there are other embodiments, such as on page 8, lines 16 to 20, in which the PVLD is a "hardware accelerator", it is not directly and unambiguously derivable from the application as filed that the "hardwired" PVLD 306 is a hardware accelerator. Moreover, it is also not directly and unambiguously derivable that each of the hardware accelerators is hardwired.

18. For the above reasons, the board considers that the amended expression "each accelerator adapted to perform a decoding function by hardware" in claim 1 of the third auxiliary request introduces subject-matter extending beyond the content of the application as filed in violation of the requirements of Article 123(2) EPC.

19. Hence the appellant's third auxiliary request is not allowable.

Conclusion

20. Since none of the appellant's requests is allowable, the appeal must be dismissed.

Order

For these reasons it is decided that:

The appeal is dismissed.

The Registrar: The Chairman:

K. Boelicke C. Kunzelmann

Decision electronically authenticated