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**Datasheet for the decision
of 14 October 2019**

Case Number: T 0696/14 - 3.4.03

Application Number: 07709682.4

Publication Number: 1972008

IPC: H01L21/84

Language of the proceedings: EN

Title of invention:
SILICON CARBIDE DIMPLED SUBSTRATE

Applicant:
Cree, Inc.

Headword:

Relevant legal provisions:

EPC Art. 123(2), 111(1)
EPC 1973 Art. 56

Keyword:

Amendments - added subject-matter (no)
Inventive step - (yes)

Decisions cited:

Catchword:



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Case Number: T 0696/14 - 3.4.03

D E C I S I O N
of Technical Board of Appeal 3.4.03
of 14 October 2019

Appellant: Cree, Inc.
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Representative: Elkington and Fife LLP
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Decision under appeal: **Decision of the Examining Division of the
European Patent Office posted on 27 November
2013 refusing European patent application No.
07709682.4 pursuant to Article 97(2) EPC.**

Composition of the Board:

Chairman G. Eliasson
Members: M. Papastefanou
T. Bokor

Summary of Facts and Submissions

I. The appeal is against the decision of the examining division refusing the European patent application No. 07 709682.4 (published as WO 2007/081964 A2) on the ground that claims 13 and 19 of the sole request before it did not meet the requirements of Article 123(2) EPC.

II. The final request of the appellant was to set the decision under appeal aside and to grant a European patent on the basis of the following application documents:

- Description:

Pages 1, 2 filed with letter of 7 August 2019;

Pages 3, 3a, 4, 6, 9 filed of letter of
1 October 2018;

Pages 5, 7, 8, 10 as published;

- Page 11 filed with letter of 18 September 2019.

- Claims 1-13 filed with letter of 18 September 2019;

- Drawings: Sheets 1/6 - 6/6 as published.

III. Reference is made to the following documents:

D2: US 2002/0117681 A1;

D5: US 2003/0062526 A1;

D11: US 2005/0233539 A1;

D12: US 2004/051136 A1.

IV. Claim 1 is worded as follows:

A semiconductor device comprising:

a silicon carbide substrate (70) having a first main surface (12) and a second main surface (14) opposing the first main surface;

an active epitaxial device layer (60) on the first main

surface of the silicon carbide substrate;
a dimple (42) extending from the second main surface into the silicon carbide substrate toward the first main surface such that the dimple extends entirely through the silicon carbide substrate;
a doped epitaxial silicon carbide layer (44) on the second main surface of the silicon carbide substrate and within the dimple, the doped epitaxial silicon carbide layer having a conductivity type opposite a conductivity type of the silicon carbide substrate;
a first electrical contact (26) over the active epitaxial device layer; and
a second electrical contact (24) overlying the second main surface and within the dimple.

V. Independent claim 8 is worded as follows:

A method of forming a semiconductor device comprising:
epitaxially growing an active device layer (60) on a first main surface (12) of a silicon carbide substrate, the silicon carbide substrate having a second main surface (14) opposing the first main surface;
forming at least one dimple (42) extending from the second main surface into the silicon carbide substrate toward the first main surface such that the dimple extends entirely through the silicon carbide substrate;
forming a first electrical contact (26) over the active device layer;
epitaxially growing a doped silicon carbide layer (44) on the second main surface of the silicon carbide substrate and within the dimple, the doped epitaxial silicon carbide layer having a conductivity type opposite a conductivity type of the silicon carbide substrate;
and forming a second electrical contact (24) overlying

the second main surface and within the at least one dimple.

Reasons for the Decision

1. The appeal is admissible.
2. The invention
 - 2.1 The invention relates to a silicon carbide semiconductor device and a method for forming it.
 - 2.2 In high power semiconductor devices and LEDs, silicon carbide is a commonly used material for the substrate. With its relatively high thermal conductivity, silicon carbide provides an effective heat sink. At the same time, however, silicon carbide has high electrical resistance, something that affects the performance of the semiconductor device.
 - 2.3 In an effort to find a compromise between these two properties of silicon carbide, dimples are formed into the silicon carbide substrate (see for example Figure 1). In this way, a quantity of the silicon carbide is removed from the substrate, reducing its electrical resistance, while leaving sufficient material so that the substrate continues to function as an effective heat sink.
 - 2.4 The claimed invention proposes a way to decrease further the resistance of the substrate without removing more material. This is achieved by adding a doped epitaxial silicon carbide layer on the back side of the substrate (see "44" in Figure 7). This added doped epitaxial silicon carbide layer has a conductivity which is opposite to the one of the

substrate, achieving, thus, a reduction of the electrical resistance of the substrate.

3. Amendments - Extent of subject matter (Article 123(2) EPC)

3.1 In the decision under appeal, the examining division was of the opinion that claims 13 and 19 of the request before it did not fulfil the requirements of Article 123(2) EPC (see point 1 of the impugned decision).

The current request does not comprise the claims objected to by the examining division; this objection has thus become moot.

3.2 The subject-matter of claim 1 of the current request finds basis in original claims 1, 4 and 6. The subject-matter of independent claim 8 finds basis in original claims 17, 23 and 25 (see application as published).

3.3 Regarding the dependent claims:

- claim 2 is a combination of original claims 2 and 3;
- claim 3 finds basis in original claim 6;
- claim 4 corresponds to original claim 7;
- claim 5 corresponds to original claim 10;
- claim 6 is a combination of original claims 12, 13 and 14;
- claim 7 corresponds to original claim 11;
- claim 9 corresponds to original claim 22;
- claim 10 finds basis in original claim 25;
- claim 11 corresponds to original claim 26;
- claim 12 corresponds to original claim 28;
- claim 13 corresponds to original claim 31.

3.4 The amendments carried out in the description were adaptations to the new claims.

3.5 The board is, thus, satisfied that the application meets the requirements of Article 123(2) EPC.

4. Since the current request on file complies with the requirements of Article 123(2) EPC, it overcomes the sole ground of refusal invoked in the impugned decision.

Since, however, the issue of inventive step was discussed during the first instance procedure (see for example the summons to the oral proceedings before the examining division, point 3) and in the statement setting out the grounds of appeal (see page 2), the board decided to make use of the power conferred by Article 111(1) EPC and proceed to decide the case on its merits without remitting it to the examining division.

5. Inventive Step (Article 56 EPC 1973)

5.1 Closest prior art

5.1.1 The examining division was of the opinion that the subject-matter of claims 1, 13 and 19 did not involve an inventive step in view of document D11 in combination with the skilled person's common general knowledge, as exemplified in document D12 (see point 3 of the summons to the oral proceedings before the examining division).

5.1.2 The board does not share this opinion of the examining division.

The objection of the examining division was based mainly on the embodiment shown in Figures 6A to 6D of D11.

The board notes that there is no indication of a dimple (trench in D11) into the substrate (41 in Figures 6A to 6D). The examining division's objection was based on the more general definition of claims 13 and 19 (from the request then on file) where there is a "first layer" instead of a substrate. The examining division regarded the P+-type base layer 43 as the "first layer", trenches 47 as the dimples and the N-type channel layer 48 as the doped epitaxial layer of the claims.

As it has been already mentioned before, claims 13 and 19 are not comprised in the current request. In claim 1 there is the specific definition of a dimple extending into the silicon carbide substrate and therefore, this feature is not disclosed in D11. Furthermore, the N-type channel layer has the same conductivity type as the substrate 41.

The board is, thus, of the opinion that D11 is not suitable as a starting point for the skilled person because the device it describes differs significantly from the device of the claims.

Document D12, mentioned also by the examining division in the same communication, describes a device similar to the one in D11 (see Figure 3 of D12). Thus D12 cannot be considered to be suitable as closest prior art, either.

- 5.1.3 The board considers that documents D2 and D5 are more appropriate as closest prior art because they describe

devices with more features in common with the claimed invention.

- 5.1.4 D2 discloses devices (see Figures 1 to 3), which are similar to the one of the claims (compare with Figure 7 of the application). The layer on the second main (back) surface of the substrate and within the dimple (see "31" in Figure 3 and paragraph [0052] of D2) is, however, a dielectric layer and not a doped epitaxial silicon carbide layer as in the claimed device (layer (44) in Figure 7 of the application).
- 5.1.5 D5 also describes a semiconductor device similar to the one of the claims (see Figures 12 to 15). In this case, the layer (480) on the second main (back) surface of the substrate and within the dimple is a metallic seed layer (see paragraphs [0071]-[0072]).
- 5.2 Difference and technical problem
 - 5.2.1 As mentioned in points 5.1.4 and 5.1.5 above, the claimed semiconductor device differs from the ones in D2 and D5 in the nature of the additional layer formed in the back side (second main surface) of the substrate and within the dimple.
 - 5.2.2 In the claimed device, the additional layer is a doped epitaxial silicon carbide layer with a conductivity opposite to the one of the silicon carbide substrate. This has the technical effect of decreasing the resistance of the substrate, and thus improving the overall performance of the semiconductor device while maintaining a high thermal conduction through the substrate (see also appellant's letter of 1 October 2018).

5.2.3 In D2 the additional layer (31 in Figure 3 of D2) on the second main (back) surface of the substrate (and within the dimple) is a dielectric layer aiming to isolate electrically portions of the back side contact (20b) in order to prevent shorting of the device (see paragraph [0052]).

5.2.4 In D5, the additional layer (480 in Figure 12) is a metallic layer, which serves as a seed layer for the electroplating or electro-less plating that follows in order to fill the cavity (416) with an additional thermally conductive material (see paragraph [0071]).

5.2.5 Starting from either D2 or D5, the skilled person is, thus, faced with the technical problem how to decrease the resistance of the substrate.

5.3 Solution and obviousness

5.3.1 This technical problem is not considered either in D2 or in D5.

Moreover, there is nothing in D2 nor in D5 that would prompt the skilled person to add a doped epitaxial silicon carbide layer on the second main (back) surface of the corresponding semiconductor device. Thus he would not arrive at the claimed device without exercising any inventive skills.

D2 teaches even in the opposite way, since there is a dielectric layer (31) added between the electrical contact (20b) and the substrate (12).

5.3.2 Hence, the subject-matter of claim 1 involves an inventive step in the sense of Article 56 EPC 1973. The same applies to the subject-matter of independent claim

8, which defines the corresponding method.

6. The board concludes, therefore, that the application and the invention to which it relates meet the requirements of the EPC and EPC 1973 and a European patent is to be granted according to Article 97(1) EPC.

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.
2. The case is remitted to the department of first instance with the order to grant a patent in the following version:
 - Description, pages:
 - 1, 2 filed with letter of 7 August 2019;
 - 3, 3a, 4, 6, 9 filed with letter of 1 October 2018;
 - 5, 7, 8, 10 as published;
 - 11 filed with letter of 18 September 2019.
 - Claims 1-13 filed with letter of 18 September 2019;
 - Drawings: Sheets 1/6 - 6/6 as published.

The Registrar:

The Chairman:



S. Sánchez Chiquero

G. Eliasson

Decision electronically authenticated