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Datasheet for the decision of 26 February 2019

Case Number: T 0419/14 - 3.4.03

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Title of invention:
III-V HEMT DEVICES

Patent Proprietor:
TOYOTA JIDOSHA KABUSHIKI KAISHA

Opponent:
Infineon Technologies Austria AG

Headword:

Relevant legal provisions:
EPC Art. 52(1), 101(3)(a)
EPC 1973 Art. 56, 111(1)
RPBA Art. 12(1), 12(2), 12(4), 13(1)

Keyword:
Inventive step - main request (yes)
Late-filed document - admitted (yes)
Late-filed lines of attack - admitted (no)

Decisions cited:
T 1761/10

Catchword:

Europäisches Patentamt
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Beschwerdekammern

Boards of Appeal

Chambres de recours

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Case Number: T 0419/14 - 3.4.03

D E C I S I O N
of Technical Board of Appeal 3.4.03
of 26 February 2019

Appellant: (Opponent)	Infineon Technologies Austria AG Siemensstrasse 2 9500 Villach (AT)
Representative:	Moore, Joanne Camilla Jensen & Son 366-368 Old Street London EC1V 9LT (GB)
Respondent: (Patent Proprietor)	TOYOTA JIDOSHA KABUSHIKI KAISHA 1, Toyota-cho, Toyota-shi, Aichi-ken, 471-8571 (JP)
Representative:	Kuhnen & Wacker Patent- und Rechtsanwaltsbüro PartG mbB Prinz-Ludwig-Straße 40A 85354 Freising (DE)
Decision under appeal:	**Interlocutory decision of the Opposition Division of the European Patent Office posted on 19 December 2013 concerning maintenance of the European Patent No. 1779438 in amended form.**

Composition of the Board:

Chairman	G. Eliasson
Members:	T. M. Häusser
	W. Van der Eijk

Summary of Facts and Submissions

I. The appeal of the opponent concerns the interlocutory decision of the opposition division to maintain the European patent EP-B-1 779 438 as amended during the opposition proceedings (Article 101(3)(a) EPC).

II. The opposition had been filed against the patent as a whole on the grounds of added subject-matter and lack of inventive step (Articles 100(a), (c) and 56 EPC 1973).

III. The following documents were cited during the appeal proceedings:

D2: US 5,949,096,

D4: US 2001/0015437 A1,

D5: JP 2003059946,

D6: R. Coffie et al., *p-Capped GaN-AlGaN-GaN High-Electron Mobility Transistors (HEMTs)*, IEEE Electron Device Letter, Vol. 23, no. 10, October 2002, pages 588-590,

D7: O. Ambacher, Growth and applications of Group III-nitrides, J. Phys. D: Appl. Phys., vol. 31 (1998), pages 2653-2710,

D8: M. Kameche et al., *Comparing High-Frequency Control Devices*, Microwaves & RF, March 2003, pages 53-71,

D9: US 2002/0066908 A1.

IV. At the oral proceedings before the board the appellant (opponent) requested that the decision under appeal be set aside and that the patent be revoked.

The respondent (patent proprietor) requested that the appeal be dismissed and the patent thus be maintained

as upheld by the opposition division (main request) or, alternatively, the decision under appeal be set aside and the patent be maintained on the basis of one of auxiliary requests 1-4, filed with letter of 10 September 2014.

V. The wording of independent claims 1, 3, 5, and 7 of the main request is as follows:

"1. A transistor comprising:
a first layer (232);
a second layer (233) stacked on a top surface of the first layer (232);
a surface layer (235) stacked on a top surface of the second layer (233); and
a gate electrode (244) formed at a top surface side of the surface layer (235);
wherein the first layer (232) is a Gallium Nitride (GaN) compound comprising a first III-V nitride semiconductor,
the second layer (233) is a Gallium Nitride (GaN) compound comprising a second III-V nitride semiconductor having a second conductivity type of p or n type,
the surface layer (235) is a Gallium Nitride (GaN) compound comprising a III-V nitride semiconductor having a first conductivity type opposite to the second conductivity type, and
a band gap of the second III-V nitride semiconductor is wider than a band gap of the first III-V nitride semiconductor."

"3. A transistor comprising:
a first layer (232);
a plurality of units of layers (236 and 237, 238 and 239), wherein each of the units of layers (236 and 237, 238 and 239) comprises a second layer (236, 238) and an

upper layer (237, 239) stacked on a top surface of the second layer (236, 238), and each of the units of layers (238 and 239) is stacked on a top surface of a lower unit of layers (236 and 237); and
a gate electrode (244) formed at a top surface side of the uppermost unit of layers (238 and 239);
wherein the first layer (232) is a Gallium Nitride (GaN) compound comprising a first III-V nitride semiconductor,
the second layer (236, 238) is a Gallium Nitride (GaN) compound comprising a second III-V nitride semiconductor having a second conductivity type of p or n type,
the upper layer (237, 239) is a Gallium Nitride (GaN) compound comprising a III-V nitride semiconductor having a first conductivity type opposite to the second conductivity type, and
a band gap of the second III-V nitride semiconductor is wider than a band gap of the first III-V nitride semiconductor."

"5. A method for manufacturing a transistor having a first layer (232), a second layer (233) stacked on a top surface of the first layer (232), a surface layer (235) stacked on a top surface of the second layer (233), and a gate electrode (244) formed at a top surface side of the surface layer (235), the method comprising:
a step of growing the second layer (233) on the top surface of the first layer (232) by epitaxial growth;
a step of growing the surface layer (235) on the top surface of the second layer (233) by epitaxial growth;
a step of forming the gate electrode (244) at the top surface side of the surface layer (235);
wherein the first layer (232) is a Gallium Nitride (GaN) compound comprising a first III-V nitride semiconductor,

the second layer (233) is a Gallium Nitride (GaN) compound comprising a second III-V nitride semiconductor having a second conductivity type of p or n type,
the surface layer (235) is a Gallium Nitride (GaN) compound comprising a III-V nitride semiconductor having a first conductivity type opposite to the second conductivity type, and
a band gap of the second III-V nitride semiconductor is wider than a band gap of the first III-V nitride semiconductor."

"7. A method for manufacturing a transistor having a first layer (232), a plurality of units of layers (236 and 237, 238 and 239), and a gate electrode (244) formed at a top surface side of the uppermost unit of layers (238 and 239), wherein each of the units of layers (236 and 237, 238 and 239) comprises a second layer (236, 238) and an upper layer (237, 239) stacked on a top surface of the second layer (236, 238), and each of the units of layers (238 and 239) is stacked on a top surface of a lower unit of layers (236 and 237), the method comprising:
(a) a step of growing the second layer (236) on the top surface of the first layer (232) by epitaxial growth;
(b) a step of growing the upper layer (237) on a top surface of the second layer (236) by epitaxial growth;
(c) a step of growing the second layer (238) on a top surface of the upper layer (237) by epitaxial growth;
(d) a step of growing the upper layer (239) on a top surface of the second layer (238) by epitaxial growth;
(e) repeating the steps of (c) and (d) for a pre-determined cycle; and
(f) a step of forming the gate electrode (244) at a top surface side of an uppermost upper layer (239);
wherein the first layer (232) is a Gallium Nitride

(GaN) compound comprising a first III-V nitride semiconductor,
the second layer (236, 238) is a Gallium Nitride (GaN) compound comprising a second III-V nitride semiconductor having a second conductivity type of p or n type,
the upper layer (237, 239) is a Gallium Nitride (GaN) compound comprising a III-V nitride semiconductor having a first conductivity type opposite to the second conductivity type, and
a band gap of the second III-V nitride semiconductor is wider than a band gap of the first III-V nitride semiconductor."

VI. The parties argued essentially as follows:

(a) Admission of document D9

The *appellant* argued that document D9 was cited in response to the reasoning provided in the decision under appeal and should be admitted into the proceedings.

The *respondent* is of the opinion that document D9 was late filed and *prima facie* not relevant and should not be admitted into the proceedings.

(b) Admission of late-filed lines of attack

The *appellant* advanced for the first time during the oral proceedings before the board that it wished to argue inventive step starting from documents D5, D7, and D8 as closest state of the art.

The *respondent* stated that it was surprised by these new lines of attack but prepared to discuss inventive step starting from documents other than document D2.

(c) Main request - inventive step starting from D2 as closest state of the art

The *appellant* argued that the subject-matter of claim 1 of the main request differed from the device of document D2 merely in that the semiconductor layers were made of gallium nitride. Using this material did not involve an inventive step in view of documents D4, D5, D6, D8, and D9.

The *respondent* argued that it was not obvious for the skilled person to replace the gallium arsenide layers disclosed in document D2 by gallium nitride layers, because of the entirely different characteristics of these materials.

Reasons for the Decision

1. Procedural matters

1.1 Admission of document D9

1.1.1 The appellant cited document D9 for the first time in its letter setting out the grounds of appeal.

The respondent requested that this document be disregarded for being late-filed and not relevant.

1.1.2 The board notes that the claims of the main request, according to which the semiconductor layers of the claimed transistors are made of gallium nitride compounds, were only filed one month prior to the oral proceedings before the opposition division.

Moreover, document D9 relates indeed to adaptations necessary when considering gallium nitride transistors as opposed to gallium arsenide transistors. In the decision under appeal the fact that several such adaptations were necessary to arrive at the claimed subject-matter when starting from document D2 was regarded an indication that the invention involved an inventive step.

Hence, the board accepts that the appellant could not have been expected to file document D9 during the opposition proceedings and that it filed this document at the earliest possible occasion, namely with the grounds of appeal. Consequently, the board did not exercise its power under Article 12(4) RPBA to hold inadmissible document D9, which is thus part of the appeal proceedings in accordance with Article 12(1) and (2) RPBA.

1.2 Admission of late-filed lines of attack

1.2.1 The appellant stated at the oral proceedings before the board that - apart from arguing lack of inventive step based on document D2 as closest state of the art (see point 2 below) - it also intended to present other lines of attack based on documents D5, D7 and D8.

1.2.2 The respondent expressed its surprise concerning the new turn of events, but stated that it was prepared to discuss inventive step starting from documents other than document D2.

1.2.3 According to Article 12(2) RPBA, the statement of the grounds of appeal must contain a party's complete case and should specify all the facts, arguments and evidence relied on.

Any amendment to a party's case after it has filed its grounds of appeal may, according to Article 13(1) RPBA, be admitted and considered at the board's discretion. The discretion must be exercised in view of *inter alia* the complexity of the new subject-matter submitted, the current state of the proceedings and the need for procedural economy.

In particular, according to Article 13(3) RPBA, amendments sought to be made after oral proceedings have been arranged shall not be admitted if they raise issues which the board or the other party cannot reasonably be expected to deal with without adjournment of the oral proceedings.

1.2.4 In the present case the objections of lack of inventive step on the basis of any one of documents D5, D7, and D8 as closest state of the art were submitted for the first time at the oral proceedings before the board. Hence these objections were submitted after the statement of the grounds of appeal and are an amendment to the appellant's case within the meaning of Article 13(1) and (3) RPBA. Consequently, the admission of these objections is at the board's discretion (see T 1761/10, point 5 of the Reasons).

1.2.5 The appellant did not provide any justification for raising the new objections at such a late stage of the proceedings. Indeed, the board does not see any reason why the appellant should not have been in a position to submit these objections at the earliest possible stage of the appeal proceedings, i. e. with the grounds of appeal. In this case a thorough exchange of views concerning the objections could have taken place already during the written stage of the appeal proceedings.

1.2.6 By contrast, if the new objections were admitted into the appeal proceedings at the oral proceedings, the focus of the discussion could be expected to shift to entirely new issues which had played no role in the appeal proceedings up to that point.

For example, the appellant had merely discussed documents D5 and D8 rather briefly in order to show that gallium nitride devices had certain advantages over gallium arsenide devices. However, there had not been any discussion whether these documents disclosed the other claimed features, for example concerning the band gaps, doping and conductivity types of semiconductor layers of the disclosed devices. Document D7 being a lengthy review article had not been discussed at all in the appeal procedure.

Moreover, complex discussions could be expected to ensue, in particular in relation to the differing features of the claimed subject-matter over the new starting points in the assessment of inventive step, the technical effects of these features and the question whether it would be obvious for the skilled person to arrive at them.

1.2.7 The respondent might thus well find - contrary to its subjective initial appraisal of the new situation - that it cannot properly argue its case within the limited time available at the oral proceedings. Hence, according to the board's assessment neither the respondent nor the board can reasonably be expected to deal with the new objections during the scheduled oral proceedings.

1.2.8 In view of the above considerations, exercising its discretion under Article 13(1) and (3) RPBA, the board

did not admit into the appeal proceedings the new objections of lack of inventive step on the basis of any one of documents D5, D7, and D8 as closest state of the art.

2. Main request - inventive step starting from document D2 as closest state of the art

2.1 Document D2 as closest state of the art

In the decision under appeal the opposition division held that the closest state of the art must be a gallium nitride based device, namely document D8, but nevertheless assessed inventive step also starting from document D2 as closest state of the art (see point 19 of the Reasons).

The board is of the opinion that document D2 discloses - as detailed below - subject-matter that is conceived for the same purpose as the claimed invention, namely for providing a hetero-junction type field effect transistor, and has many relevant technical features in common with it. Inventive step may therefore well be assessed starting from document D2 as the closest state of the art.

2.2 Distinguishing features

2.2.1 In the decision under appeal the opposition division held that the subject-matter of claim 1 differed from the device of document D2 in that gallium nitride was used to form the semiconductor layers (see points 19.2 and 19.3 of the Reasons).

2.2.2 Document D2 discloses (see column 4, lines 25-53) a field effect transistor comprising a high purity

intrinsic-type GaAs buffer layer 12, a high purity $In_{0.15}Ga_{0.85}As$ channel layer 13, a Si-doped n-type $Al_{0.2}Ga_{0.8}As$ electron supply layer 14, a C-doped p-type $Al_{0.2}Ga_{0.8}As$ contact layer 15, and a Si-doped n-type GaAs cap layer 16, grown on a semi-insulating GaAs substrate 11 in this order by a MOCVD method. Next, after a photoresist layer 17 is patterned, the Si-doped n-type GaAs cap layer 16 is crystal-etched so as to expose a portion of the C-doped p-type $Al_{0.2}Ga_{0.8}As$ layer 15. Then a Schottky gate electrode 18 of a Ti/Pt/Au structure is formed on the exposed portion of the C-doped p-type $Al_{0.2}Ga_{0.8}As$ layer 15 in a vacuum vapor deposition apparatus. Next, ohmic electrodes 19 composed of AuGe/Ni/Au are formed as a source and a drain on the Si-doped n-type GaAs cap layer 16 on both sides of Schottky gate electrode 18 in the vacuum vapor deposition apparatus. Finally, heat treatment is performed at the temperature of 450°C for alloying such that ohmic alloy layers 20 are formed, thus completing the field effect transistor.

2.2.3 It is uncontested between the parties that document D2 discloses - using the wording of claim 1 of the main request - a transistor (field effect transistor) comprising:
a first layer ($In_{0.15}Ga_{0.85}As$ channel layer 13);
a second layer (Si-doped n-type $Al_{0.2}Ga_{0.8}As$ electron supply layer 14) stacked on a top surface of the first layer (channel layer 13);
a surface layer (C-doped p-type $Al_{0.2}Ga_{0.8}As$ contact layer 15) stacked on a top surface of the second layer (electron supply layer 14); and
a gate electrode (Schottky gate electrode 18) formed at a top surface side of the surface layer (contact layer 15);

wherein the first layer (channel layer 13) comprises a first III-V semiconductor ($In_{0.15}Ga_{0.85}As$),
the second layer (electron supply layer 14) comprises a second III-V semiconductor ($Al_{0.2}Ga_{0.8}As$) having a second conductivity type of p or n type (namely n-type),
the surface layer (contact layer 15) comprises a III-V nitride semiconductor ($Al_{0.2}Ga_{0.8}As$) having a first conductivity type (namely p-type) opposite to the second conductivity type (n-type).

2.2.4 The respondent argued that there was no disclosure in document D2 concerning the band-gap ratios of the semiconductor layers of the disclosed devices.

In the decision under appeal the opposition division held that the band gap of the $Al_{0.2}Ga_{0.8}As$ electron supply layer 14 was known to be larger than that of the $In_{0.15}Ga_{0.85}As$ channel layer 13 (see point 19.2 of the Reasons).

The board agrees with the opposition division and further notes that document D2 relates to hetero-junction type field effect transistors incorporating a junction between two materials with different band gaps, namely in particular between the $Al_{0.2}Ga_{0.8}As$ layer (having the wider band gap) and the $In_{0.15}Ga_{0.85}As$ layer (see D2, column 1, lines 34-41).

Hence, document D2 also discloses - using the claimed wording - that a band gap of the second III-V semiconductor ($Al_{0.2}Ga_{0.8}As$ electron supply layer 14) is wider than a band gap of the first III-V semiconductor ($In_{0.15}Ga_{0.85}As$ channel layer 13).

2.2.5 Consequently, the subject-matter of claim 1 of the main request differs from the device of document D2 in that

- the first layer is a Gallium Nitride compound comprising a first III-V nitride semiconductor,
- the second layer is a Gallium Nitride compound comprising a second III-V nitride semiconductor, and
- the surface layer is a Gallium Nitride compound comprising a III-V nitride semiconductor.

2.3 Objective technical problem

The board agrees with the appellant in that the effect of using gallium nitride as a base material is to allow operation at high temperatures (due to its large band gap) and high voltages (due to its high breakdown voltage). The objective technical problem is thus to achieve these effects.

2.4 Obviousness

2.4.1 In the decision under appeal the opposition division held that it would not be obvious for the skilled person to arrive at the claimed subject-matter, in particular in view of the fact that - when starting from document D2 as closest state of the art - various adaptations would be necessary to transform the normally-on device of document D2 into the claimed normally-off device (points 19.4 to 19.8 of the Reasons).

2.4.2 The opposition division thus assumed that the device of claim 1 of the main request was normally-off. However, at the oral proceedings before the board both parties agreed that the features of that claim did not necessarily imply that the claimed device was normally-off. The board agrees with this point of view, since many

characteristics of the semiconductor layers having an influence on this matter, such as the precise compositions, thicknesses and doping concentrations of the layers, are not specified in claim 1 of the main request.

2.4.3 Moreover, the board agrees with the appellant in that gallium nitride is known from documents D4, D5, D6, D8 and D9 to be used for the production of hetero-junction type field effect transducers and is also known to be a wide band gap semiconductor material with a high critical breakdown field. These documents would therefore be considered by the skilled person when attempting to solve the posed technical problem.

2.4.4 However, none of the documents D4, D5, D6, D8 and D9 discloses a gallium nitride based hetero-junction type field effect transistor having the claimed pn-junction (see second and third to last features of claim 1 of the main request). Such a pn-junction is only known from document D2 in combination with a gallium arsenide based hetero-junction type field effect transistor (see point 2.2 above).

Hence, the question arises whether the skilled person would - when starting from D2 as closest state of the art - retain the pn-junction disclosed in D2 when contemplating the use of gallium nitride for the production of a hetero-junction type field effect transducer.

The appellant was of the opinion that the skilled person would expect gallium nitride to show a similar behaviour to gallium arsenide and would thus not be dissuaded to retain the pn-junction when considering the use of gallium nitride in the device of document D2.

The board notes that the object stated in document D2 was to overcome large changes - in the known gallium arsenide based hetero-junction type field effect transistors - of the threshold voltage due to thickness variations of the electron supply layer. These were the result of the steep inclination of the electrostatic potential in the n-type $Al_{0.2}Ga_{0.8}As$ electron supply layer 4 under the Ti/Pt/Au Schottky gate electrode 7 in these known transistors. In order to stabilize the threshold voltage document D2 proposes to use a p-type $Al_{0.2}Ga_{0.8}As$ layer 15 between the Ti/Pt/Au Schottky gate electrode 18 and the n-type $Al_{0.2}Ga_{0.8}As$ electron supply layer 14, thereby rendering the electrostatic potential under the Schottky gate electrode 18 more gentle due to the pn-junction (see D2, column 1, lines 42-57; column 4, line 54 - column 5, line 5; Figures 2 and 6).

The gallium nitride hetero-junction type field effect transistors disclosed in documents D4, D5, D6, D8 and D9 differ not only in the base material from the gallium arsenide based transistors described in document D2, but also in the metal compositions of the respective gate electrodes and the doping levels of the respective electron supply layers and channel layers. It is therefore not considered evident for the skilled person that in these gallium nitride based transistors the electrostatic potential under the respective gate electrodes would behave similarly to the electrostatic potential of the transistor described in document D2.

Furthermore, due to the wider band gap of gallium nitride as compared to gallium arsenide the problem described in document D2 (large changes of the threshold voltage due to thickness variations of the electron supply layer) might not arise in gallium nitride based hetero-junction type field effect transistors at all.

In view of these considerations, the board is of the opinion that the skilled person would not - when starting from D2 as closest state of the art and attempting to solve the posed technical problem - replace the gallium arsenide layers of the transistor of D2 by gallium nitride layers and at the same time retain the pn-junction of that transistor. Rather, the skilled person would replace the entire transistor of document D2 by one of the known gallium nitride based heterojunction type field effect transistors.

2.4.5 Therefore, the subject-matter of claim 1 of the main request involves an inventive step over document D2 in combination with the documents D4, D5, D6, D8, and D9.

Claim 3 relates to a transistor corresponding to the transistor specified in claim 1 but comprising a plurality of pairs of layers of opposite conductivity type.

Independent method claims 5 and 7 correspond to respective device claims 1 and 3. Claims 2, 4, 6, and 8 are dependent on claims 1, 3, 5, and 7, respectively.

Accordingly, the subject-matter of claims 1 to 8 of the main request involves an inventive step over document D2 in combination with the documents D4, D6, D8, and D9 (Article 52(1) EPC and Article 56 EPC 1973).

3. Conclusion

Since the board is - as indicated above - of the opinion that the patent as upheld by the opposition division (main request) and the invention to which it relates meet the requirements of the EPC, the appeal is

to be dismissed (Article 101(3)(a) EPC and Article 111(1) EPC 1973). Consideration of the auxiliary requests is therefore not necessary.

Order

For these reasons it is decided that:

The appeal is dismissed.

The Registrar: The Chairman:

S. Sánchez Chiquero G. Eliasson

Decision electronically authenticated