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# Datasheet for the decision of 18 January 2019

**Case Number:** T 2288/13 - 3.4.01

**Application Number:** 04733859.5

**Publication Number:** 1639378

**IPC:** G01R31/28, H04L1/24, G06F11/267

**Language of the proceedings:** EN

**Title of invention:**
MEMORY BUS CHECKING PROCEDURE

**Applicant:**
Memory Technologies LLC

**Headword:**
Determination of usable bus width / Memory Technologies LLC

**Relevant legal provisions:**
EPC Art. 123(2)
EPC 1973 Art. 84

**Keyword:**
Amendments - added subject-matter (no)
Claims - clarity after amendment (yes)

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**Case Number: T 2288/13 - 3.4.01**

# D E C I S I O N
# of Technical Board of Appeal 3.4.01
# of 18 January 2019

| | |
|---|---|
| **Appellant:** (Applicant) | Memory Technologies LLC<br>6787 W. Tropicana Ave., Suite 238<br>Las Vegas, NV 89103 (US) |
| **Representative:** | Swindell & Pearson Limited<br>48 Friar Gate<br>Derby DE1 1GY (GB) |
| **Decision under appeal:** | **Decision of the Examining Division of the European Patent Office posted on 28 May 2013 refusing European patent application No. 04733859.5 pursuant to Article 97(2) EPC.** |

**Composition of the Board:**

| | |
|---|---|
| **Chairman** | P. Scriven |
| **Members:** | P. Fontenay |
| | J. Geschwind |

## Summary of Facts and Submissions

I. This is the Board's decision on the appeal filed by the applicant against the Examining Division's decision to refuse European patent application 04733859.

II. The application was refused because the independent claims according to the main request and two auxiliary requests then on file did not meet the requirements of clarity of Article 84 EPC.

The Examining Division held that independent claim 1 of the main request did not contain all features essential to achieving the object of identifying the number of usable bus lines between two electronic modules. In order to eliminate false interpretations, the handshake procedure between the modules required the exchange of two cycles of bit patterns. The subject-matter of claim 1 of the main request, defining only one cycle, could not provide reliable results. Moreover, the Examining Division considered that the context in which the claimed method and electronic modules were to be employed had to be specified. In particular, the fact that all bus lines needed to be fault-free, and the relative numbers of bus lines in the first and second modules needed to be specified in the independent claims.

The Examining Division further noted that the conditions recited in Rule 43(2) EPC justifying the existence of a plurality of independent claims in the same category were not met.

Finally, the Examining Division held that, even if the claim wording had been clear, the claimed subject-matter would have been obvious in view of document

D2: US-B-6 345 372.

As to the auxiliary requests, while acknowledging that some of the clarity issues did not apply to the independent claims, these claims, too, failed to define all essential features.

III. The appellant requested that the Examining Division's decision be cancelled in its entirety and that a patent be granted on the basis of one of four amended sets of claims, filed with the statement of grounds as a main request and first to third auxiliary requests.

IV. In the statement of grounds, the appellant provided arguments as to why the claimed subject-matter met the requirements of Article 84 EPC.

With regard to the main request, the appellant expressed the view that the independent claims did not need to incorporate the second cycle of exchange of a third and fourth bit patterns. It was stressed that the first round of the handshake procedure, consisting in the exchange of a first and a second bit pattern, provided valuable indications as to the electrical functionality of the data bus between the two modules. This information could then be combined with some additional information or assumptions regarding the type of bus in use, in order to increase the reliability of the obtained results. In practice, for example, the assumption that the number of bus lines

was an elevation [sic] of two (e.g. 4, 8, 16, ...) contributed to improving the reliability of the results.

Arguments with regard to novelty and inventive step with regard to D2 were also put forward.

V. In the course of oral proceedings before the Board, the appellant filed a new request consisting of a set of claims 1 to 13. It replaced all previous requests on file and defines the sole request on which the Board had to adjudicate.

VI. Claim 1 of the sole request reads:

*An electronic module (10), comprising:*
*means for conveying a first bit pattern, using multiple parallel bit lines of a data bus (120), to a further electronic module;*
*means for receiving a second bit pattern, using the multiple parallel bit lines of the data bus, in response to the first bit pattern;*
*means for comparing the second bit pattern with the first bit pattern, in order to identify a first section in which each bit has a value that is complementary to the corresponding bit of the first bit pattern;*
*means for conveying a third bit pattern, using the multiple parallel bit lines of the data bus, to the further electronic module, wherein each bit of the third bit pattern is complementary to the corresponding bit of the first bit pattern;*

*means for receiving a fourth bit pattern, using the multiple parallel bit lines of the data bus, in response to the third bit pattern;*
*means for comparing the fourth bit pattern with the third bit pattern, in order to identify a second section in which each bit has a value that is complementary to the corresponding bit of the third bit pattern; and*
*means for determining a usable width of the data bus based on the first and second sections.*

VII. Independent claim 10 reads:

*A computer program comprising code that, when run by a processor of an electronic module, causes the following to be performed by the electronic module:*
*conveying a first bit pattern, using multiple parallel bit lines of a data bus, to a further electronic module;*
*comparing a second bit pattern, received using the multiple parallel bit lines of the data bus in response to the first bit pattern, with the first bit pattern in order to identify a first section in which each bit has a value that is complementary to the corresponding bit of the first bit pattern;*
*conveying a third bit pattern, using the multiple parallel bit lines of the data bus, to the further electronic module, wherein each bit of the third bit pattern is*

*complementary to the corresponding bit of the first bit pattern;*
*comparing a fourth bit pattern, received using the multiple parallel bit lines of the data bus in response to the third bit pattern, with the third bit pattern in order to identify a second section in which each bit has a value that is complementary to the corresponding bit of the third bit pattern; and*
*determining a usable width of the data bus based on the first and second sections.*

## Reasons for the Decision

1. *Added subject-matter (Article 123(2) EPC)*

In the following, reference is made to the original application as filed, and published as WO 2005/003797.

1.1 Although focusing, primarily, on a a configuration associating a host device to a memory card, the description provides ample basis for a system associating, more generally, two electronic modules (cf. page 2, lines 18-20; page 3, lines 14-16). The handshake procedure described in relation to the system consisting of the host device and memory unit is the same as the one taking place between the two electronic modules (cf. page 10, lines 22-29).

The modules communicate with each other by means of a data bus whose functionality is to be checked (cf. page

2, lines 18-20; page 3, lines 14-16, page 10, lines 23-25, Figure 5). They both operate according to specific rules embodied in dedicated program code.

1.2 As such, each module constitutes a separate and independent unit which may be claimed on its own, as acknowledged on page 4, line 6 to page 5, line 4 by reference to the third and fourth aspects of the invention, respectively. More specifically, for the electronic module of current claim 1, reference is made also to original claim 24.

The claimed module incorporates the features of a software program for checking the electronic functionality of the data bus. The functional limitations recited in claim 1 reflect, in substance, the content of the first and second codes of the software program referred to on page 4, lines 17-28 of the published application. Concretely, the cited passages establish the existence within the first electronic modules of:
means for conveying a first bit pattern, using multiple parallel bit lines of a data bus to a further electronic module;
means for receiving a second bit pattern, using the multiple parallel bit lines of the data bus, in response to the first bit pattern; and
means for comparing the second bit pattern with the first bit pattern.

Regarding the existence of the means for receiving the second bit pattern, reference is made to the evocation of the "second bit pattern received from the memory" on page 4, lines 25 and 26 and to a similar reference in original claim 26. Both passages establish, without ambiguity, the existence within the first electronic

module of the corresponding receiving means. Further support for the recited features can be found in the passage describing the program to be used in the first electronic module, as such, on page 3, line 14 to page 4, line 5.

Support for the step of comparing the second bit pattern with the first bit pattern may be found, for example, in original claim 2; in page 2, lines 28 and 29; and in page 3, lines 18-24. The concept of a first section, in which each bit has a value that is complementary to the corresponding bit of the first bit pattern can be derived from the passage on page 3, lines 5-7, or from the evocation in original claim 6 of "a section in which the pattern is complement to the corresponding part of the first bit pattern". Although different, the wording in claim 1 is technically equivalent to the original wording in these passages.

With regard to the second cycle of the handshake procedure, in which a third bit pattern is generated and a fourth bit pattern received and compared, reference is made to page 10, lines 36-39 of the application as filed according to which: "*If desirable, a second cycle can be carried out, similar to steps 220 to 240. Preferably, the test bit pattern in the second cycle is complementary to the test bit pattern in step 220. The second cycle can be used to ensure that no bit in the data bus is stuck to "0" or "1"* ". Further support can be found on page 3, line 29 - page 4, line 5.

Figure 6 is a schematic representation of the algorithm implemented in the first electronic module. It establishes without ambiguity that the steps to be performed with regard to the third and fourth bit

patterns are carried out according to the same set of rules as those applying to the first and second bit pattern. This directly results from the steps 210 to 240 being repeated in a loop following the first implementation of step 240. Only then is the determination of the data width carried out.

Furthermore, the very purpose of the claimed module is to provide a reliable indication of the usable bus width by excluding the bits that are stuck at 0 or 1. This requires the use of the first and second sections (cf. claims 5 and 7 together with Figure 6).

Explicit reference to the fact that each bit of the third bit pattern is complementary to the corresponding bit of the first bit pattern can be found in original claim 17 and on page 10, line 37-39.

1.3 Concerning independent claim 10, reference is made, primarily, to original claims 12, 13, 16 and 17. Original independent claim 12 refers to a software program for use in a first electronic module for checking the functionality of a data bus between two electronic modules. Original claim 13 recites, more specifically, that the purpose of the software program is for determining a usable bus width, as now recited in claim 10.

Explicit reference to a section of the second bit pattern in which the pattern is complementary to the corresponding part of the first bit pattern is to be found in original claim 16. The wording used in current claim 10 is technically equivalent to the original wording in original claim 16.

As underlined above with regard to claim 1, the embodiment illustrated in relation with Figure 6 provides a sufficient basis for a repetition of the handshake procedure with a third pattern being conveyed and a fourth pattern being received by the electronic module in which the claimed computer program is to be implemented.

Similarly, Figure 6 and the corresponding description establish that the bus width is to be determined on the basis of a repetition of steps 220 to 240, that is, on the basis of a (first) section being identified in a first cycle of exchanged bit patterns, and a subsequent (second) section being identified in a second cycle of bit patterns being exchanged.

Original claim 17 and page 10, line 37-39, explicitly establish that each bit of the third bit pattern is complementary to the corresponding bit of the first bit pattern.

A further confirmation for a repetition of the exchange procedure is to be found in original claim 17, where it is specified that the fourth bit pattern has "a predetermined relationship to the received third bit pattern, so as to allow the further code to determine the usable width of the data bus".

*2. Clarity (Article 84 EPC)*

2.1 Claim 1 incorporates the features as to the means for conveying a first and third bit patterns and the associated means for receiving, in response, second and fourth bit patterns.

The determination of the usable bus width, carried out on the basis of a conveyed first bit pattern and received second bit pattern, is not sufficient to establish with certainty whether an expected 0 (or 1) in the second bit pattern is the result of complementing operations taking place in the second electronic module, or simply the consequence of a bit in the data bus being stuck at 0 (or 1). This is acknowledged in the original application, since it proposes improving the reliability by making assumptions as to the expected width of the used bus.

By incorporating the features of the second exchange of bit patterns, claim 1 incorporates all the features actually required to solve the problem of providing reliable information as to the usable bus width.

The claimed inventions specify that each bit of the third bit pattern is complementary to the corresponding bit of the first bit pattern. This feature is essential in view of the problem to be solved, because a mere repetition of a bit on one line would not permit the resolution of the ambiguities resulting from that line being stuck at 0 or 1.

2.2 The claimed electronic module is defined in terms of functional limitations. It corresponds to a (first) electronic module within a system incorporating another (second) electronic module, which is programed to provide the expected complementary second and fourth bit patterns in response to the first and third bit patterns conveyed by the first module. The first electronic module, however, defines a physical entity that exists as stand-alone unit, independently of the second electronic module.

It is established case law of the Boards of Appeal that, under such circumstances, a claim does not need to be limited to the system and to incorporate the features of the external units, although said units are required for the whole system to operate. The situation is equivalent to the case of an invention consisting of a plug and socket or of an audio/video coder and decoder. In the present situation, the requirement as to clarity is met insofar as the claimed module incorporates all the functionalities actually required to determine the usable bus width. Should the second electronic module not be able to respond to the first and third bit patterns by generating the expected complementary second and fourth bit patterns, for example, because it does not include the required program code, the claimed module will conclude that no communication is actually possible, i.e. that the usable bus width is zero.

2.3 Claim 1 defines a first section of the second bit pattern and a second section of the fourth bit pattern. It further specifies that the usable data width is determined on the basis of the identified first and second sections, that is, on those sections in which each bit has a value that is complementary to the corresponding bit of the first, respectively, third bit pattern. The Board is satisfied that claim 1 reproduces all information required for determining the usable width of the data bus based on the first and second sections previously identified.

The steps recited in claim 1 regarding the exchanges of bit patterns combined with the conditions that the second, third and fourth patterns should meet with regard to the first bit pattern, and the further definitions regarding the first and second sections,

constitute clear guidelines as to how the problem underlying the claimed invention is to be solved. In this respect, the claimed definitions are not limited to simply claiming said underlying problem but incorporate concrete measures as to how this is to be achieved. The final step of determining the usable width of the data bus based on the first and second sections is straightforward. Since each of said sections provides an indication as to the maximal usable bus width, it follows that the actual usable width is the lowest of the two values thus obtained.

The computer program of claim 10 reproduces the corresponding limitations embodied in its code.

2.4 Consequently, the claims meet the requirements of Article 84 EPC as to the conditions of clarity and support by the description.

3. The claims of the appellant's sole request do not contain subject-matter extending beyond the content of the application as filed (Article 123(2) EPC). They are clear and concise in the sense of Article 84 EPC.

**Order**

**For these reasons it is decided that:**

1. The decision under appeal is set aside.

2. The case is remitted to the to the department of first instance for further prosecution on the basis of the sole request of the appellant (claims 1 to 13) filed during the oral proceedings on 18 January 2019.

The Registrar: The Chairman:

K. Götz-Wein P. Scriven

Decision electronically authenticated