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Case Number: T 1998/13 - 3.4.03

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Language of the proceedings: EN

Title of invention:
SILICON CARBIDE MOSFETS WITH INTEGRATED ANTIPARALLEL JUNCTION BARRIER SCHOTTKY DIODE AND METHODS OF FABRICATING SAME

Applicant:
Cree, Inc.

Headword:

Relevant legal provisions:
EPC 1973 Art. 56

Keyword:
Inventive step - all requests (no)

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T 0164/92

Catchword:

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Case Number: T 1998/13 - 3.4.03

D E C I S I O N
of Technical Board of Appeal 3.4.03
of 3 May 2018

Appellant: (Applicant)	Cree, Inc. 4600 Silicon Drive Durham, NC 27703 (US)
Representative:	Boult Wade Tennant Verulam Gardens 70 Gray's Inn Road London WC1X 8BT (GB)
Decision under appeal:	**Decision of the Examining Division of the European Patent Office posted on 23 April 2013 refusing European patent application No. 04712840.0 pursuant to Article 97(2) EPC.**

Composition of the Board:

Chairman	G. Eliasson
Members:	M. Papastefanou
	T. Bokor

Summary of Facts and Submissions

I. The appeal is against the decision of the Examining Division refusing the European patent application No. 04 712 840.0 (published as WO 2004/097944 A2) on the grounds that the subject matter of independent claims 1, 12, 26 and 36 of the request before it did not involve an inventive step.

II. Reference is made to the following documents, cited in the decision under appeal:

D2: US 4 811 065 A
D3: US 5 111 253 A.

III. At the end of the oral proceedings before the Board, the Appellant's request was to set the decision under appeal aside and to grant a patent according to the Main request or one of the First, Second, Third and Fourth Auxiliary requests, all filed with its letter dated 3 April 2018.

IV. Claim 1 of the **Main request** is worded as follows:

A silicon carbide semiconductor device for blocking voltages of greater than 600V, comprising:
a silicon carbide DMOSFET;
an integral silicon carbide junction barrier Schottky (JBS) diode configured to have a turn-on voltage lower than a turn-on voltage of a built-in body diode of the DMOSFET, the silicon carbide JBS diode comprising:
a p-type junction barrier Schottky (JBS) grid having a plurality of spaced apart p-type silicon carbide regions (26), including a peripheral p-type region of the p-type JBS grid (40) adjacent a source region (22) of the DMOSFET and in contact with a p-type well region

(20) of the DMOSFET, the peripheral p type region of the JBS grid having a higher doping concentration than a doping concentration of the p-type well region (20) of the DMOSFET;
the silicon carbide JBS diode further comprising a Schottky contact (30) on the p-type JBS grid; and
wherein a source contact (24) of the DMOSFET is on a portion of the peripheral p-type region of the JBS grid and forms an ohmic contact with the peripheral p-type region of the JBS grid (26).

V. The wording of Claim 1 of the **First Auxiliary request** is as follows:

A silicon carbide semiconductor device for blocking voltages of greater than 600V, comprising:
a silicon carbide DMOSFET;
an integral silicon carbide junction barrier Schottky (JBS) diode configured to have a turn-on voltage lower than a turn-on voltage of a built-in body diode of the DMOSFET, the silicon carbide JBS diode comprising:
a p-type junction barrier Schottky (JBS) grid having a plurality of spaced apart p-type silicon carbide regions (26), including a peripheral p-type region of the p-type JBS grid (40) adjacent a source region (22) of the DMOSFET and in contact with a p-type well region (20) of the DMOSFET, the peripheral p type region of the JBS grid having a higher doping concentration than a doping concentration of the p-type well region (20) of the DMOSFET;
the silicon carbide JBS diode further comprising a Schottky contact (30) on the p-type JBS grid; and
wherein a source contact (24) of the DMOSFET that comprises a material different than the Schottky contact (30) is on a portion of the peripheral p-type region of the JBS grid and on a portion of the source

region (22), the source contact (24) being annealed so as to form an ohmic contact with the peripheral p-type region of the JBS grid (26) and the source region (22).

VI. Claim 1 of the **Second Auxiliary request** is worded as follows:

A silicon carbide semiconductor device for blocking voltages of greater than 600V, comprising:
a silicon carbide DMOSFET;
an integral silicon carbide junction barrier Schottky (JBS) diode configured to have a turn-on voltage lower than a turn-on voltage of a built-in body diode of the DMOSFET, the silicon carbide JBS diode comprising:
a p-type junction barrier Schottky (JBS) grid having a plurality of spaced apart p-type silicon carbide regions (26), including a peripheral p-type region of the p-type JBS grid (40) adjacent a source region (22) of the DMOSFET and in contact with a p-type well region (20) of the DMOSFET, the peripheral p-type region of the JBS grid having a higher doping concentration than a doping concentration of the p-type well region (20) of the DMOSFET;
the silicon carbide JBS diode further comprising a Schottky contact (30) on the p-type JBS grid;
wherein a source contact (24) of the DMOSFET that comprises a material different than the Schottky contact (30) is on a portion of the peripheral p-type region of the JBS grid and on a portion of the source region (22), the source contact (24) being annealed so as to form an ohmic contact with the peripheral p-type region of the JBS grid (26) and the source region (22); and
wherein the active area of the integral JBS diode is less than the active area of the DMOSFET and the active area of the integral JBS diode relative to the active

area of the DMOSFET is selected to flow a full switch current of the DMOSFET at a forward bias voltage of less than or equal to 2.6V.

VII. Claim 1 of the **Third Auxiliary request** has the following wording:

A silicon carbide semiconductor device for blocking voltages of greater than 600V, comprising:
a silicon carbide DMOSFET;
an integral silicon carbide junction barrier Schottky (JBS) diode configured to have a turn-on voltage lower than a turn-on voltage of a built-in body diode of the DMOSFET, the silicon carbide JBS diode comprising:
a p-type junction barrier Schottky (JBS) grid having a plurality of spaced apart p-type silicon carbide regions (26), including a peripheral p-type region of the p-type JBS grid (40) adjacent a source region (22) of the DMOSFET and in contact with a p-type well region (20) of the DMOSFET, the peripheral p-type region of the JBS grid having a higher doping concentration than a doping concentration of the p-type well region (20) of the DMOSFET;
the silicon carbide JBS diode further comprising a Schottky contact (30) on the p-type JBS grid;
wherein a source contact (24) of the DMOSFET that comprises a material different than the Schottky contact (30) is on a portion of the peripheral p-type region of the JBS grid and on a portion of the source region (22), the source contact (24) being annealed so as to form an ohmic contact with the peripheral p-type region of the JBS grid (26) and the source region (22); and
wherein an active area of the integral silicon carbide JBS diode is ***less than 50%*** *the active area of the*

silicon carbide DMOSFET (emphasis by the Board).

VIII. Claim 1 of the **Fourth Auxiliary request** has the same wording with claim 1 of the Third Auxiliary request with the exception that in the last feature it is defined that *an active area of the integral silicon carbide JBS diode is **less than 25%** the active area of the silicon carbide DMOSFET* (emphasis by the Board).

Reasons for the Decision

1. The appeal is admissible.

2. Closest prior art

It remained undisputed that document D2 represented the closest prior art to the claimed invention. Since some aspects of its disclosure were disputed throughout the examination and appeal proceedings, the Board will establish the disclosure of D2 first.

2.1 D2 describes a semiconductor device comprising a DMOSFET with an integral junction barrier Schottky (JBS) diode (see Figure 6 and column 3, lines 11-16) configured to have a turn-on voltage lower than the one of the built-in body diode of the DMOSFET (column 4, lines 40-46). The device in D2 comprises further a plurality of spaced apart P+ type body regions forming a p-type JBS grid (*P-N junction guard ring*, see column 4, lines 17-21), in the drift N type region (see P+ type regions 112 in Figure 6). The JBS diode comprises also a Schottky contact (110) adjacent and coupled to the source region (82, 92) of the DMOSFET (see Figure 6 and column 4, lines 8-21).

2.2 The contested points during the first and the second instance proceedings were whether D2 disclosed or not the following features (see Figure 2A of the application and claim 1 of all requests on file):

(a) the p-type JBS grid including a peripheral p-type region adjacent a source region (22) of the DMOSFET and in contact with a p-type well region (20) of the DMOSFET; and
(b) the peripheral p-type region of the JBS grid having a higher doping concentration than a doping concentration of the p-type well region (20) of the DMOSFET.

2.3 In the impugned decision, as well as in the Board's preliminary opinion, it was asserted that, despite no corresponding explicit disclosure in D2, the P+ type body regions 81 and 91 (in Figure 6), comprised two different regions with two different doping concentrations. The first region, which was the thinner part below and to the external side of the N+ type source regions and which contained also the channel regions 84 and 94 corresponded to the p-type well region of the claim (i. e. it belonged to the DMOSFET) and had a first doping concentration (P). The remaining part, the deep body regions 81 and 91 belonged to the JBS grid (*guard ring* in D2) and had a higher doping concentration (P+) than the first part. This interpretation appeared to be corroborated by the description of the prior art semiconductor device of Figure 2. With reference to this figure, it was described (see column 1, lines 49-54) that within the N type layer 54 there was a P+ type deep body region 56 (which corresponded to the region labelled 81/91 in Figure 6) and a P body region 57. Within body region 57 there were N+ source regions 58, 60 (corresponding to

regions 82 and 92 of Figure 6). Between the diffusion boundaries of source regions 58, 60 and body region 57 there were channel regions 61, 63.

2.4 The Appellant contested these assertions.

2.4.1 Regarding feature (b), the Appellant argued that there was no indication in D2 that the P+ type body region of the DMOSFET (81/91 in Figure 6) comprised two parts with different doping concentrations. Figure 2 referred to a device of the state of the art - with respect to the invention described in D2 - and could not be taken as basis for understanding the device in Figure 6. Moreover, there were passages in the description that indicated that the whole of the P+ type body regions 81 and 91 in Figure 6 had a uniform, high doping concentration P+ (column 4, lines 3-5 and line 11).

2.4.2 Furthermore, making reference to document D3, the Appellant argued that the purpose of the P+ type deep body region 56 in Figure 2 of D2 was to increase resistance of the DMOSFET to avalanche breakdown. Since there was no need for such protection in the device of Figure 6, there was no need to have two different doping concentrations in the P+ type body regions 81 and 91.

2.4.3 Regarding feature (a), the Appellant argued that, since there was only one P+ type body region (81/91) in the DMOSFET of the device of Figure 6 with a homogenous doping concentration, it was clear that this area belonged to the DMOSFET and not to the JBS grid. In addition the JBS grid p-type regions (26) of the claimed invention had almost the same depth as the p-type well region (20) of the DMOSFET: 0.3 µm to 1.5 µm for the JSB grid (page 9, lines 30-32) and 0.5 µm to

1.5 µm for the DMOSFET (page 9, lines 5-7). In D2, although there were no explicit statements about the depths of the corresponding regions, it was evident from Figure 6 that the P+ type body region of the DMOSFET (81/91) was deeper than the P+ type regions of the JBS grid (112). This was another indication that body region 81/91 belonged to the DMOSFET and not to the JBS grid and, hence, feature (a) was not disclosed in D2.

2.5 The Board is not convinced by the Appellant's arguments.

2.5.1 According to established case law and practice of the EPO, the disclosure of a publication is determined by what knowledge and understanding can and may be expected of the average skilled person (T 164/92 OJ EPO 1995, 305, Corr 387; Headnote I). In other words, the disclosure of a publication comprises what the skilled person can derive from it, directly and unambiguously, and based on his common general knowledge (Case Law of the Boards of Appeal of the EPO, 8th edition, I.C.4.1). Furthermore, the skilled person using his common general technical knowledge and consulting the reference literature would also be cable to recognise which information in the prior art document was not correct (Case Law of the Boards of Appeal of the EPO, 8th edition, I.C.4.9)

2.5.2 With regards to the doping concentration in the body region (81/91) of the device on Figure 6 of D2, the Board notes at first that it is generally known (and it was so before the priority date of the application) that the doping concentration of the p-type well region of a MOSFET has a direct impact on the value of the threshold voltage of the MOSFET, i. e. the voltage

which has to be applied at the gate to create a channel so that current can flow through the MOSFET. The higher the doping concentration of the p-type well region of the MOSFET, the higher the threshold voltage is.

In the device of Figure 6, in order to create a channel at the channel region (94), which will permit current to flow from the source N+ region (92) into the drift N region (102), a voltage has to be applied at the gate (96).

As is also generally known, high voltages applied at the gate can cause damage to the DMOSFET, by causing the destruction (collapse) of the gate insulator (93), for example. Hence, the doping concentration of the p-type region at the channel region has to be moderate.

At the same time, the p-type region of the DMOSFET has to be grounded via the source contact, which indicates that there must be an ohmic contact between the anode (110) and the body region 91. In order to achieve this ohmic contact, the doping concentration of the semiconductor contacting the anode must be high, as also indicated by the P+ symbol in Figure 6.

2.5.3 In the prior art device of Figure 2, there is a distinction between the two parts of the p-type body region, as explained above. The Board does not agree with the Appellant that the device of Figure 6 is a completely different device to the one in Figure 2. The skilled person recognises the problem of the device in Figure 2 (slowing down of the switching frequency because of the body diode of the DMOSFET, like in the present application) and tries to improve the device by integrating a built-in JBS diode (like in the claimed invention). There is no reason for the skilled person

to modify the doping concentration of the various semiconductor regions of the device when integrating the JBS diode into it.

2.5.4 The Board concludes, therefore, that the skilled person, taking into account the generally known operation principles of the DMOSFET, would understand that the body regions 91 and 81 of Figure 6 comprise two distinct parts with two different doping concentrations (P+ of the internal, deeper part and P for the external, thinner part which includes the channel region), despite the statements on column 4 of D2 pointed out by the Appellant, which would, thus, be understood as errors, or merely as imprecise statements, in that the authors of D2 did not specifically emphasise that also the body regions 81 and 91 in the device of Figure 6 had in fact two different doping concentrations.

2.6 Regarding feature a), the Board remarks at first that the naming of the various regions in the device in D2 and in the application does not define their actual function. In the claimed invention (Figure 2A of the application), the peripheral p-type regions (26) of the JBS grid which are in contact with the p-type well regions (20) of the DMOSFET play two roles: by providing an ohmic contact of the p-type well region (20) to the source contact (24) of the DMOSFET (see also page 10, lines 5-7) they are part of the DMOSFET and, at the same time, they are part of the JBS grid since they operate with the remaining p-type regions (26) to remove the depletion region of the JBS diode away from the Schottky contact (30) when the diode is reverse biased, diminishing, thus, the leakage current.

2.6.1 In the same way, in the device of Figure 6 of D2, the P+ type body region 81/91 (the internal, deeper part) provides the ohmic contact between the anode (110) (i. e. the source contact) and the P type region (the external, thinner part containing the channel region) and at the same time it operates with the other P+ type regions (112), as part of the JBS grid, to diminish any leakage currents of the Schottky diode during reverse bias.

2.6.2 The figures in D2 are rather schematic - something also acknowledged by the Appellant - and no conclusions can be drawn about the depths of the various regions.

2.7 For the above reasons, the Board reaches the conclusion that both features a) and b) (see point 2.2) are implicitly disclosed in D2 for the skilled person.

3. Main request

3.1 In view of the above, the features distinguishing Claim 1 of the Main request from D2 are that the semiconductor device is made of silicon carbide (SiC) (instead of silicon - Si - in D2) and that it is suitable for blocking voltages greater than 600V (there is no such explicit disclosure in D2).

3.2 The use of SiC in the manufacture of semiconductor devices like the one of the claims is well known in the art and was so by the priority date of the application. It is also known that one of the advantages of SiC when compared to Si is that semiconductor devices made of SiC can achieve higher blocking voltages than when they are made of Si (e. g. in the range of 600 - 3300V depending also on the type of SiC used).

3.3 It is also well known that the use of SiC in the manufacture of semiconductors became widespread during the 1990's. D2 was published in 1989 and the present application has a priority date in 2003. Hence, the skilled person reading D2 on the priority date of the application, and based only on his common general knowledge, would readily recognise the advantages of using SiC instead of Si in the semiconductor device of D2 - especially in an effort to achieve higher blocking voltages - and would be prompted to manufacture such a device in an obvious and straightforward manner.

3.4 The Appellant argued essentially that the replacement of Si with SiC in the context of the device of D2 was not such a straightforward step. SiC was a more complex material when compared to Si and it introduced several new aspects and problems the skilled person would have to take into account. Hence, it could not be simply said that using SiC instead of Si was an obvious step the skilled person would take without exercising any inventive skill.

3.5 The Board is not convinced by this argument. As already stated previously, the use of SiC in devices like the ones of D2 was generally known by the priority date of the application. For the skilled person, such common general knowledge would also include the various characteristics of SiC, as well as its advantages and disadvantages over other commonly used materials such as Si. If the skilled person knew that SiC was a more suitable material, he would be prepared to accept that it may be more difficult to work with. He would only be dissuaded if he would expect the problems to be extreme or outright insurmountable. In the description of the application, reference is made to technical literature that refers to comparison between SiC and Si for use in

power devices (see lines 2-4 on page 2), something that confirms that such issues were already part of the common general knowledge in the technical field in question by the priority date of the application.

3.6 The Board's conclusion is, thus, that the subject matter of claim 1 of the Main request does not involve an inventive step.

4. First Auxiliary request

4.1 The features distinguishing claim 1 of the First Auxiliary request from D2 are the use of SiC instead of Si as a semiconductor material and the fact that the Schottky contact and the source contact are made of different materials, the latter being in addition annealed.

4.2 In D2, there is one contact/anode (110 in Figure 6) which serves both as contact for the integrated JBS diode as well as the source contact of the DMOSFET (column 3, lines 26-30). The type of contact made with the different semiconductor regions of the device depends on the doping concentration of the corresponding semiconductor material. Hence, there are ohmic contacts with the source N+ regions (82, 92) and the P+ body regions (81, 91, 112) but there is a Schottky contact with the N (drift) region (102) (see column 4, lines 8-21).

4.3 In the grounds of appeal, the Appellant argued that, by having two separate contacts made of different materials, one for the source contact of the DMOSFET and one for the Schottky contact of the JBS diode, it was possible to anneal the former in order to be able to create an ohmic contact with the n-type source

region and p-type peripheral region of the JBS grid irrespective of the doping concentration of the underlying semiconductor regions, avoiding thus any constraints for the doping concentration of these regions, and in particular for the source region (see grounds of appeal, page 6).

4.4 The Board notes that the two contacts are physically contacting each other (Figure 2A) and that there is a metallic overlayer (36) over both of them (page 11, lines 2-9). The two contacts are, thus, at least electrically coupled to each other (as defined also in the claim).

4.4.1 From D2, where there are no specific values of the doping concentrations of the various semiconductor regions mentioned, it appears that the doping concentrations of the various semiconductor regions that were necessary in order to achieve different types of contact (ohmic and Schottky) with the same anode were generally known. It is specifically stated in D2 that the semiconductor device is manufactured using well-known techniques in an obvious manner (column 5, lines 3-5).

4.4.2 Moreover, annealing was a well known technique before the priority date of the application and its advantages, disadvantages and effects on the metals that were being annealed were generally known.

4.4.3 Summarising, in D2 there is a semiconductor device with a single contact/anode where the type of contact between this anode and the various semiconductor regions underlying it depends on the doping concentration of each region. In the claimed device, a more complicated construction of two contacts and an

overlayer is used, with one of the contacts being annealed in order to guarantee an ohmic contact with the underlying semiconductor regions allowing lower doping concentration in these regions. Hence, although these features of the claim indeed relieve the constraints regarding the doping concentration of the semiconductor source region, they also create the disadvantage of a more complicated structure of the contact/anode of the device.

The Board concludes, therefore, that the skilled person starting from D2 would apply the solution of the claim to the device of D2 in an obvious and straightforward manner should specific needs and circumstances create such a need, since both solutions present known advantages and disadvantages.

4.5 The Appellant argued that the claimed solution was not a mere question of weighing advantages and disadvantages of the two solutions. As already argued previously, SiC was a more complex material than Si and its use in the semiconductor device raised issues which the skilled person could not foresee when taking the decision to replace Si with SiC. The selection of two different materials for the Schottky and the source contacts provided an improved control of the operation of the device, since it allowed for the optimal choice of materials for both cases. In particular, regarding the Schottky contact, the choice of material would have a direct influence on the turn-on voltage of the JBS diode, which had to be lower than the body diode of the DMOSFET in order to guarantee the desired operation. In D2 such issues were not present, since Si was not such a complicated material like SiC. The skilled person would have no motivation to change the elegant, simple construction of the device in Figure 6 of D2, which had

only one anode/contact, and decide for the more complicated, more difficult to manufacture solution of having two different contacts made of two different materials as in the claimed device.

4.5.1 The Board cannot follow this argument. As already explained with regard to the Main request, SiC as semiconductor material and its use in devices like the ones of D2 were generally known before the priority date of the application. The skilled person taking the obvious step of replacing Si with SiC in the device of Figure 6 of D2 would be aware of the additional issues raised by the introduction of SiC. Moreover, the Schottky barrier values for materials to be used as Schottky contacts were generally known and well documented by the priority date, so the skilled person would be in a position to select the appropriate material for the Schottky contact based only on his common general knowledge.

4.5.2 It was also well known that a Schottky diode would normally have a lower turn-on voltage than a p-n diode with the same semiconductor material. The skilled person would, thus, know that the JBS diode in the device of Figure 6 would turn on before the body diode of the DMSOSFET. Furthermore, in the application it is already suggested that the decision to use different materials for the Schottky and source contacts was to be weighted against ease of manufacture of the contacts (see page 16, lines 4-8), implying that this decision was more a question of optimisation than of some unexpected technical effect.

4.6 The Board concludes, thus, that the subject matter of claim 1 of the First Auxiliary request does not involve

an inventive step.

5. Second Auxiliary request

5.1 Claim 1 of the Second Auxiliary request is distinguished from D2 by that in the claimed device SiC is used as semiconductor material, that the Schottky contact and the source contact are made of different materials, the latter being in addition annealed, and that the active area of the integral JBS diode is less than the active area of the DMOSFET and the active area of the integral JBS diode relative to the active area of the DMOSFET is selected to flow a full switch current of the DMOSFET at a forward bias voltage of less than or equal to 2.6V.

5.2 The Appellant argued, in a similar way to the previous requests, that the distinguishing features combined to provide a better control of the operation of the claimed device, and in particular, to assure that the JBS diode would turn on before the body diode of the DMOSFET. The last feature of the claim would especially guarantee that by the time the voltage reached 2.6 V - which was the turn-on voltage of the body diode of the DMOSFET - all the switch current would have flown through the JBS diode and the body diode would not turn on at all.

5.3 The Board notes that it was common general knowledge that the JBS diode had a higher current density than the DMOSFET in the SiC device (see also page 12, lines 3-28 of the application) and considers the last features of claim 1 to be inherent in the use of SiC in the manufacture of the claimed semiconductor device (see also lines 11-14 on page 12).

5.4 In D2 it is also stated that the Schottky diode bypassed all current from the body diode, thus, preventing the turning on of the body diode (see column 4, lines 47-51).

5.5 In addition, since claim 1 defines a device, it is not possible to determine whether such features are inherent features to the device or they are implemented by design ("*selected to*"; see claim 1).

5.6 The Appellant did not provide any further arguments regarding this request.

5.7 The Board concludes thus, that the subject matter of claim 1 of the Second Auxiliary request does not involve an inventive step, either.

6. Third and Fourth Auxiliary requests

6.1 Claim 1 of the Third Auxiliary request differs from D2 in that the semiconductor material of the claimed device is SiC instead of Si, that the Schottky and source contacts are made of different materials, the latter being also annealed, and that the active area of the integral JBS diode is less than 50% the active area of the DMOSFET.

Claim 1 of the Fourth Auxiliary request has the same distinguishing features with the difference that the active area of the integral JBS diode is defined to be less than 25% the active area of the DMOSFET.

6.2 Making reference to the description (page 11, lines 10-21 and page 12, lines 7-14), the Appellant argued that the JBS diode sharing the same drift layer with the DMOSFET had a much lower on-resistance. This

allowed the JBS diode to have a smaller active area than the DMOSFET.

6.2.1 The combination of the distinguishing features provided the technical effect of reducing the resistance of the Schottky contact, assuring, thus, that the JBS diode would be turned on before the body diode of the DMOSFET. By selecting the appropriate material for the Schottky contact and by reducing the size of the active area of the JBS diode, the resistance of the Schottky contact was decreased and a more efficient device was, thus, obtained, a device of smaller size and higher recovery (effectively providing a higher switching frequency).

6.2.2 The skilled person starting from D2 and aiming to achieve higher power and higher switching frequency of the semiconductor device would not arrive at the claimed invention in an obvious manner since there were several steps he would have to take that could not be considered common general knowledge.

6.2.3 The Appellant acknowledged that the specific values of less than 50% (Third Auxiliary request) and less than 25% (Fourth Auxiliary request) were not addressing any specific technical problems; they were rather defining the purpose of reducing the active area of the JBS diode with respect to the active area of the DMOSFET as much as possible.

6.3 The Board does not share the Appellant's opinion in this matter.

6.3.1 As already stated in the description passages referred to by the Appellant, the JBS diode having a lower on-resistance than the DMOSFET is an inherent, generally

known feature of such devices. The desire to obtain a device that would be as small as possible and at the same time have the highest possible performance is a permanent one in the manufacture of electronic devices in general and semiconductor devices in particular.

6.3.2 The device in D2 is a DMOSFET at the first place and the integrated JBS diode is an additional element improving its performance. It would, thus, be obvious for the skilled person that the aim would be to limit the relative size of the JBS diode in the device with comparison to the size of the DMOSFET.

6.3.3 Following from the reasoning regarding the previous requests, the Board is of the opinion that once the skilled person would take the obvious decision to replace Si with SiC in the device of Figure 6 of D2, all the other distinguishing features, including those of claim 1 in the Third and Fourth Auxiliary requests, relate either to inherent properties of the materials to be used or to standard features of the DMOSFET and the JBS diode and are, therefore, part of the general common knowledge of the skilled person.

6.4 In the case of the Third and Fourth Auxiliary requests, the fact that the JBS diode has a lower on-resistance than the DMOSFET is an inherent feature of the device, and so is the fact that the JBS diode can have a smaller active area than the DMOSFET. The specific percentages of the active areas of the JBS diode and the DMOSFET defined in the claims do not address any particular technical problem and the Board sees them as more or less arbitrary design choices.

Regarding the selection of the materials for the Schottky and source contacts, reference is made to the

reasoning related to the First Auxiliary request (see point 4 above). The skilled person starting from the device of D2 and aiming to obtain a smaller device of high performance would take all these aspects into account based only on his common general knowledge and arrive at the claimed device in an obvious and straightforward manner.

6.5 The conclusion of the Board is, therefore, that the subject matter of claim 1 of both the Third and the Fourth Auxiliary requests involves no inventive step.

7. Following from the above reasoning, the Board reaches the final conclusion that the subject matter of claim 1 of the Main request as well as of the First, Second, Third and Fourth Auxiliary requests does not involve an inventive step within the meaning of Article 56 EPC 1973 in light of D2 and the skilled person's common general knowledge.

Since none of the requests on file is allowable, the appeal must fail.

Order

For these reasons it is decided that:

The appeal is dismissed.

The Registrar: The Chairman:

S. Sánchez Chiquero G. Eliasson

Decision electronically authenticated