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Datasheet for the decision of 22 July 2014

Case Number: T 1700/13 - 3.4.03

Application Number: 07122898.5

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Language of the proceedings: EN

Title of invention:
Active matrix type display device

Applicant:
LG Display Co., Ltd.

Headword:

Relevant legal provisions:
EPC Art. 123(2)

Keyword:
Amendments - added subject-matter (yes)

Decisions cited:
T 0169/83

Catchword:

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Case Number: T 1700/13 - 3.4.03

D E C I S I O N
of Technical Board of Appeal 3.4.03
of 22 July 2014

Appellant: (Applicant)	LG Display Co., Ltd. 20, Yoido-dong, Youngdungpo-gu, Seoul (KR)
Representative:	Viering, Jentschura & Partner Patent- und Rechtsanwälte Am Brauhaus 8 01099 Dresden (DE)
Decision under appeal:	**Decision of the Examining Division of the European Patent Office posted on 27 February 2013 refusing European patent application No. 07122898.5 pursuant to Article 97(2) EPC.**

Composition of the Board:

Chairman	G. Eliasson
Members:	V. L. P. Frank
	T. Karamanli

Summary of Facts and Submissions

I. This is an appeal against the refusal of European patent application No. 07 122 898 for the reason of added subject-matter (Article 123(2) EPC).

II. The appellant requested in writing that the decision under appeal be set aside and that a patent be granted on the basis of claim 1 filed with the statement of grounds of appeal.

Auxiliarily, oral proceedings were requested.

III. The sole claim of this request reads as follows (emphasis added by the board):

"1. An active matrix type display device comprising:

first to sixth gate lines (GL1-GL6) arranged at one direction;

data lines (DL1-DLm) arranged orthogonally to the first to sixth gate lines (GL1-GL6);

a first red pixel cell (R1) connected to the first gate line (GL1) and the data line (DL1), wherein the first red pixel cell (R1) displays red color;

a first green pixel cell (G1) connected to the second gate line (GL2) and the data line (DL1), wherein the first green pixel cell (G1) displays green color;

a first blue pixel cell (B1) connected to the third gate line (GL3) and the data line (DL1), wherein the first blue pixel cell (B1) displays

blue color;

a second blue pixel cell (B2) connected to the fourth gate line (GL4) and the data line (DL1), wherein the second blue pixel cell (B2) displays blue color;

a second green pixel cell (G2) connected to the fifth gate line (GL5) and the data line (DL1), wherein the second green pixel cell (G2) displays green color; and

a second red pixel cell (R2) connected to the sixth gate line (GL6) and the data line (DL1), wherein the second red pixel cell (R2) displays red color,

wherein the first red pixel cell (R1), the first green pixel cell (G1) and the first blue pixel cell (B1) constitute a first unit pixel (PXL1) for displaying a first unit image;

and the second red pixel cell (R2), the second green pixel cell (G2) and the second blue pixel cell (B2) constitute a second unit pixel (PXL2) for displaying a second unit image;

wherein the first red pixel cell (R1) and the first green pixel cell (G1) are positioned between the first and second gate lines (GL1, GL2);

wherein the first blue pixel cell (Bl) and the second blue pixel cell (B2) are positioned between the third and fourth gate lines (GL3, GL4);

wherein the second green pixel cell (G2) and the

second red pixel cell (R2) are positioned between the fifth and sixth gate lines (GL5, GL6);

wherein a pixel electrode of the first red pixel cell (R1) is positioned closer to the first gate line (GL1) than to the second gate line (GL2), while a pixel electrode of the first green pixel cell (G1) is positioned closer to the second gate line (GL2) than to the first gate line (GL1);

wherein a pixel electrode of the first blue pixel cell (B1) is positioned closer to the third gate line (GL3) than to the fourth gate line (GL4), while a pixel electrode of the second blue pixel cell (B2) is positioned closer to the fourth gate line (GL4) than to the third gate line (GL3);

wherein a pixel electrode of the second green pixel cell (G2) is positioned closer to the fifth gate line (GL5) than to the sixth gate line (GL6), while a pixel electrode of the second red pixel cell (R2) is positioned closer to the sixth gate line (GL6) than to the fifth gate line (GL5)."

IV. The decision of the examining division can be summarized as follows:

- Claim 1 was amended to specify the relative positions of the pixel electrodes with respect to the gate lines, ie the features highlighted in bold in claim 1 (see point III above).

- The applicant argued that the relations between these distances were disclosed in figure 7. Although figure 5 showed the connections of the pixels to the gate lines and to the data lines in

a merely schematic way, figure 7 showed the arrangement of the pixels in a more detailed way, as it also showed the indentations in the pixel electrodes which accommodated the transistors. Hence also the different spacings between the pixel electrodes and the gate lines should be regarded as intentionally disclosed features in that figure.

- The examining division however found that although figure 7 showed different distances between the pixel electrodes and their adjacent gate lines, it was merely a schematic drawing of the connections of the pixel cells to the respective gate lines and to the data line and did not provide any detailed information about the sizes and distances in a real layout of the pixel matrix on a substrate. The data lines, the gate lines and the transistors were only represented by their abstract symbols. Furthermore, although figure 7 showed the pixel arrangement in more detail than figure 5, only the electrical connections were more detailed. From the description, the skilled person learned that the present invention sought to reduce the fabrication cost of the active matrix display, by reducing the number of high-priced data driving integrated circuits, and increasing the number of relatively low-priced gate driving integrated circuits. This object was achieved by connecting two columns of pixels to a single data line and increasing the number of gate lines, as depicted in figure 7. The schematic pixel arrangement of figure 7 was therefore only useful to understand how the different pixels were electrically connected by transistors to the data line and the respective gate lines. This figure

was not intended to show the layout of the active matrix display in terms of the physical sizes and positions of electrodes.

V. The appellant argued essentially as follows:

- The subject-matter of independent claim 1 constituted subject-matter which was unambiguously derivable from the original application documents, since figure 7 was not merely a schematic drawing. Although the figures included graphical symbols for, for example, the connecting lines and the transistors, every single pixel electrode was depicted in its concrete and exact shape with a recess for accommodating the thin film transistor (TFT) between the pixel electrode and the respective gate line to which the pixel electrode was connected by the TFT. Additionally, it was not stated anywhere in the description that the figures were schematic.

- Furthermore, as could be deduced from figure 3, showing another pixel structure, distances between the pixel electrode and the gate line, to which the pixel electrode was connected by a TFT, were smaller than distances between the respective pixel electrode and the gate line, to which the pixel electrode was not connected by the TFT. While figures 2 and 5 showed and paragraphs 33 and 54 talked about *"pixel cells"*, it could be clearly seen that figures 3 and 4 and figures 6 and 7 disclosed *"pixel electrodes"*, as further evidenced by paragraph 39. Thus, it was clear that figures 3, 4, 6 and 7 of the application showed a higher level of detail and structural accuracy than figures 2 and 5, since the former figures showed a

notch in the pixel electrode to allow for placement of other components. This meant, that looking at the application as a whole, it was clear to a person of ordinary skill in the art that the different distances between the pixel electrodes and their adjacent gate lines as shown in figure 7 would not be interpreted as being drawing artifacts of a mere schematic representation of a pixel matrix. Therefore, the arrangement of the electrodes in figure 7 represented the correct relative distances as found in the real layout drawing.

- In summary, the distances between the pixel electrodes and the respective gate lines were not drawing artifacts as interpreted by the examining division, but depicted the proportions necessary to avoid parasitic capacities, even though this relationship might not be mentioned explicitly in the description as originally filed and even though data lines, scan lines, and transistors were represented by their respective graphical symbol.

VI. In the communication annexed to the summons to oral proceedings the board observed that the application disclosed all the figures to be diagrams, making no difference between eg figures 5 and 7 ([0015]-[0022]). A diagram, however, was a graphic design that explained rather than represented something.

VII. With letter dated 5 June 2014 the appellant informed the board that it would not attend the oral proceedings, making no further substantive comments.

VIII. Oral proceedings were held in the absence of the appellant.

Reasons for the Decision

1. The appeal is admissible.

2. Amendments (Article 123(2) EPC)

2.1 The active matrix type display of claim 1 is based on the 2nd embodiment of the invention having, in particular, the specific arrangement of pixels depicted in figure 7 (Figures 5-7; [0053]-[0063] and [0071]-[0072] of the published application).

2.2 The examining division found in the decision under appeal that the following features of claim 1:

(a) *wherein a pixel electrode of the first red pixel cell (R1) is positioned closer to the first gate line (GL1) than to the second gate line (GL2), while a pixel electrode of the first green pixel cell (G1) is positioned closer to the second gate line (GL2) than to the first gate line (GL1);*

(b) *wherein a pixel electrode of the first blue pixel cell (B1) is positioned closer to the third gate line (GL3) than to the fourth gate line (GL4), while a pixel electrode of the second blue pixel cell (B2) is positioned closer to the fourth gate line (GL4) than to the third gate line (GL3);*

(c) *wherein a pixel electrode of the second green pixel cell (G2) is positioned closer to the fifth*

gate line (GL5) than to the sixth gate line (GL6), while a pixel electrode of the second red pixel cell (R2) is positioned closer to the sixth gate line (GL6) than to the fifth gate line (GL5)

were not directly and unambiguously derivable from the application documents as filed.

2.3 The application discloses that conventional display devices require three times more data lines than gate lines, since each unit pixel is formed by a red, a blue and a green pixel ([0004]-[0005]). Hence the production cost of the conventional display device is high, since a higher quantity of the expensive data driving integrated circuits are required than of the less expensive gate driving integrated circuits([0006]-[0008]).

An object of the present invention is thus to reduce the fabrication cost by decreasing the number of relatively high-priced data driving integrated circuits, while increasing the number of relatively low-priced gate driving integrated circuits ([0010], [0075]-[0077]).

This is achieved eg by the structure shown in figure 7, according to a 2nd embodiment of the invention, in which two pixels (eg R1 and G1) share the same data line DL1, while requiring two different gate lines GL1 and GL2 to drive them. Thus for the two unit pixels shown in figure 7, formed respectively by the R1, G1, B1 pixels and the R2, G2, B2 pixels, one data line DL1 and six gate lines GL1-GL6 are required. In contrast, the conventional display device shown in figure 1 would require three data lines and two gate lines to drive two unit pixels.

2.4 The appellant argued that the objected features (a) to (c) concerned the relative positions of the pixel electrodes with respect to the gate lines. Figure 7 depicted every single pixel electrode in its concrete and exact shape with a recess for accommodating the thin film transistor (TFT) between the pixel electrode and the respective gate line to which the pixel electrode was connected by the TFT. While figure 5 showed the pixel cells schematically, figures 6 and 7 disclosed the pixel electrodes. Figures 6 and 7 showed a higher level of detail and structural accuracy than figure 5, since the former figures showed a notch in the pixel electrode to allow for placement of other components. It was thus clear that the different distances between the pixel electrodes and their adjacent gate lines shown in figure 7 were not a drawing artifact of a mere schematic representation of a pixel matrix. The arrangement of the electrodes in figure 7 represented the correct relative distances as found in the real layout drawing.

2.5 It is the established jurisprudence of the boards of appeal that when considering features disclosed solely in the drawings, the structure and function of such features had to be clearly, unmistakably and fully derivable from the drawings by the skilled person and not at odds with the other parts of the disclosure (see eg T 169/83, OJ EPO 1985, 193).

2.6 In the view of the board the skilled person when reading the present application would have considered the arrangement of the data and gate lines and their respective connections to the pixels to be the teaching of the invention. The application in particular gives no indications that the relative distances between the

pixel electrodes and the data or gate lines play any role for the present invention, since they do not influence the number of data or gate lines, increasing or decreasing them. Thus, although the pixels are shown in figure 7 as being slightly closer to the respective gate line to which they are connected, the skilled person would not consider this fact as significant, much less as a specific teaching that should be taken into account, but would have disregarded it as a drawing artifact. Furthermore, the drawings are all stated in the application to be *"a diagram illustrating"* either the prior art or the inventive embodiments. A diagram, however, is a graphic design that explains rather than represents something. There are thus no reasons to consider that eg figures 5 and 7 are anything else than a schematic illustration of the inventive concept to reduce the number of data lines while increasing the number of gate lines or that these figures are of a different character, ie that figure 7 is a more real representation of the pixel matrix structure than figure 5.

2.7 The board agrees with the finding in the decision under appeal that the features (a) to (c) of claim 1 mentioned above are not directly and unambiguously derivable from the application as filed taken as a whole.

2.8 Hence the application does not comply with the requirements of Article 123(2) EPC.

Order

For these reasons it is decided that:

The appeal is dismissed.

The Registrar: The Chairman:

S. Sánchez Chiquero G. Eliasson

Decision electronically authenticated