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Datasheet for the decision of 28 June 2018

Case Number: T 1565/13 - 3.4.03

Application Number: 05026110.6

Publication Number: 1715472

IPC: G09G3/32

Language of the proceedings: EN

Title of invention:
Display device and method of driving the same

Applicant:
LG Display Co., Ltd.

Headword:

Relevant legal provisions:
EPC 1973 Art. 56

Keyword:
Inventive step - (no)

Decisions cited:

Catchword:

Europäisches Patentamt
European Patent Office
Office européen des brevets

Beschwerdekammern

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Case Number: T 1565/13 - 3.4.03

D E C I S I O N
of Technical Board of Appeal 3.4.03
of 28 June 2018

Appellant: (Applicant)	LG Display Co., Ltd. 20, Yoido-dong, Youngdungpo-gu, Seoul (KR)
Representative:	Ter Meer Steinmeister & Partner Patentanwälte mbB Nymphenburger Straße 4 80335 München (DE)
Decision under appeal:	**Decision of the Examining Division of the European Patent Office posted on 14 March 2013 refusing European patent application No. 05026110.6 pursuant to Article 97(2) EPC.**

Composition of the Board:

Chairman	G. Eliasson
Members:	M. Stenger
	C. Schmidt

Summary of Facts and Submissions

I. The appeal concerns the decision of the Examining Division to refuse European patent application No. 05026110. The Examining Division found neither the main request nor any of auxiliary requests 1 to 6 allowable, raising objections relating to Articles 56 with JP 2000 347628 (D1) as closest prior art and 123(2) EPC.

II. At the end of the oral proceedings before the Board, the appellant requested the grant of a patent according to a main request and auxiliary requests 1 to 5, all filed with the grounds of appeal.

III. The following documents will be referred to in the present decision:
D1: JP 2000 347628 A
D3: US 2005/078066 A1
D4: US 6 323 871 B1

IV. Claim 1 of the main request has the following wording (labeling A), B), ... added by the Board):

An organic light emitting display (OLED) device comprising:
A) *a display panel (410) having a plurality of pixels (414),*
A1) *each of the plurality of pixels having R, G and B subpixels (22)*
A2) *arranged in intersections between a plurality of data lines (DL1-DLm/3) extending in a vertical direction and a plurality of scan lines (SL1-3SLn) extending in a horizontal direction,*
A3) *each subpixel having one of a plurality of thin film transistors (T1) formed at intersections,*

B) *a first and a second scan driver (442, 444) disposed on opposite sides of the display panel (410) to drive the plurality of scan lines (SLI-3SLn) by means of a plurality of circuit parts (446, 447) included in the first and second scan drivers (442, 444), each circuit part (446, 447) being arranged to drive one of the scan lines (SLI-3SLn); and*
C) *a data driver (430) adapted to drive the plurality of data lines (DL1-DLm/3),*
D) *wherein each of the plurality of pixels (414) has a vertical stripe form, in which the R, G and B subpixels are arranged in the vertical direction,*
E) *and wherein a height (C) of each circuit part (446, 447) in the vertical direction is equal to that of two subpixels adjacent in the vertical direction.*

V. Claim 1 of auxiliary request 1 differs from claim 1 of the main request by the following additional features (labeling F), G), ... added by the Board):

F) *wherein a first circuit part (446, 447) of the first and second scan drivers (442, 444) is arranged adjacent to a first and second subpixel (R, G) of three subpixels of first pixels (414), respectively, the subpixels being aligned along the data line,*
and
G) *wherein an adjacent second circuit part of the first and second scan drivers (442, 444) is arranged adjacent to the third subpixel (B) of the first pixels and to the next first subpixel (R) of second pixels being arranged below the first pixels along the data line, respectively;*
and
H) *wherein adjacent odd scan lines are connected to adjacent circuit parts (446) of the first scan driver (442) and adjacent even scan lines are connected to*

adjacent circuit parts (447) of the second scan driver (444).

VI. Claim 1 of auxiliary request 2 differs from claim 1 of the main request by additional feature H) and the following additional feature (labeling I) added by the Board):

I) *wherein the plurality of circuit parts (446) of the first scan driver (442) are connected to the plurality of circuit parts (447) of the second scan driver (444) through corresponding scan lines, in order to use output signals of the first scan driver (442) as input signals of the second scan driver (444) and output signals of the second scan driver (444) as input signals of the first scan driver (442); and*

VII. Claim 1 of auxiliary request 3 differs from claim 1 of the main request by additional feature H) and the following additional feature (labeling J) added by the Board):

J) *wherein each subpixel includes a light emitting device (OLED) connected between a power supply voltage (VDD) and a ground voltage (GND) and a driving circuit (130) for driving the light emitting device (OLED) in response to a driving signal supplied from the data line and the scan line, the driving circuit (130) including a drive TFT DT, a first switching TFT T1, a second switching TFT T2, a conversion TFT MT, and a storage capacitor Cst, wherein the gates of the first switching TFT Tl and the second switching TFT T2 are commonly connected to the scan line, and*

VIII. Claim 1 of auxiliary request 4 differs from claim 1 of the main request by additional feature H), modified

features A2'), D') and E') replacing features A2), D) and E), respectively, and the additional feature K) as follows (labeling A2'), D'), ... added by the Board):

A2') *arranged in intersections between a plurality of data lines (DL1-DLm/3) and a plurality of scan lines (SL1-3SLn),*

D') *wherein each of the plurality of pixels (414) has a vertical stripe form, in which the R, G and B subpixels are arranged along a data line with their longitudinal orientation parallel to the scan lines,*

E') *wherein a height (C) of each circuit part (446, 447) in the direction parallel to the data line is equal to that of two adjacent subpixels in the same direction,*

K) *wherein thin film transistors connected to the odd scan lines are turned on/off in response to output signals of circuit parts of the first scan driver and thin film transistors connected to even scan lines are turned on/off in response to output signals of circuit parts of the second scan driver; and*

IX. Claim 1 of auxiliary request 5 differs from claim 1 of the main request by an additional feature corresponding in substance to feature K) and the following additional feature (labeling L) added by the Board):

L) *wherein the height (C) of each circuit part is smaller than the longitudinal extension of the circuit part.*

X. The arguments of the appellant with respect to which document was to be regarded as closest prior art, as

far as they are relevant to the present decision, may be summarised as follows:

D4 disclosed a colour display with gate drivers arranged on both sides of the panel. It would thus be more suitable as closest prior art than D3 or D1. Starting from D4, the skilled person would then try to solve the objective technical problem of reducing the bezel/rim size of the colour display. This corresponded to the original problem to be solved by the application.

XI. The arguments of the appellant with respect to whether features E), F), G) and L) were disclosed in D3 or not, as far as they are relevant to the present decision, may be summarised as follows:

Although D3 disclosed in [66] and figure 6 circuit parts which, compared to a conventional display, extended further in the vertical direction and were arranged roughly adjacent to the gate lines, D3 did not disclose that the circuit part had a height exactly equal to the height of two subpixels as defined in feature E) and was smaller than the longitudinal extension of the circuit part as defined in feature L), and as shown in figures 3 and 4 of the application. Further, D3 did not disclose particular circuit parts arranged, respectively, adjacent to two subpixels as defined in features F) and G) and as also shown in figures 3 and 4 of the application.

XII. The arguments of the appellant with respect to inventive step starting from document D3, as far as they are relevant to the present decision, may be summarised as follows:

(a) Features A1) and D), D4

(i) Document D4 related essentially to liquid crystal displays (LCDs). The requirements of LCDs and OLEDs were quite different, so that the skilled person would not implement the teaching of D4 in an OLED display (see also grounds for appeal, page 5, penultimate paragraph to page 6, third paragraph).

(ii) If one assumed that the distinguishing features of claim 1, starting from D3, were features A1) and D), then the technical effect of these distinguishing features was that colour could be displayed. The objective technical problem to be solved could then be formulated as how to provide a colour display while keeping the small bezel/rim around the panel. This corresponded to the problem stated in the application. In contrast, D3 did not mention the manufacturing cost or power consumption of the display at all.

(iii) The arrangement of D4 implied more gate drivers than the conventional (horizontal) subpixel arrangement, leading to an increased width of the layout area. This contradicted the aim of D3 expressed in [14] and [15] to maximise the display area with respect to the overall panel area.

(iv) D4 used conventional, discrete chips for implementing the drivers, whereas D3 employed circuits integrated into the panel, i.e. a completely different driver structure.

(v) The different driver structures would in addition require an adaptation of the data structure.

For each of these reasons, the skilled person would not turn to D4 when, starting from D3, trying to solve the above-mentioned objective technical problem.

(b) Feature I), D1

(i) The skilled person would not get any hint in D3 to connect the first scan driver to the second scan driver through scan lines and using the output of the first scan driver as an input for the second scan driver as defined in feature I), since D3 neither disclosed how the scan drivers were controlled nor how the signals were provided to the scan lines. The same held for D4.

(ii) D1 did not relate exclusively to the problem of saving space as D3, but also to the problem of simplifying the signal structure. The skilled person would thus not consult D1 when starting from D3.

(iii) Even if the skilled person consulted D1, he would not consider to implement the control system of D1 in the display of D3, because he would already have to modify the data structure of the scan signals in order to integrate features A1) and D) into the display of D3. He would then not consider any modification that would require an additional adaptation of the gate signal data structure.

Reasons for the Decision

1. Closest state of the art

1.1 The application relates to a matrix colour OLED display with a scan or gate driver and a data or source driver. The aim of the application is to minimise the layout area of the scan driver (see [2]). This is achieved by arranging first and second scan drivers on opposite sides of the display panel (see [22] and [23]) and further by adapting the height and width of the scan driving circuit parts (see [39] to [41]).

1.2 Document D1 concerns a matrix display and aims at providing a large display area in comparison to the area needed for the driver (see [8] to [12] and [15]). D1 discloses an arrangement of two scan drivers on opposite sides of a panel. In [11], D1 further mentions that the display can be an organic electroluminescence display. Thus, D1 aims at solving the same problem as and shares many features with the application.
D1, which was used in the contested decision as the closest state of the art, can thus be regarded as a suitable starting point for the problem solution approach.

1.3 Document D3 discloses an OLED matrix display with a maximised picture area on a given panel size, achieved by arranging two gate or scan drivers on opposite sides of the panel (see abstract). In addition to what is disclosed in D1, D3 explicitly discusses the height and width of the scan driver circuits ([66] to [68]) and discloses the diagram of an electronic circuit used to control the individual OLED pixels (figure 5).
In view of features E) (all requests) and J) (auxiliary request 2), D3 is thus considered by the Board to be

even more suitable as starting point for the purpose of the problem solution approach than D1.

1.4 Document D4 concerns a matrix display with scan driver circuit parts Gd1 to Gd6 being arranged on opposite sides of the panel. This is similar to the arrangement of the application.
As argued by the applicant (see section X. above), D4 explicitly relates to a colour display and discloses a vertical stripe arrangement of R, G, B subpixels as required by features A1) and D), while D1 and D3 do not mention colour at all.
On the other hand, D4 does not mention the height and width of the scan drivers at all. Furthermore, the scan drivers and data drivers in D4 are implemented in form of discrete chips mounted on the display, whereas in the claimed device and in D3, the drivers are integrated in the display. Hence, D4 does not disclose more features of the application than D3. Further, D4 aims at reducing manufacturing cost and power consumption of the display while maintaining the image quality (column 2, lines 22 to 59). Thus, contrary to D1 and D3, D4 aims at solving a different problem than that addressed by the application.
The Board therefore concludes that D4 is a less suitable starting point for the problem solution approach than D1 and D3. This holds for all requests on file.

1.5 It follows from the above that document D3 is to be considered as representing the closest state of the art for the problem-solution approach.

2. Main request

2.1 Document D3 discloses:

An organic light emitting display device ([7]) *comprising:*
A) *a display panel* (electro-luminescence display part, see [18]) *having a plurality of pixels* (figures 3, 7 and 8),
A2) *arranged in intersections between a plurality of data lines* (DL) *extending in a vertical direction and a plurality of scan lines* (GL1, GL2, Gl3,...) *extending in a horizontal direction* (figures 3, 7 and 8),
A3) *each (sub)pixel having one of a plurality of thin film transistors* (DT, MT, ST1, ST2) *formed at intersections* (figure 5 and [57] to [60]),
B) *a first and a second scan driver* 122a, 122b (first gate driver, second gate driver, see [18]) *disposed on opposite sides of the display panel* (electro-luminescence display part) *to drive the plurality of scan lines* (GL1, GL2, GL3, ...) *by means of a plurality of circuit parts* 123 (plurality of gate shift registers) *included in the first and second scan drivers, each circuit part* 123 *being arranged to drive one of the scan lines* (GL1, GL2, GL3, ..., see [66] and figure 5)*; and*
C) *a data driver 124 adapted to drive the plurality of data lines* (DL, [69]).

This was not disputed by the appellant. However, the appellant argued that D3 did not disclose the height of the circuit parts as defined in feature E) and as shown in figures 3 and 4 of the application (see section XI. above).

The Board accepts that the blocks representing the gate shift registers 123 in figure 6 of D3 are indicated as having a certain vertical distance to each other and thus a height which seems to be just a bit more than

the vertical distance between two gate lines, whereas the blocks representing the circuit parts in figures 3 and 4 of the application are indicated as having essentially the same height as the distance between three gate lines, corresponding to the height of two subpixels.

However, both in D3 and in the application, abstract blocks in the form of simple rectangles are used to represent the circuit parts; there is no indication in the application or in D3 that these rectangles have been drawn to scale.
Further, neither D3 nor the application disclose any details concerning the arrangement of the electronic elements making up these circuit parts. In that respect, the Board notes that it is not possible that the whole area of such a circuit part can be covered by electronic elements like integrated circuits, discrete elements and/or wiring. On the contrary, it is inevitable that certain distances between the individual elements of each circuit part are provided, for example to avoid short-circuits and/or crosstalk between such elements. For the same reasons, certain distances between (adjacent elements of) adjacent circuit parts have to be respected.
Therefore, the rectangles used to represent the circuit parts in the application as well as the rectangles used to represent the corresponding gate shift registers in D3 can at best be interpreted as giving a rough estimation of (the proportions of) the area actually covered by the electronic components making up the circuit parts.

Further, the Board notes that D3 discloses in [66] and [67] that compared to the prior art, the area of a gate shift register 123 is kept constant, while its width is

reduced by half (see [66]: *an area of a region at which each of the plurality of gate shift registers 123 is provided is equal to the gate shift registers in the prior art*; see [67]: *a width of the first gate driver 122a is reduced to a half of the width of the conventional gate driver*).
This reduction by half is exactly what is achieved by the application as well (see penultimate sentence of [40]).

The Board thus concludes that D3 discloses feature E) to the same extent as the application itself.

2.2 Distinguishing features
In view of the above, the subject-matter of claim 1 of the main request differs from D3 by features A1) and D).

2.3 Inventive step

2.3.1 Technical effect
The technical effect of these distinguishing features is that a colour display is provided which, compared to a horizontal arrangement of the subpixels, needs less data lines but more scan lines.

2.3.2 Objective problem to be solved.
Providing R, G and B pixels is the standard manner in which colour displays are provided. The skilled person would thus readily assign respective ones of these basic colours to each of the pixels shown in D3. He would thereby implement feature A1) when starting from D3 and trying to provide a colour display.
He would then have to find a geometrical arrangement for the (sub)pixels of the basic colours.

The Board accepts that manufacturing cost and power consumption are not mentioned explicitly in D3, as argued by the appellant (see section XII(a)(ii) above). However, these are issues that play an important role in any technical system. Thus, the skilled person will always take them into account when designing a display (or any other technical system).

The objective technical problem to be solved starting from D3 can thus be formulated as being how to provide a colour display such that it is cost-effective and does not consume too much power.

2.3.3 D4

As mentioned before, document D4 relates to a matrix display with a scan driver arrangement similar to the one of the application.
Moreover, D4 (see column 2, lines 40 to 44) aims at solving the objective technical problem as defined above.

The Board appreciates that document D4 relates essentially to liquid crystal displays (LCDs), as argued by the appellant (see section XII(a)(i) above) and that the manner in which the individual pixels of LCDs are controlled differs from the manner in which the individual pixels of electroluminescent displays are controlled.
However, the logic and the electronics governing *when which pixel of a matrix is controlled* are the same in LCDs and electroluminescence displays. D4 further explicitly mentions the applicability to electroluminescent displays in matrix form (*EL display*, see column 12, lines 3 to 12).

The skilled person would thus consult D4 when trying to solve the above-mentioned objective technical problem.

To solve the objective technical problem posed, D4 suggests to arrange pixels of the basic colours R, G and B such that each of these basic colours is addressed by one scanning line G (see figures 1 and 2). In the terminology of the application, that corresponds to a vertical stripe form of the R, G and B pixels and thus to features A1) and D).

The skilled person would therefore be led by the teaching of D4 to integrate features A1) and D) into the display disclosed in D3.

2.3.4 Further arguments of the appellant (see section XII (a))

(a) The appellant argued that more scan drivers would require more space for the corresponding circuitry (see section XII(a)(iii) above).

However, as acknowledged by the appellant, in technical areas such as displays, a large number of parameters have to be optimised at the same time and it is a common situation that certain of these parameters can be optimised only at the expense of one or more of the others. The skilled person would thus regard the increase in area necessary for the scan driver circuitry as a simple trade-off for the improvements in cost-effectiveness and power consumption and would make his choice according to the circumstances.

(b) As pointed out by the appellant, D3 discloses drivers integrated on the panel, while the drivers

according to D4 are separate chips connected to the panel. Thus, D3 and D4 disclose different drivers (see section XII(a)(iv) above) in the sense that they are manufactured by different processes.

However, the functions of the different drivers are the same in both documents. Hence, the Board finds that D4 does not teach the skilled person to replace the integrated drivers of D3 by the discrete chip drivers of D4, but only to change the *number* of gate drivers and the *number* of data drivers used in D3.

Furthermore, data/source drivers will always be more complex than scan/gate drivers, irrespective of whether these drivers are realised in thin film technology or by means of conventional semiconductor manufacturing processes. Thus, the advantages in terms of cost-effectiveness and power consumption obtained by having a large number of scan drivers and a small number of source drivers are independent of the manufacturing method of the drivers.
Thus, the different technology used to manufacture the drivers would not dissuade the skilled person from using the teaching of D4 in the display of D3.

(c) The Board does not agree with the appellant that the data structure has to be adapted when changing from drivers produced by one process to drivers produced by a different process (see section XII(a)(v) above), as long as their *functions* are the same.
The Board accepts, however, that the structure of the data sent to the gate drivers and the source drivers has to be adapted to the *number* of scan

lines and to the *number* of data lines. The Board further notes that D4 also teaches in detail which data input format to employ (see, e.g., column 8, lines 9 to 26 and column 8, lines 62 to column 9, line 2).

2.4 Conclusion

In view of the above, the skilled person would consider D4 when trying to solve the above-mentioned objective technical problem starting from D3. He would then be led by the teaching of D4 to integrate features A1) and D) into the display disclosed in D3, thereby arriving at the subject-matter of claim 1 without the exercise of an inventive step according to Article 56 EPC 1973.

3. Auxiliary request 1

Additional feature H) is disclosed in D3 as well, see figure 6 in combination with figure 3. This was not disputed by the appellant.

The appellant submitted (see section XI), however, that D3 did not disclose the exact arrangement of particular circuit parts adjacent to specific two subpixels according to features F) and G).

As mentioned before with respect to feature E), the rectangles/blocks shown in figure 6 of D3 and figures 3 and 4 of the application are considered to give only a *rough estimation* of the (proportions of the) area of the gate shift register/circuit parts. This applies also to the geometrical arrangement adjacent to the gate lines/(sub)pixels. Thus, features F) and G) are disclosed in D3 to the same extent as in the application.

Therefore, the additional features of claim 1 of auxiliary request 1 are all disclosed in the document D3 as well. Consequently, the argumentation concerning lack of inventive step of claim 1 of the main request applies to claim 1 of auxiliary request 1 as well and the subject-matter of this claim lacks an inventive step according to Article 56 EPC 1973.

4. Auxiliary request 2

Additional feature H) is disclosed in D3 as well, as mentioned above, and thus cannot contribute to the acknowledgement of an inventive step.

Additional feature I), on the other hand, is not disclosed in D3, which, like D4, does not mention any details concerning how the signals are transmitted to and through the scan lines. This was pointed out by the appellant (see section XII (b)(i) above).

Thus, when implementing a display according to D3 taking into account the teaching of D4, the skilled person would further have to find a solution for transmitting the scan signals. This technical problem is hence different from the technical problem addressed by the previous requests.

D1 relates to a matrix display that can be an organic electroluminescent display (see [11]) and aims at solving the same problem as D3, i.e., increasing the display area for a given panel size (see [15]). This is achieved, as in D3, by providing a scan driver on both sides of a panel (see figures 1 to 3).
D1 thus discloses a similar structural arrangement and is directed to the same basic problem as D3.

Therefore the skilled person would consult D1 when looking for a solution for transmitting the scan signals.

Concerning the argument of the appellant that D1 was further directed to the problem of simplifying the signal structure (see section XII(b)(ii) above), the Board notes that this would give the skilled person an additional reason to consult D1 when looking for a solution for transmitting the scan signals.

In D1, the scan signals are transmitted to and through the scan lines in the same zig-zag manner as defined by feature I) (see figure 3). According to D1, this has the advantage that the area necessary for the scan drivers can be further reduced because less wiring is needed and output buffers can be dispensed with (see [10]).

Concerning the argument that the skilled person would not want to adapt the data structure twice, i.e., once when combining D3 and D4 and once when integrating the teaching of D1 (see section XII(b)(iii) above), the Board accepts that any specific way of transmitting the scan line signal will inevitably require a corresponding adaptation of the scan line signal structure.
However, D1 discloses how to do that as well (see figure 4 in combination with [59]ff.).

The skilled person would thus be incited to further implement feature I) and would thereby arrive at the subject-matter of claim 1 of auxiliary request 2 without the exercise of an inventive step according to Article 56 EPC 1973 in view of document D3 combined with documents D4 and D1.

5. Auxiliary request 3

D3 also discloses feature H) as mentioned above. Further, additional feature J) which is based on figure 4 and [51] to [55] of the application corresponds to the circuitry shown in figure 5 of D3. This was not disputed by the appellant.

Since the additional features of claim 1 of auxiliary request 3 are equally disclosed in the closest prior art document D3, the subject-matter of claim 1 of auxiliary request 3 lacks an inventive step according to Article 56 EPC 1973 in view of D3 combined with the teaching of D4.

6. Auxiliary request 4

The amendments of features A2'), D') and E') as compared to features A2), D) and E) amount on the one hand to

i) a replacement of the definition of the direction in which the subpixels are arranged (along/parallel a data line instead of vertical),

and on the other hand to

ii) the feature that the longitudinal orientation of the subpixels is parallel to the scan lines.

However, both the direction of arrangement and the orientation of the subpixels are disclosed in D4 as well (see figure 2).

Further, additional feature K) is disclosed in both D3 (see figure 3) and D4 (see figure 1). This was not disputed by the appellant.

As a consequence, the subject-matter of claim 1 of auxiliary request 4 lacks an inventive step according

to Article 56 EPC 1973 for the same reasons as for the main request.

7. Auxiliary request 5
Additional feature K) is, as mentioned above, disclosed in both D3 and D4. Further, additional feature L) is disclosed in D3 (see figure 6) to the same extent as in the present application (see also section 2.1 above).

Consequently, the subject-matter of claim 1 of auxiliary request 5 also lacks an inventive step according to Article 56 EPC 1973 for the same reasons as for the main request.

8. It follows from the above that none of the requests fulfills the requirements of Article 56 EPC 1973. Thus, the appeal must fail.

It is therefore not necessary to discuss compliance of the requests with other Articles of the EPC.

Order

For these reasons it is decided that:

The appeal is dismissed.

The Registrar: The Chairman:

S. Sánchez Chiquero G. Eliasson

Decision electronically authenticated