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Datasheet for the decision of 16 January 2020

Case Number: T 1435/13 - 3.5.01

Application Number: 07872357.4

Publication Number: 2092431

IPC: G06F13/24

Language of the proceedings: EN

Title of invention:
INTERRUPT CONTROLLER

Applicant:
Microchip Technology Incorporated

Headword:
Interrupt controller/MICROCHIP

Relevant legal provisions:
EPC Art. 56, 123(2)
EPC R. 103(1)(a)

Keyword:
Inventive step - adding a conventional group interrupt controller to one using coalescing (no - routine design) - adding additional group interrupt controllers using coalescing with different time windows (yes - not obvious over D1)

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Case Number: T 1435/13 - 3.5.01

D E C I S I O N
of Technical Board of Appeal 3.5.01
of 16 January 2020

Appellant: (Applicant)	Microchip Technology Incorporated 2355 West Chandler Boulevard Chandler, AZ 85224-6199 (US)
Representative:	sgb europe Lechnerstraße 25a 82067 Ebenhausen (DE)
Decision under appeal:	**Decision of the Examining Division of the European Patent Office posted on 25 January 2013 refusing European patent application No. 07872357.4 pursuant to Article 97(2) EPC.**

Composition of the Board:

Chairman	W. Chandler
Members:	A. Wahrenberg
	Y. Podbielski

Summary of Facts and Submissions

I. This is an appeal by the applicant (appellant) against the decision of the examining division to refuse the European patent application No. 07872357.4 on the grounds of added subject-matter for the main request and lack of inventive step for the auxiliary request. The objection of lack of inventive step was based on the combination of the teachings of D5 (INTEL: "8259A PROGRAMMABLE INTERRUPT CONTROLLER (8259A/8259A-2)", DATASHEET INTEL, vol. doc. 8259A, 1 December 1988), and D1 (WO 00/36519 A).

The decision also mentioned documents D2 (WO 02/41153 A), D3 (US 5 905 913 A), and D4 (US 6 115 779 A), but no objection was raised based on those documents.

II. In the statement of grounds of appeal, the appellant requested that the decision of the examining division be set aside and that a patent be granted on the basis of the refused main or auxiliary request. The appellant also requested reimbursement of the appeal fee for reasons of a substantial procedural violation in the proceedings before the examining division.

III. In the communication accompanying the summons to oral proceedings, the Board considered that, whether or not the main request contained added subject-matter, it was not allowable for lack of inventive step over D1. The subject-matter claimed in the auxiliary request seemed to involve an inventive step over D5 in combination with D1, but there was a problem of added subject-matter (Article 123(2) EPC).

IV. In a reply to the Board's communication dated 12 December 2019, the appellant filed a new main request based on the previous auxiliary request. The requests previously on file were withdrawn.

V. During oral proceedings before the Board on 16 January 2020, the appellant filed a new auxiliary request and an amended description. The appellant's final requests were that the decision under appeal be set aside and that a patent be granted on the basis of the main request filed with letter dated 12 December 2019 or on the basis of the auxiliary request filed during the oral proceedings before the Board. The appellant maintained the request for reimbursement of the appeal fee.

VI. Claim 1 of the main request reads:

An interrupt controller comprising:

a first group interrupt controller (100a) to which first interrupt sources are assigned, comprising:

a group interrupt register unit (120) receiving a plurality of interrupt source signals from said first interrupt sources;

an interrupt detector (130) coupled to the group interrupt register unit (120);

a counter unit coupled to the interrupt detector (130), wherein on the first occurrence of any received interrupt source signal the counter unit (130) defines a time window during which the interrupt register stores further interrupt source signals; and

a group interrupt request unit (170) coupled to the counter unit for generating a first group interrupt request signal;

a second group interrupt controller (100b) to which second interrupt sources are assigned and generating a second group interrupt request signal whenever it occurs;

a group interrupt arbiter (210) receiving the group interrupt signals from the plurality of interrupt group controllers (100a, 100b, l00n); and

an interrupt request unit (220) coupled to the group interrupt arbiter (210) for generating an interrupt request signal.

VII. Claim 1 of the auxiliary request reads:

An interrupt controller comprising:

a plurality of group interrupt controllers (100a, 100b,...100n), the plurality of group interrupt controllers (100a, 100b,...100n) comprising

a plurality of first group interrupt controllers, wherein a plurality of first interrupt sources is assigned to each of the plurality of first group interrupt controllers, and wherein each of the plurality of first group interrupt controllers comprises:

a group interrupt register unit (120) receiving a plurality of interrupt source signals from said first interrupt sources;

an interrupt detector (130) coupled to the group interrupt register unit (120);

a counter unit coupled to the interrupt detector (130), wherein on the first occurrence of any received interrupt source signal the counter unit, depending on a latency value assigned for the first group interrupt controller, defines a time window during which the interrupt register stores further interrupt source signals; and

a group interrupt request unit (170) coupled to the counter unit for generating a first group interrupt request signal after expiration of the time window;

a group interrupt arbiter (210) receiving the group interrupt signals from the plurality of interrupt group controllers (100a, 100b,...100n); and

an interrupt request unit (220) coupled to the group interrupt arbiter (210) for generating an interrupt request signal.

VIII. Claim 8 of the auxiliary request reads:

A method for handling a plurality of interrupts comprising the steps of:

assigning interrupt source signals to each of a plurality of group interrupt controllers (100a, 100b,...100n), the plurality of group interrupt controllers 100a, 100b,...100n) comprising a plurality of first group interrupt controllers;

for each of the plurality of first group interrupt controllers, performing the steps of:

receiving a first interrupt source signal;

storing the first interrupt source signal;

depending on a latency value assigned for the first group interrupt controller, defining a time window upon receipt of any of the first interrupt source signal;

storing any further interrupt source signals occurring during the time window; and

generating a first group interrupt signal after expiration of the time window;

arbitrating any group interrupt signal from the plurality of group interrupt controllers (100a, 100b,...100n); and

generating an interrupt request.

Reasons for the Decision

1. *Background*

The invention concerns an interrupt controller comprising a plurality of "group interrupt controllers" (100a, 100b, ...100n in Figure 3 of the published application), each capable of handling a plurality of interrupt sources.

Among the plurality of group interrupt controllers, there is a first type that uses coalescing. Interrupt coalescing essentially means that interrupts are held

off until some condition is reached (in this case the expiration of a time window). Coalescing can thus reduce the number of times the processor is interrupted.

Figures 1 and 2 show examples of the first type of group interrupt controller. This has an interrupt register unit (120), an interrupt detector (130), and a counter unit. The counter unit comprises either a counter (150) and a time out circuit (160), or a counter (150) and a comparator (210) in Figures 1 and 2, respectively. Upon the first occurrence of an interrupt from one of the interrupt sources, the counter starts counting until the expiration of the time window.

Interrupt coalescing causes latency. To deal with high priority interrupts, there is a second type of group interrupt controller without a counter unit that issues the interrupt request to the CPU whenever an interrupt occurs from one of the sources.

The outputs from the plurality of group interrupt controllers are arbitrated by an arbiter (210), and the output from the arbiter is, in turn, forwarded to the CPU by an "interrupt request unit" (220).

2. *Main request*

2.1 Claim 1 of the main request is directed to an embodiment of the invention comprising one group interrupt controller of the first type and one group interrupt controller of the second type. In other words, there is one group interrupt controller using coalescing and one conventional interrupt controller

without coalescing.

2.2 The examining division considered that essentially this subject-matter lacked an inventive step over D5 in combination with D1.

2.3 D5 discloses, in Figure 11, a cascaded arrangement of interrupt controllers (SLAVE A, SLAVE B), each capable of handling interrupt requests from eight sources. The interrupt requests have different priorities, so each interrupt controller has a priority resolver (Figure 1) for determining which of the plurality of interrupts to be issued as output (INT).

A further interrupt controller (MASTER) receives the outputs (INT) and prioritises them just like the other source signals.

2.4 Thus, slaves A and B in D5 are "group interrupt controllers" in the sense of claim 1, and the master serves as both the "arbiter" and the "group interrupt request unit".

2.5 The difference between the arrangement in D5 and the invention in claim 1 is that one of the group interrupt controllers uses coalescing.

2.6 The examining division formulated the technical problem to be solved by the invention as "How to implement interrupt coalescing for some interrupt sources" (point 12.3 of the decision). In the Board's view, this problem is based on hindsight, because coalescing is part of the technical solution to the problem of handling interrupts efficiently. Instead, the Board considers that the correctly formulated problem is how to efficiently handle interrupts of different

priorities.

2.7 Although coalescing was known *per se*, the Board judges that the skilled person would not have considered using it in one of the group interrupt controllers (slaves) in D5, in particular since each slave in the cascaded arrangement deals with interrupts of different priorities. That rather speaks against coalescing those interrupts. Thus, in the Board's view, it would not have been obvious, starting from D5, to provide an arrangement comprising a group interrupt controller using coalescing and a conventional group interrupt controller, as in claim 1 of the main request.

2.8 However, starting from D1, the Board reaches a different conclusion, namely that the subject-matter of claim 1 of the main request lacks an inventive step (Article 56 EPC).

2.9 It is undisputed that D1 discloses the first group interrupt controller using coalescing in claim 1. In D1 (see the abstract), a number of interrupts specified by a variable bundle size are bundled together so as to produce a single interrupt for a plurality of events. There is also a timer. An interrupt is triggered if the timer times out before the bundle is filled.

2.10 Thus, the subject-matter of claim 1 of the main request differs from D1 by the addition of a second, conventional group interrupt controller and an arbiter that arbitrates the output from the two group interrupt controllers.

2.11 The appellant argued that the interrupt controller in claim 1 of the main request had the advantage that it could handle interrupts of different priorities.

Coalescing was used only for low priority interrupts whereas high priority interrupts were issued whenever they were received. Thus, the subject-matter of claim 1 of the main request solved the technical problem of how to efficiently handle interrupts of different priorities. Starting from D1, the skilled person would not have added a second interrupt controller to deal with high priority interrupts, because there was simply no motivation to do so. The skilled person, starting from D1, and looking to solve the problem of efficiently dealing with interrupts of different priorities would rather have looked for a solution within the framework of coalescing, for example by adapting the bundle size.

2.12 The Board does not agree.

In D1, interrupt coalescing is described against the background of conventional interrupt controllers that issue the interrupts immediately. D1 teaches that coalescing might be efficient in that it decreases the number of times that the processor is interrupted. It does not teach the skilled person that interrupt coalescing is the only way and that conventional interrupt controllers are never to be used. Conventional interrupt controllers thus remain part of the building blocks available to the skilled person.

Furthermore, the purpose of the variable bundle size in D1 is to increase the efficiency of coalescing in the sense of filling the bundle as much as possible within the available time window (page 3, lines 14 to 17). It has nothing to do with the priority of interrupts. Therefore, the Board does not agree that the skilled person would be led to adapt the bundle size in order

to deal with interrupts of different priorities.

Starting from D1 that deals with interrupt coalescing, the problem to be solved is, in the Board's view, reducing the latency of high priority interrupts. In order to solve that problem, it would have been obvious for the skilled person to add a second, conventional interrupt controller for dealing with high priority interrupts. Whenever there are two or more outputs, arbitration is necessary. Therefore, the skilled person would also add an arbiter.

2.13 For these reasons, the Board judges that the skilled person would have arrived at the subject-matter of claim 1 of the main request without inventive activity. Therefore, the main request is unallowable for lack of inventive step (Article 56 EPC).

3. *Auxiliary request*

3.1 In claim 1 of the auxiliary request, the plurality of group interrupt controllers comprises a plurality of group interrupt controllers of the first type, i.e. the type using coalescing. Claim 1 of the auxiliary request furthermore specifies that the time window is defined depending on a latency value assigned for each group interrupt controller.

By assigning a latency value for each group interrupt controller, the interrupt controller can efficiently handle interrupts of different priorities.

Claim 8 defines the corresponding method of handling interrupts.

3.2 The basis in the application as filed for claims 1 and 8 of the auxiliary request is claim 7 in combination with the disclosure from page 8, line 28 to page 9, line 2. The auxiliary request therefore complies with the requirements of Article 123(2) EPC.

3.3 The subject-matter of the independent claims of the auxiliary request involves an inventive step over D5 for the same reasons as the main request. The skilled person would have had no reason to use coalescing in the arrangement in D5, let alone coalescing based on a time window that is individually defined for each group interrupt controller.

3.4 Starting from the disclosure of D1, the problem to be solved is how to efficiently handle interrupts of different priorities. There is nothing in the prior art at hand that would have prompted the skilled person to add additional group interrupt controllers, each having a coalescing time window defined based on a latency value assigned individually for each group interrupt controller. Nor is this part of the skilled person's common general knowledge.

Thus, the Board judges that the subject-matter of claim 1 of the auxiliary request involves an inventive step over D1 (Article 56 EPC).

3.5 No objection was raised during the examination proceedings based on documents D2 to D4 and the Board considers the disclosure in those documents to be no more relevant than that provided by D1 and D5.

4. *Completeness of the search*

4.1 In the communication accompanying the summons to oral proceedings, the Board had some doubts whether the aspect of a plurality of group interrupt controllers had been sufficiently searched. However, since this subject-matter was present in claim 7 and 8 as originally filed, which are indicated as searched in the search report, the Board must be able to assume that it was searched completely.

5. *The request for reimbursement of the appeal fee*

5.1 The appellant argued that the examining division's failure to deal with all the independent claims of the then main request constituted a substantial procedural violation, which warranted the reimbursement of the appeal fee under Rule 103(1)(a) EPC.

The appellant cited the EPO Guidelines (IX-5.1): *"The decision should normally deal with all independent claims of the valid request(s) that were discussed during the proceedings"*.

5.2 The Board does not consider that the appeal fee should be reimbursed. Whilst it might have been desirable that the decision under appeal included reasoning with respect to all independent claims and thus also claim 9, the fact that claim 1 of the main request did not fulfill the requirements of the EPC meant that the main request could not be allowed, even if independent claim 9 complied with the requirements of the EPC. As the examining division decided on all requests before it, the Board does not consider that a substantial procedural violation occurred.

For these reasons the appellant's request for the refund of the appeal fee is rejected.

Order

For these reasons it is decided that:

The decision under appeal is set aside.

The case is remitted to the examining division with the order to grant a patent in the following version:

Description: pages 1-8 filed during the oral proceedings on 16 January 2020

Claims 1-14 filed during the oral proceedings on 16 January 2020

Drawings: Sheets 1/4-4/4 as originally filed.

The request for the reimbursement of the appeal fee is refused.

The Registrar: The Chairman:

T. Buschek W. Chandler

Decision electronically authenticated