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Datasheet for the decision of 5 February 2018

Case Number: T 0976/13 - 3.4.03

Application Number: 03255355.4

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Language of the proceedings: EN

Title of invention:
Nanometer-scale semiconductor devices and method of making

Applicant:
Samsung Electronics Co., Ltd.

Headword:

Relevant legal provisions:
EPC 1973 Art. 56

Keyword:
Inventive step - (yes)

Decisions cited:

Catchword:

Europäisches Patentamt
European Patent Office
Office européen des brevets

Beschwerdekammern

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Case Number: T 0976/13 - 3.4.03

D E C I S I O N
of Technical Board of Appeal 3.4.03
of 5 February 2018

Appellant: (Applicant)	Samsung Electronics Co., Ltd. 129, Samsung-ro Yeongtong-gu Suwon-si, Gyeonggi-do, 443-742 (KR)
Representative:	Mounteney, Simon James Marks & Clerk LLP 90 Long Acre London WC2E 9RA (GB)
Decision under appeal:	**Decision of the Examining Division of the European Patent Office posted on 31 October 2012 refusing European patent application No. 03255355.4 pursuant to Article 97(2) EPC.**

Composition of the Board:

Chairman	G. Eliasson
Members:	M. Papastefanou
	C. Schmidt

Summary of Facts and Submissions

I. The appeal is against the decision of the Examining Division refusing the European patent application No. 03 255 355.4 on the grounds that neither the Main nor the Auxiliary request before it involved an inventive step within the meaning of Article 56 EPC.

The following document, cited during the first instance procedure, is relevant for this decision:

D7: US 5 772 905 A

II. In the grounds of appeal, the Appellant (Applicant) requested that the decision of the Examining Division be set aside and that a patent be granted according to the Main request or, as an auxiliary measure, according to one of the First, Second or Third Auxiliary requests, all of which were filed with the grounds of appeal. The Appellant requested also the holding of oral proceedings, should the Board be minded to refuse the Main request or any of the Auxiliary requests.

III. In a communication pursuant to Article 15(1) Rules of Procedure of the Boards of Appeal (RPBA), which was annexed to the summons to oral proceedings, the Board issued its preliminary opinion, according to which the Main request did not meet the requirements of Article 123(2) EPC and the subject matter of claim 1 of the First Auxiliary request did not involve an inventive step in view of D7 and the common general knowledge of the skilled person. Regarding the Second Auxiliary request, the Board indicated that it appeared to be meeting the requirements of Article 52(1) EPC but not those of Article 84 EPC 1973 because of an unclear term

in claim 1.

IV. In reaction to the Board's communication, the Appellant withdrew the Main and First Auxiliary requests filed with the grounds of appeal, as well as its request for oral proceedings. In addition, it filed an amended Second Auxiliary request taking into account the Board's objection, as well as amended description pages.

V. Following the Appellant's reaction, the Board cancelled the scheduled oral proceedings and issues its decision in writing.

VI. The Appellant requests that the decision under appeal be set aside and that a patent be granted in the following version (amended Second Auxiliary request):

Claims 1-6 filed with the letter dated 19 December 2017;

Description pages 1-26 filed with the letter dated 19 December 2017;

Drawing sheets 1/17-17/17 filed with the letter dated 25 September 2003.

The Third Auxiliary request filed with the grounds of appeal is not relevant for this decision.

VII. Independent claim 1 of the amended Second Auxiliary request is worded as follows:

A method for forming nanoscale semiconductor junctions comprising:
creating an epitaxial semiconducting layer including a

dopant of a first polarity formed on a semiconductor substrate having a dopant of a second polarity, wherein the second polarity is opposite to the first polarity;
creating an imprint layer (686) on said epitaxial semiconducting layer;
urging a nanoimprinter (687) toward said imprint layer;
removing selective portions of said epitaxial semiconducting layer;
forming an epitaxial semiconducting structure having an area having at least one lateral dimension less than 75 nanometers; and
forming a first semiconducting junction having an area having at least one lateral dimension less than 75 nanometers; and further comprising:
creating a first planarizing dielectric layer (782) over said epitaxial semiconducting structure;
co-planarizing said first planarizing dielectric layer (784) to substantially the same thickness as said epitaxial semiconductor structure;
creating a second semiconducting layer (785) including a dopant of a second polarity over said epitaxial semiconducting layer and said first planarizing dielectric layer;
creating a second imprint layer (786) on said second semiconducting layer;
urging a nanoimprinter (787) toward said second imprint layer;
removing selective portions of said second semiconducting layer; and
forming a second semiconducting structure having an area having at least one lateral dimension less than 75 nanometers.

Reasons for the Decision

1. Amendments

1.1 Independent claim 1 finds basis in original claims 9, 10 and 13.

1.2 Dependent claims 2, 3, 4, 5 and 6 correspond to original claims 14, 15, 16, 17 and 18 respectively.

1.3 The Board is, hence, satisfied that the requirements of Article 123(2) EPC are met.

2. Inventive step

The Examining Division considered D7 as the closest prior art. The Appellant did not contest this and the Board does not see any reason to differ.

2.1.1 D7 describes a method of forming patterns (lithography) in nanoscale size (see Abstract). The method is similar to the one used in the claimed invention: an imprint layer (thin film layer 20) is formed on a substrate (18) and a nanoimprinter (mold 10) is urged on the imprint layer to create a pattern. The formed pattern is used then as resist for forming a pattern on the substrate (see Figures 1A-1D, column 2, lines 19-34, column 3, line 28 - column 4, line 49).

2.1.2 There is no disclosure in D7 of forming an epitaxial semiconducting layer having a dopant of a first polarity on a semiconductor substrate having a dopant of a second (opposite) polarity. In other words, there is no disclosure of forming a semiconductor junction using the described nanoscale lithography method. There is general mention in D7 of using the described lithography method in the creation of integrated circuits and microdevices (column 2, lines 19-21), as

well as mention of a general need for an improved lithography method to be used in the manufacturing of semiconductor integrated circuits (column 2, lines 13-16).

2.1.3 In addition, there is no disclosure in D7 of

creating a first planarizing dielectric layer over said epitaxial semiconducting structure;
co-planarizing said first planarizing dielectric layer to substantially the same thickness as said semiconductor structure;
creating a second semiconducting layer including a dopant of a second polarity over said epitaxial semiconducting layer and said first planarizing dielectric layer;
creating a second imprint layer on said second semiconducting layer;
urging a nanoimprinter toward said second imprint layer;
removing selective portions of said second semiconducting layer; and
forming a second semiconducting structure having an area having at least one lateral dimension less than 75 nanometers.

2.2 In essence, the main difference between the invention in claim 1 and D7 is that in claim 1 there is a method for forming a bipolar junction transistor by forming two semiconductor structures one over the other, separated by a dielectric layer, whereas D7 describes a general method of nanoscale lithography. There are some general statements in D7 about possible use of the described lithography method in the creation of integrated circuits and microdevices (column 2, lines

19-21) but there are no more details (see also point 2.1.2 above).

2.3 The technical problem the skilled person starting from D7 would be faced with would thus be how to create a bipolar junction transistor using the described lithography method.

2.4 Even if it were to be considered that forming an epitaxial semiconducting layer having a dopant of a first polarity on a semiconductor substrate having a dopant of a second (opposite) polarity is a common and generally used way of forming semiconductor junctions, as the Board stated in its preliminary opinion, the claimed method comprises more steps, which go beyond what could be considered as obvious for the skilled person.

As already stated, in D7 there is only a description of the nanoscale lithography method in general with only some vague indication(s) about possible applications. Even if the use of the described nanoscale lithography method to form a semiconductor junction, or even two semiconductor junctions, were to be considered as obvious for the skilled person, the specific method of claim 1 cannot be considered as such.

According to the Board's opinion, the specific order of steps in claim 1 and, in particular, the creating and co-planarizing of a first dielectric layer over the epitaxial semiconductor structure before forming the second semiconductor structure over it, cannot be deduced from D7 in an obvious manner and would require the exercise of inventive skill by the skilled person.

2.5 The Board concludes, therefore, that the subject matter of claim 1 involves an inventive step within the meaning of Article 56 EPC 1973.

3. The term "about" in the expression less *about 75 nanometers* in claim 1, which was objected to as being unclear by the Board in its preliminary opinion (see point 4.1 of the communication annexed to the summons to oral proceedings), has been removed from the amended claims. The requirements of Article 84 EPC 1973 are, hence, met.

4. The description has been adapted to the new claims and the document D7 is also mentioned therein.

5. The Board is, therefore, satisfied that the requirements of EPC and EPC 1973 are met.

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the department of first instance with the order to grant a patent in the following version:

   Claims 1-6 filed with the letter dated 19 December 2017;

   Description pages 1-26 filed with the letter dated 19 December 2017;

   Drawing sheets 1/17-17/17 filed with the letter dated 25 September 2003.

The Registrar: The Chairman:

S. Sánchez Chiquero G. Eliasson

Decision electronically authenticated