

Internal distribution code:

- (A) [-] Publication in OJ
- (B) [-] To Chairmen and Members
- (C) [-] To Chairmen
- (D) [X] No distribution

**Datasheet for the decision
of 5 March 2019**

Case Number: T 0656/13 - 3.5.06

Application Number: 08016826.3

Publication Number: 2040159

IPC: G06F9/30, G06F13/16

Language of the proceedings: EN

Title of invention:

Processor and interface

Applicant:

CAMBRIDGE CONSULTANTS LIMITED

Headword:

Processor and interface/CAMBRIDGE CONSULTANTS

Relevant legal provisions:

EPC 1973 Art. 56

Keyword:

Inventive step - (no)

Decisions cited:

Catchword:



Beschwerdekammern
Boards of Appeal
Chambres de recours

Boards of Appeal of the
European Patent Office
Richard-Reitzner-Allee 8
85540 Haar
GERMANY
Tel. +49 (0)89 2399-0
Fax +49 (0)89 2399-4465

Case Number: T 0656/13 - 3.5.06

D E C I S I O N
of Technical Board of Appeal 3.5.06
of 5 March 2019

Appellant: CAMBRIDGE CONSULTANTS LIMITED
(Applicant) Science Park,
Milton Road
Cambridge CB4 0DW (GB)

Representative: Cozens, Paul Dennis
Mathys & Squire LLP
The Shard
32 London Bridge Street
London SE1 9SG (GB)

Decision under appeal: Decision of the Examining Division of the
European Patent Office posted on 19 October 2012
refusing European patent application No.
08016826.3 pursuant to Article 97(2) EPC.

Composition of the Board:

Chairman M. Müller
Members: A. Teale
A. Jimenez

Summary of Facts and Submissions

I. The present appeal is against the decision, dispatched with reasons on 19 October 2012, to refuse the application on the basis that the subject-matter of claim 1 did not involve an inventive step in view of the disclosure of D2 combined with *inter alia* D4, these documents being:

D2: US 6 311 263 B1

D4: Ray Weiss, "PowerPC On-Chip Debug Hardware Resources", 1 October 2001, [Retrieved from the Internet URL <http://electronicdesign.com/print/embedded/powerpc-on-chip-debughardware-resources3675.aspx> on 17 March 2011]. At present, this document can be found at: <https://www.electronicdesign.com/embedded/powerpc-chip-debug-hardware-resources>

II. A notice of appeal and the appeal fee were received on 17 December 2012, the appellant requesting that the decision be set aside in its entirety and that the application be granted. The appellant also made an auxiliary request for oral proceedings.

III. With a statement of grounds of appeal, received on 28 February 2013, the appellant submitted amended claims according to a main and two auxiliary requests and reiterated the auxiliary request for oral proceedings.

IV. In an annex to a summons to oral proceedings the board set out its preliminary opinion. *Inter alia* the board had doubts regarding claim 1 of all three requests as to clarity, Article 84 EPC 1973, and as to inventive

step, Article 56 EPC 1973, in view of D2 combined with common general knowledge, as exemplified by D4.

V. In a response received on 18 February 2019 the appellant stated that it would not be attending the oral proceedings. No amendments or arguments were submitted. The board then cancelled the oral proceedings.

VI. The application is thus being considered in the following form:

Description (all requests):

pages 4 to 222, as originally filed, and 1 to 3, received on 23 November 2010.

Claims:

Main request: 1 to 18.

First auxiliary request: 1 to 17.

Second auxiliary request: 1 to 18.

Drawings (all requests):

Pages 1/76 to 76/76, received on 8 January 2009.

VII. Claim 1 of the main request reads as follows:

"A data processing apparatus comprising:

a processor constructed to operate under control of a stored program comprising a sequence of program instructions selected from a predetermined processor instruction set; a master processor provided on the same integrated circuit as said processor operable to request access to storage locations of said processor, wherein said processor is configured to function as a slave with respect to the master processor; an

interface circuit provided on the same integrated circuit as said processor which is operable to provide a common interface for both an external master apparatus and said master processor to signal requests for access to storage locations of said processor and/or its associated memory, wherein said processor is also configured to function as a slave with respect to the external master apparatus; and control means operable to provide access between the storage locations and the interface circuit in response to the requests only at predetermined points in the execution of the stored program by said processor, wherein said control means comprises a generic communication instruction of the processor instruction set, the generic communication instruction being available for execution only at said predetermined points by said processor in dependence upon the position of the generic communication instructions within the sequence of stored processor instructions as specified at program time such that execution timing of the stored processor instructions is independent of whether or not a request is actually supplied by said external master apparatus or said master processor at run time to said interface circuit; whereby the master processor and the external master apparatus are operable to access storage locations of said processor and/or its associated memory during real time operation of said processor without altering the timing or functionality of said processor, and are further adapted to control and/or debug said processor."

- VIII. Compared to claim 1 of the main request, claim 1 of the first auxiliary request sets out a plurality of slave processors as well as a master processor on the same integrated circuit.

IX. Compared to claim 1 of the main request, claim 1 of the second auxiliary requests sets out the following additional features:

"wherein the master processor and the external master apparatus operate independently and asynchronously of one another" and

"wherein debug instructions are passed via said generic communication instruction".

Reasons for the Decision

1. The admissibility of the appeal

In view of the facts set out at points I to III above, the appeal fulfills the admissibility requirements under the EPC and is consequently admissible.

2. A summary of the invention

2.1 According to page 73, lines 1 to 6, the description sets out three embodiments of the invention, namely the SIF Network Debug Interface (see page 73, line 26, to page 111, line 34, and figures 1 to 32), the XAP3 32-bit ASIC processor (see page 111, line 35, to page 160, line 13, and figures 33 to 47) and the XAP4 16-bit ASIC processor (see page 160, line 14, onwards and figure 48 onwards.)

2.2 The data processing apparatus according to claim 1, the only independent claim of all requests, sets out an interface according to the first embodiment in combination with a processor according to either the second or the third embodiment.

- 2.3 As illustrated in figure 31, the application relates to an integrated circuit, for instance an ASIC (Application Specific Integrated Circuit), comprising a slave processor (XAP 0,1) running a program comprising instructions stored in an associated memory (Memory 0,1), and a common interface circuit (termed the "interface circuit" in claim 1 and the "SIF module" in the description and drawings).
- 2.4 The interface circuit receives requests from an internal master processor (termed the "iSIF Master") and, via an "SIF pod", requests from an external computer to access storage locations of the slave processor (by which the board understands, for instance, registers) and via the slave processor to access storage locations in the associated memory, the purpose being to control and/or debug the slave processor.
- 2.5 The SIF pod comprises a hardware interface between the ASIC and a personal computer; see page 17, line 32. According to page 17, lines 11 to 12, "The SIF Pod and the SIF computer together may be referred to as a SIF master".
- 2.6 The iSIF master is connected to the interface circuit by a parallel interface "iSIF" (see page 15, lines 12 to 13, and page 105, table 17), whereas the external master apparatus (i.e. the master computer and SIF pod) is connected to the interface circuit via a serial interface "xSIF" of the integrated circuit; see page 19, lines 15 to 17. The SIF module deals alternately with xSIF and iSIF requests; see page 24, lines 1 to 6.
- 2.7 According to page 22, lines 31 to 40, and page 23, lines 19 to 23, both the internal and the external

master can read and write to the memory and registers of each individual slave processor and also issue debug commands, such as Start, Stop and Single-Step. However the claims are directed to embodiments in which the slave processor is not stopped during debugging. According to claim 1, the integrated circuit also comprises control means to allow the interface circuit to access the storage locations only at points determined by the position of generic communication instructions in the program, the execution timing of the stored instructions being independent of whether the masters request access from the interface. The board understands the "generic communication instructions" in this context as the various break instructions mentioned (first embodiment) from page 65, line 34, to page 70, line 7, (second embodiment) from page 113, line 7, to page 115, line 2, and (third embodiment) from page 162, line 10, to page 163, line 5.)

2.8 The board understands the independence of execution timing from access requests, mentioned in claim 1, in the light of page 73, lines 37 to 38, which states that the external master apparatus "can read or write any memory-mapped address inside the SIF slave in real time, **without affecting the timing or functionality of the SIF slave**" (emphasis by the board); see also the statements regarding not stopping the processor on page 114, lines 14 to 16, (second embodiment) and page 162, lines 19 to 21 (third embodiment).

3. The board's understanding of certain terms in the claims

3.1 Regarding the expression in claim 1 "integrated circuit", the board notes that the description states

that "The SIF Slave is typically an ASIC or FPGA or Integrated Circuit (IC) or chip". However, figures 4, 11, 12, 13, 16 and 17 all refer to a "SIF Slave PCB". Hence the board understands the expression in claim 1 "Integrated Circuit" broadly to cover "ASIC", "FPGA", "chip" and "PCB" (Printed Circuit Board).

3.2 Claim 1 refers to the internal master processor and the external master apparatus being "further adapted to control and/or debug [the slave] **processor**" (emphasis by the board). The description, for instance page 162, lines 20 to 21, mentions "debugging User Mode **applications**" (emphasis by the board). The board understands from this that the internal master processor and external master apparatus can read and write to storage locations of the slave processor and/or its associated memory as it carries out the instructions of an application program. In this context "controlling" the slave processor is understood to mean writing to its storage locations and/or those of the associated memory.

4. Clarity, Article 84 EPC 1973

Despite the doubts expressed in the board's preliminary opinion, the board finds that the claims are sufficiently clear to be construed for the purposes of assessing inventive step.

5. The prior art on file

5.1 Document D2

5.1.1 According to its abstract and figure 1, D2 relates to a single-chip data processing device (IC) comprising a processor core (100) with a "Harvard

architecture" (i.e. separate buses and storage for instructions and data); see program memory (ROM 104) and data memory (RAM 108, ROM 106) and column 3, lines 64 to 66. The IC comprises two external pins (STOPB and RUN_STEP) (see column 4, lines 42 to 46, and column 11, line 42, to column 12, line 15) for debugging purposes (DEBUG) and a further four external pins (SER_IN, SER_OUT, SER_CLK and SER_LOADB) for a serial interface (SIF); see column 12, line 54, to column 13, line 20).

5.1.2 The debugging interface (DEBUG) provides the debugging operations start, stop, breakpoint and single step. These functions are not however intended to be used by application programs; see column 11, line 42, to column 12, line 15. When the processor executes the BRK (Break) instruction (see column 15, lines 44 to 46) it stops, unless the RUN_STEP pin is held high. Thus strategic breakpoints can be left in the program code and enabled using the RUN_STEP pin for test and verification purposes.

5.1.3 The serial interface (SIF) allows an external master apparatus to directly access the program and data spaces of the processor and its registers (see column 13, lines 3 to 5) to read and write data (see column 10, lines 30 to 31) for testing during circuit design and manufacture as well as for linking the IC post-manufacture to an external microprocessor providing "testability functions"; see column 12, line 54, to column 13, line 20, and column 3, lines 54 to 63. The serial clock SER_CLK is asynchronous with the processor clock; see sentence bridging columns 12 and 13. When the processor is running normally, the registers and limited data space areas cannot be written to; see column 13, lines 9 to 13. However, when the processor is stopped, the registers and full data space can be

written to. An example of the serial interface is illustrated in figure 7 and described from column 16, line 25, to column 17, line 39.

- 5.1.4 According to the last seven lines of claim 1 in D2 (see also claims 52 and 55), the control means in D2 is "operable to fix periods of time for providing such access relative to the sequence of program instructions such that execution timing of the stored program is independent of whether or not such a communication request is supplied to said interface circuit by said external apparatus".
- 5.1.5 Figure 12 shows an embodiment in which an external master microprocessor (1200) communicates with three slave ASICs (1202, 1204, 1206); see column 23, line 66, to column 24, line 21.
- 5.1.6 In terms of claim 1 of the main request, D2 discloses (see figures 1 and 12) a data processing apparatus comprising: a processor (core 100, slave 1202) constructed to operate under control of a stored program (program ROM 104) comprising a sequence of program instructions selected from a predetermined processor instruction set; an interface circuit (see the circuitry in figure 1 between the core 100 and the pins of the chip 102) provided on the same integrated circuit as said processor which is operable to provide an interface (SIF and DEBUG pins) for an external master apparatus to signal requests for access to storage locations of said processor (100) and/or its associated memory (104), wherein said processor is also configured to function as a slave with respect to the external master apparatus (see figure 12 and column 23, line 66, to column 24, line 21); and control means operable to provide access between the storage

locations and the interface circuit in response to the requests only at predetermined points in the execution of the stored program by said processor (see claim 1 of D2), wherein said control means comprises a generic communication instruction of the processor instruction set (see claim 2 of D2), the generic communication instruction being available for execution only at said predetermined points by said processor in dependence upon the position of the generic communication instructions within the sequence of stored processor instructions as specified at program time such that execution timing of the stored processor instructions is independent of whether or not a request is actually supplied to said interface circuit (see claim 1 of D2); whereby the external master apparatus is operable to access storage locations of said processor and/or its associated memory during real time operation of said processor without altering the timing or functionality of said processor, and is further adapted to control and/or debug said processor; see claim 1 of D2, lines 19 to 29, and column 23, line 45, to column 24, line 21.

5.2 Document D4

5.2.1 The decision refers to D4 as evidence that it was known in the prior art to provide debugging circuitry on-chip as well as off-chip.

5.2.2 D4 describes the PowerPC chip which comprises an on-chip processor (COP) (see page 1, lines 8 to 11) for on-chip debugging. Off-chip debugging is also possible, via the "Power Port Debug Interface"; see page 1, lines 17 to 19, and page 2, lines 10 to 11. Debugging occurs in a special "Debug Mode", meaning that a debug event may cause an interrupt; see page 1, lines 24 to 26.

5.2.3 There is no disclosure of the main PowerPC processor being a slave to the COP.

6. Inventive step, Article 56 EPC 1973

6.1 According to the appealed decision, the subject-matter of claim 1 differed from the disclosure of the closest prior art document D2 in that master circuitry was provided on the same integrated circuit as the processor which was operable to request access to storage locations of the processor. Moreover the interface was operable to provide an interface for the master circuitry, and the execution timing of the stored processor instructions was independent of whether or not a request was actually supplied by the master circuitry at run time to the interface circuit. Providing a debugging circuit on the chip in addition to an external debugger was a known technique in the art of debugging; see D3 (paragraph [3]) and the whole of a further document D4. The skilled person would have been aware of this option and introduced such a debugger on the integrated circuit of D2 without taking an inventive step. The other difference features were direct consequences of taking this approach, integrating more (or less) components on a chip being a usual matter for the skilled person.

6.2 In the grounds of appeal the appellant argued that claim 1 of the main request had been amended to add the following characterizing features over the disclosure of D2, in addition to those identified in the decision:

(a) the master circuitry was a master processor operable to request access to the storage locations

of the embedded processor, which was configured to operate as a slave to said master processor,

(b) the master processor and the external master apparatus were both operable to access storage locations of the slave processor and/or its associated memory during real time operation of the slave processor without altering the timing or functionality of the slave processor and

(c) the master processor and the external master apparatus were both adapted to control and/or debug the slave processor.

The appellant also argued that in D2 a "non-invasive" serial interface allowed an external apparatus, such as an external PC, to request access to storage locations of the slave processor. This interface did not interrupt execution timing and was used during production and testing of processors. In contrast to the invention, the non-invasive serial interface was not used for debugging; this was done using another, dedicated, interface; see figure 1, item 102. The invention was aimed at accessing processor/memory storage locations of embedded processors to upgrade their software in the field whilst minimising the required number of chip pins. The solution lay in providing an on-chip master processor and modifying the non-invasive interface to accept debug instructions and to allow both the existing external master apparatus and the new on-chip master processor to control the slave processor. Thus the non-invasive interface used to debug and/or control the slave processor during production and/or testing could now be used in the field to do the same thing. D2 contained no hint at doing this, rather than using the known external serial

interface. D4 did not disclose adding an on-chip master processor to access storage locations in a slave processor or its memory. In D4 a PowerPC was debugged in a special debugging mode in a manner which changed its timing and function. Hence even the combination of D2 with D4 did not yield the subject-matter of claim 1.

6.3 The board's finding on inventive step

6.3.1 In view of the above analysis, the subject-matter of claim 1 of the main request differs from the disclosure of D2 in the following features:

- i. a master processor is provided on the same integrated circuit as the processor, said processor also being configured to function as a slave with respect to said master processor, the master processor being operable to access storage locations of said processor and/or its associated memory during real time operation of said processor without altering the timing or functionality of said processor, and being further adapted to control and/or debug said processor,
- ii. the interface circuit is a common interface operable to also provide an interface for said master processor to signal requests for access to storage locations of said processor and/or its associated memory.

6.3.2 According to the appellant, the claimed subject-matter also differs from the disclosure of D2 in that the invention allows the non-invasive serial interface, used in D2 to debug and/or control the slave processor during production and/or testing, to now be used in the

field to do the same thing. The board is not persuaded that this difference exists, since D2 discloses the serial interface being usable to link the processor (100) to an external processor post-manufacture to provide "testability functions"; see column 3, lines 54 to 63. Moreover how the claimed integrated circuit is used, be it in production testing or debugging in the field, is not a feature of the integrated circuit itself. Given that an "integrated circuit" according to claim 1 can be understood as a chip on a PCB including an external master, the serial interface in D2 (including the debug pins) could be used to debug the processor both during production and in the field. The board appreciates that, generally speaking, "debugging" during production differs from "debugging" in the field, but the description does not explain how they differ. The appellant has also not explained why the use of the integrated circuit "in the field" implies that there is no external master apparatus.

6.3.3 The appellant has also not explained what technical effects the addition of an internal master processor and appropriate adaption of the interface has. It is not, for instance, miniaturization of the debugging circuitry by moving it onto the integrated circuit, since claim 1 covers the case of the external master apparatus still being present and the description mentions dealing alternately with iSIF and xSIF requests.

6.3.4 The decision does not define an objective technical problem which is solved to arrive at the invention. The appellant has argued that the invention is aimed at accessing processor/memory storage locations of embedded processors to upgrade their software in the field. This aim is not however mentioned in the

application, and upgrading software need not involve debugging.

- 6.3.5 The board regards the objective technical problem as being to provide an alternative way of debugging the slave processor.
- 6.3.6 At the priority date the skilled person would have been aware of data processing apparatuses with both on-chip and off-chip debugging processors, as exemplified by D4; see COP, page 1, lines 8 to 11.
- 6.3.7 The skilled person would have recognised that an internal debugging processor solved the objective technical problem, there being no reason to also add the feature, known from D4, that debugging stops the processor under test. Hence the skilled person starting from D2 would have added an internal master to the chip in D2 (difference feature "i") as a matter of usual design. This change would have required adaption of the interface circuit known from D2. The claimed solution is that the interface circuit treats both the internal and the external master processors in the same way, namely the way that is known from D2 (difference feature "ii"). The board regards modifying an existing interface for an additional use rather than adding another interface specifically for that as a matter of convenience and economy and thus a usual design choice for the skilled person, it having no unexpected advantage or synergy with difference feature "i".
- 6.3.8 Regarding the first auxiliary request, claim 1 differs from that of the main request in setting out a plurality of slave processors with memory. Given the disclosure in D2 in figure 12 and column 23, line 66, to column 24, line 21, of a plurality of slave ASICs,

the difference feature is known from D2 and is thus unable to lend inventive step to claim 1 in view of the combination of D2 and common general knowledge, set out above for the main request.

6.3.9 Regarding the second auxiliary request, claim 1 differs from that of the main request in the features that:

- a. the master processor and the external master apparatus operate independently and asynchronously of one another, and
- b. debug instructions are passed via said generic communication instruction.

In the board's view, neither difference feature is able to lend inventive step to claim 1. Regarding feature "a", according to D2, the serial clock SER_CLK is asynchronous with the processor clock; see sentence bridging columns 12 and 13. Feature "a" sets out a simple extension of this principle, it being usual that processors operate independently of one another.

Regarding feature "b", D2 states that the serial interface (SIF) allows an external master apparatus to directly access the program and data spaces of the processor and its registers (see column 13, lines 3 to 5) to read and write data (see column 10, lines 30 to 31) for testing during circuit design and manufacture. In the board's view this implies that debug instructions are passed via the generic communication instruction mentioned in claim 2 of D2. Hence this feature is also known from D2 and is thus unable to lend inventive step to claim 1.

Order

For these reasons it is decided that:

The appeal is dismissed.

The Registrar:

The Chairman:



L. Stridde

M. Müller

Decision electronically authenticated