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Datasheet for the decision of 27 August 2015

Case Number: T 0184/13 - 3.5.05

Application Number: 05011019.6

Publication Number: 1564950

IPC: H04L25/02

Language of the proceedings: EN

Title of invention:
Timing signal generator

Applicant:
FUJITSU LIMITED

Headword:
Timing circuit/FUJITSU

Relevant legal provisions:
EPC Art. 56, 76(1), 84, 123(2)
RPBA Art. 12(4)

Keyword:
Admission of main request - (no): withdrawn at first instance
Admissible amendments - first and third auxiliary request (no)
Clarity - first auxiliary request (no)
Inventive step - second and third auxiliary request (no)

Decisions cited:
T 0922/08, T 2278/08, T 1231/09

Catchword:

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Case Number: T 0184/13 - 3.5.05

D E C I S I O N
of Technical Board of Appeal 3.5.05
of 27 August 2015

Appellant: (Applicant)	FUJITSU LIMITED 1-1, Kamikodanaka 4-chome, Nakahara-ku Kawasaki-shi, Kanagawa 211-8588 (JP)
Representative:	Stebbing, Timothy Charles Haseltine Lake LLP Lincoln House, 5th Floor 300 High Holborn London WC1V 7JH (GB)
Decision under appeal:	**Decision of the Examining Division of the European Patent Office posted on 18 July 2012 refusing European patent application No. 05011019.6 pursuant to Article 97(2) EPC.**

Composition of the Board:

Chair	A. Ritzka
Members:	K. Bengi-Akyuerek
	D. Prietzel-Funk

Summary of Facts and Submissions

I. The appeal is against the decision of the examining division to refuse the present European patent application - divided from its parent application No. 99304279.5 - on the grounds of lack of inventive step (Article 56 EPC) with respect to a sole claim request, having regard to the combined disclosures of

D1: R.C. Walker et al.: "A 10Gb/s Si-Bipolar TX/RX Chipset for Computer Data Transmission", Proceedings of IEEE International Solid-State Circuits Conference ISSCC98, pp. 302-303 and 450, February 1998;

D3: T.A. Knotts et al.: "A 500 MHz Time Digitizer IC with 15.625ps Resolution", Proceedings of IEEE International Solid-State Circuits Conference ISSCC94, pp. 58-59, February 1994.

Furthermore, the following prior-art documents were also cited in the course of the examination proceedings:

D2: M. Horowitz et al.: "PLL Design for a 500 MB/s Interface", Proceedings of IEEE International Solid-State Circuits Conference ISSCC93, pp. 160-161 and 282, February 1993;

D4: T.H. Lee et al.: "A 2.5V Delay-Locked Loop for an 18Mb 500MB/s DRAM", Proceedings of IEEE International Solid-State Circuits Conference ISSCC94, pp. 300-301, February 1994.

II. With the statement setting out the grounds of appeal, the appellant filed an amended set of claims according to an auxiliary request (referred to as "first auxiliary request" in the following). It requested that

the decision of the examining division be set aside and that a patent be granted on the basis of the claims submitted in the first-instance proceedings with the letter dated 3 May 2012 as its main request or on the basis of the newly filed first auxiliary request.

III. In an annex to the summons to oral proceedings pursuant to Article 15(1) RPBA, the board gave its preliminary opinion on the appeal. In particular, it expressed concerns about the admissibility of the main request under Article 12(4) RPBA, raised objections under Articles 123(2), 76(1) and 84 EPC, and made preliminary observations on novelty and inventive step.

IV. With a letter of reply, the appellant filed additional sets of amended claims according to second and third auxiliary requests.

V. Oral proceedings were held as scheduled on 27 August 2015, during which the admissibility and allowability of all claim requests on file were discussed.

The appellant's final request was that the decision under appeal be set aside and a patent be granted on the basis of the claims of the main request, submitted with the letter dated 3 May 2012, or of the first auxiliary request, submitted with the statement setting out the grounds of appeal, or on the basis of the second or third auxiliary requests, submitted with the letter dated 16 July 2015. At the end of the oral proceedings, the decision of the board was announced.

VI. Claim 1 of the **main request** reads as follows:

"A timing signal generator circuit comprising:
a first timing signal generator (3001) arranged to

receive a clock signal (CKr), give the clock signal a variable delay, and generate a first timing signal (CKs) by a phase interpolator (3012) of high frequency based on the delayed clock signal;

a phase controller (3002) arranged to control a phase of the first timing signal; and

a second timing signal generator (3003) arranged to divide a frequency of the first timing signal by an integer to generate a second timing signal (CKin)."

Claim 1 of the **first auxiliary request** reads as follows:

"A timing signal generator circuit comprising:

a first timing signal generator (3001), including a multiphase clock generator circuit (3011) arranged to receive a clock signal (CKr) and generate multiphase output signals (φ1,φ2,φ3,φ4), and a phase interpolator (3012) arranged to receive the multiphase output signals of said multiphase clock generator circuit, arranged to give the clock signal (CKr) a variable delay, and generate a first timing signal (CKs);

a phase controller (3002) arranged to control a phase of the first timing signal (CKs) by controlling the phase interpolator (3012); and

a second timing signal generator (3003) arranged to divide a frequency of the first timing signal (CKs) by an integer to generate a second timing signal (CKin)."

Claim 1 of the **second auxiliary request** reads as follows (amendments compared with the first auxiliary request underlined by the board):

"A timing signal generator circuit comprising:

a first timing signal generator (3001), including a <u>4-phase</u> clock generator circuit (3011) arranged to

receive a clock signal (CKr) and generate 4-phase output signals (φ1,φ2,φ3,φ4), and a phase interpolator (3012) arranged to receive the 4-phase output signals of said 4-phase clock generator circuit, arranged to give the clock signal (CKr) a variable delay, and generate a first timing signal (CKs) having an optional phase determined by the 4-phase output signals (φ1,φ2,φ3,φ4);

a phase controller (3002) arranged to control the phase of the first timing signal (CKs) by controlling the phase interpolator (3012); and

a second timing signal generator (3003) arranged to divide the frequency of the first timing signal (CKs) by an integer to generate a second timing signal (CKin), wherein said 4-phase clock generator circuit (3011) is a delay locked loop circuit."

Claim 1 of the **third auxiliary request** comprises all the features of claim 1 of the second auxiliary request, except for its last phrase "wherein said 4-phase clock generator circuit (3011) is a delay locked loop circuit", and adds the following phrase at its end:

"wherein said phase controller (3002) includes:

a phase comparison circuit (3021) arranged to compare the phase of the second timing signal (CKin) with the phase of an external clock signal (CKe) supplied externally of the timing signal generator; and

an up/down counter (3022) connected to an output (UP/DW) of the phase comparison circuit (3021) for providing an output signal to control the phase of the first timing signal (CKs)."

Reasons for the Decision

1. MAIN REQUEST

This request corresponds to the set of claims filed for the first time in the first-instance proceedings on 3 May 2012 (as the then applicant's sole claim request).

1.1 *Admission into the appeal proceedings*

The claims of this request had already been discussed and objected to under Articles 123(2) and 84 EPC (notably due to the phrase "by a phase interpolator of high frequency") in the first-instance proceedings (see minutes of the oral proceedings held on 13 June 2012 before the examining division, items 3.1 and 3.2). The then applicant, of its own volition, subsequently replaced those claims with a new set of claims including an amendment in order to overcome those objections (cf. minutes of the first-instance oral proceedings, item 5). On the basis of this amended claim request the application was eventually refused under Article 56 EPC (cf. point I above). Furthermore, the appellant did not provide any further substantiation, as to the objections raised by the examining division under Articles 123(2) and 84 EPC, for re-filing the abandoned claims in the appeal proceedings.

It follows from the above that the claims of the present main request had already been presented in the first-instance proceedings and were thereafter abandoned. That prevented them from being decided on their merits by the examining division, with the consequence that this board would have to decide on the

main request as if it were a first-instance department. Such a situation, however, is generally to be avoided (see e.g. ex parte cases T 922/08, point 2.1; T 2278/08, point 2; T 1231/09, point 1). The board concludes therefrom that this claim request not only *could* but also *should* have been presented and prosecuted in the examination proceedings within the meaning of Article 12(4) RPBA.

The board sees the appellant's argument that the amendment filed to overcome the objections of the examining division "was not in fact necessary" (see statement setting out the grounds of appeal, page 3, third paragraph) as reinforcing its view that the appellant should indeed have maintained those claims before the examining division e.g. by filing them at least as an auxiliary request so that it would have obtained an appealable decision on them. Therefore, in the exercise of its discretion, the board declined to admit this request into the appeal proceedings.

1.2 In conclusion, the main request is not admissible under Article 12(4) RPBA.

2. FIRST AUXILIARY REQUEST

Claim 1 of this auxiliary request comprises the following features (as labelled by the board):

A timing signal generator circuit comprising:

a) a first timing signal generator, including a multi-phase clock generator circuit arranged to receive a clock signal and generate multi-phase output signals, and a phase interpolator arranged to receive multi-phase output signals of said multi-phase clock generator circuit, arranged to

give the clock signal a variable delay, and generate a first timing signal;

b) a phase controller arranged to control a phase of the first timing signal by controlling the phase interpolator;

c) a second timing signal generator arranged to divide a frequency of the first timing signal by an integer to generate a second timing signal.

2.1 Articles 123(2) and 76(1) EPC

In the board's judgment, claim 1 of this request does not comply with Articles 123(2) and 76(1) EPC, for the following reasons:

2.1.1 As regards feature a) of claim 1, both the present divisional application and its parent application as originally filed state at page 50, lines 6-11:

"... An embodiment of the third aspect effectively variably delays the clock signal CKr not only by directly delaying the clock signal CKr with the use of a variable delay line but also by controlling the phase of the clock signal CKr with the use of, for example, a phase interpolator"

and at page 50, line 35 to page 51, line 4 relating to Figure 49:

"... The 4-phase clock generator 3011 ... generates 4-phase clock signals ϕ1 to ϕ4, which are supplied to the phase interpolator 3012 to provide a first timing signal CKs having an optional phase determined by the signals ϕ1 to ϕ4."

2.1.2 The board takes from the above passages that the actual function of the phase interpolator is to provide a first timing signal having an optional phase determined by the phases of the clock signals received from a multi-phase clock generator rather than to solely give the received multi-phase clock signals a variable delay, as implied by present claim 1. In the board's view, feature a) thus amounts to an intermediate generalisation of the original disclosure. Therefore, and since moreover the appellant could not provide any other disclosure which might lend additional support for feature a), the board concludes that claim 1 contains subject-matter which extends beyond the content of both the present divisional and the parent application as filed.

2.2 Article 84 EPC

The board further holds that features b) and c) of claim 1 contradict the teaching of the description, since the original description indicates that the phase controller is arranged to control the phase of the first timing signal (cf. page 49, last line to page 50, first line) and that the second timing signal generator is arranged to divide the frequency of the first timing signal CKs (cf. page 50, lines 3-6), rather than controlling or dividing one of (possibly) more phases or frequencies, as suggested by claim 1.

In this regard, the appellant's mere assertion that it was clear to the skilled person which phase and frequency were to be processed by the claimed circuit could not convince the board. In view of the above, the board finds that claim 1 lacks both support by the description and clarity (Article 84 EPC).

2.3 Hence, the first auxiliary request is not allowable under Articles 123(2), 76(1) and 84 EPC.

3. SECOND AUXILIARY REQUEST

Claim 1 of this request differs from claim 1 of the first auxiliary request basically in that it now specifies that (emphasis added by the board)

d) the multi-phase clock generator circuit is a four-phase clock generator circuit and that the output signals are four-phase output signals;
e) the generated first timing signal has an optional phase determined by the four-phase output signals;
f) the phase of the first timing signal is controlled;
g) the frequency of the first timing signal is divided;
h) the four-phase clock generator circuit is a delay locked loop circuit.

Following the amendments made in features d) to g), the board is satisfied that the objections under Articles 123(2), 76(1) and 84 EPC, raised in points 2.1 and 2.2 above, no longer apply.

3.1 Article 52(1) EPC: novelty and inventive step

The board judges that claim 1 of this auxiliary request does not meet the requirements of Article 52(1) EPC, for the following reasons:

3.1.1 The board, firstly, agrees with the appellant that the subject-matter of claim 1 is novel over the cited prior-art documents. As to the evaluation of inventive step, in the decision under appeal, D1 was considered

to be the closest prior art for the claims on file. However, following the introduction of feature h), the board regards document D4 as a more suitable starting point, since it is also concerned with clock synchronisation based on a delay-locked loop (DLL), unlike documents D1 to D3 which rather rely on phase-locked loops (PLLs) based on voltage-controlled oscillators.

3.1.2 Document D4 teaches that, based on an input (reference) clock signal (e.g. "INTCLK" in Figure 1), four clock signals, i.e. two in-phase ("I") signals, having a phase of 0°, and two quadrature ("Q") signals, having a phase of 90°, are generated and fed into a phase interpolator (made up of two sub-units both labelled "PHASE INTERP" in Figure 1). This is done to create a phase-shifted, i.e. variably delayed, output clock signal ("RCLK" in Figure 1) via a receiver DLL (see in particular first page, left-hand column, fourth and fifth paragraphs). Hence, features a), d) and h) of claim 1 are considered to be known from D4.

As to feature e), the resulting phase of the output clock signal of D4 (see "J xor R" signal in Figure 2) is derived from the corresponding input phases (see e.g. first page, left-hand column, fifth paragraph, penultimate sentence: *"... a resultant vector with any phase shift ... can be generated by mixing the I (in-phase) and Q (quadrature) vectors with appropriate weights ..."*). Also, in accordance with features b) and f) of claim 1, a phase selector ("FSM" in Figure 1) controls the phase interpolator of D4 (see e.g. first page, right-hand column, fourth paragraph, first sentence: *"To provide a continuous and unlimited phase shift ... requires seamless switching (controlled by the phase selector FSM) of the signals fed to the*

interpolator").

As to features c) and g) of claim 1, it is apparent to the board that the DLL timing circuit of D4 also relies on a "quadrature divider" whose outputs (denoted as "0°" and "90°" in Figure 1) are at half the frequency of the input signal (see e.g. first page, left-hand column, fifth paragraph). Thus, the board holds that this unit corresponds to a frequency divider, which in this case divides the frequency by two (i.e. the respective integer equals two). However, the board also infers from D4 that said division of the input frequency is performed *prior* rather than *subsequent* to the phase interpolation, as features c) and g) mandate.

3.1.3 Hence, the board concludes that the subject-matter of claim 1 differs from the disclosure of D4 in that the frequency of the "first timing signal" - rather than the frequency of the "4-phase output signals" - is divided. Put differently, the claimed frequency division is applied to the *output* signal of the phase interpolator and not to its *input* signals as is the case in D4.

Consequently, the subject-matter of claim 1 of this auxiliary request is held to be novel over D4 (Article 54 EPC).

3.1.4 As regards the use of a frequency divider in the claimed circuit, the present application as filed indicates that this enables the receiver timing circuit in question to cover a wide range of operation frequencies and thus generate an accurate, high-speed timing signal without jitter (cf. page 51, line 31 to page 52, line 5 in conjunction with Fig. 50). However, as to the additional technical effect achieved by the

specific *location* of the frequency divider according to the above distinguishing feature, the present application is completely silent. At the oral proceedings before the board, the appellant argued that the claimed location of the frequency divider might be beneficial in view of the layout of the circuit. The board however considers this argument to be speculative and thus not plausible. Moreover, the application does not provide any indication that the layout would lead to a possible surprising benefit or bonus effect obtained by a different positioning of the frequency divider. Rather, the board holds that the above effect, i.e. increasing the range of available operation frequencies, is achieved independently of the location of the frequency divider within the circuit in question. This is due to the fact that the overall signal-specific result of incorporating such a frequency divider - whether *first* dividing the frequency of the incoming clock signal and *then* interpolating its corresponding phases (as in D4) or the other way round (as claimed) - is considered to be the same, whilst the choice of one of those two options is based solely on circuit-implementation constraints. In view of the above, the board finds that the distinguishing feature is no more than an obvious alternative solution to the problem of covering a wider range of operation frequencies by the DLL-based timing circuit according to D4.

3.1.5 Accordingly, the subject-matter of claim 1 of this auxiliary request does not involve an inventive step having regard to D4 and the skilled person's common general knowledge.

3.2 In conclusion, the second auxiliary request is not allowable under Article 56 EPC.

4. THIRD AUXILIARY REQUEST

Claim 1 of this request differs from that of the second auxiliary request basically in that it no longer includes feature h), i.e. omits the limitation to a DLL-based circuit, and further specifies that the phase controller includes

i) a phase comparison circuit arranged to compare the phase of the second timing signal with the phase of an external clock signal supplied externally of the timing signal generator;
j) an up/down counter connected to an output of the phase comparison circuit for providing an output signal to control the phase of the first timing signal.

Feature i) is supported e.g. by claim 61 and Figure 55 of the present (and parent) application as originally filed.

4.1 Articles 123(2) and 76(1) EPC

As to new feature j) relating to the sixth embodiment of the present application, the present (and the parent) application as originally filed states at page 55, lines 23-36:

"... If the phase of the internal clock signal (second timing signal) CKin is behind the phase of the external clock signal CKe, feedback control through the up-down counter 3022 is carried out to reduce the phase delay of a phase interpolator

3012. If the phase of the signal CKin is ahead of the phase of the signal CKe, the feedback control through the up-down counter 3022 is carried out to increase the phase delay of the phase interpolator 3012. In more detail, the up-down counter 3022 integrates the up signal UP or down signal DW provided by the phase comparator 3021 according to phase advance or delay and controls the phase of the phase interpolator 3012 according to a digital value of the integration."

Feature j), however, merely indicates, in a quite general manner, that the phase of the first timing signal is controlled by an output signal provided by an up/down counter, without saying how such control is actually conducted based on the description as originally filed. Therefore, the board holds that the subject-matter of present claim 1 amounts to an inadmissible generalisation of the original content, contrary to Articles 123(2) and 76(1) EPC.

4.2 Article 52(1) EPC: novelty and inventive step

4.2.1 The feature analysis and the observations on the distinguishing features set out in point 3.1 above as regards the second auxiliary request apply *mutatis mutandis* to claim 1 of this auxiliary request.

4.2.2 Furthermore and notwithstanding the objections under Articles 123(2) and 76(1) EPC raised in point 4.1 above, the board notes that the DLL circuit of D4 also makes use of a unit ("PHASE DETECT" in Figure 1), which is obviously supposed to compare the phase of the timing circuit's output clock (i.e. "RCLK") with that of an external clock signal ("EXTCLK"), and another unit ("CHG PUMP" in Figure 1), connected to the former

unit, which controls the phase (via control signal "V_C" in Figure 1) of the phase interpolator's output signal (see also first page, right-hand column, first to third paragraphs in conjunction with Figure 5). Thus, in the absence of a more specific definition of an "external clock signal" and the type of the required phase control in present claim 1, the corresponding teaching of D4 is believed to perfectly fall within the terms of features i) and j) of claim 1. It is also apparent to the board that D2, directed to a PLL-based timing circuit, likewise demonstrates a phase control loop made up of a phase comparator ("Input Sampler") and an "Up/Down Counter" (see D2, Figure 2) for the same purpose as in the present invention. This is taken as further confirmation of the board's finding that features i) and j) cannot render the underlying subject-matter inventive.

4.2.3 In view of the above, the subject-matter of claim 1 of this auxiliary request, besides comprising inadmissible amendments, does not involve an inventive step having regard to D4 and the skilled person's common general knowledge (Article 56 EPC).

4.3 In summary, the third auxiliary request is not allowable under Articles 123(2), 76(1) and 56 EPC.

Order

For these reasons it is decided that:

The appeal is dismissed.

The Registrar: The Chair:

K. Götz-Wein A. Ritzka

Decision electronically authenticated