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**Datasheet for the decision  
of 13 October 2017**

**Case Number:** T 0130/13 - 3.4.03

**Application Number:** 02702140.1

**Publication Number:** 1444704

**IPC:** H01C7/06, H01C7/00

**Language of the proceedings:** EN

**Title of invention:**  
SURGE CURRENT CHIP RESISTOR

**Applicant:**  
Vishay Intertechnology, Inc.

**Headword:**

**Relevant legal provisions:**

EPC 1973 Art. 54(1), 54(2)  
EPC R. 137(5)  
RPBA Art. 12(4)

**Keyword:**

Novelty - (no)  
Request filed with grounds for appeal - request identical to  
request not admitted in first instance proceedings  
Reimbursement of appeal fee - (no)

**Decisions cited:**

**Catchword:**



**Beschwerdekammern**  
**Boards of Appeal**  
**Chambres de recours**

Boards of Appeal of the  
European Patent Office  
Richard-Reitzner-Allee 8  
85540 Haar  
GERMANY  
Tel. +49 (0)89 2399-0  
Fax +49 (0)89 2399-4465

Case Number: T 0130/13 - 3.4.03

**D E C I S I O N**  
**of Technical Board of Appeal 3.4.03**  
**of 13 October 2017**

**Appellant:** Vishay Intertechnology, Inc.  
(Applicant) 63 Lincoln Highway  
Malvern, PA 19355 (US)

**Representative:** Plaçais, Jean Yves  
Cabinet Netter  
36, avenue Hoche  
75008 Paris (FR)

**Decision under appeal:** **Decision of the Examining Division of the  
European Patent Office posted on 9 August 2012  
refusing European patent application No.  
02702140.1 pursuant to Article 97(2) EPC.**

**Composition of the Board:**

**Chairman** G. Eliasson  
**Members:** M. Stenger  
C. Schmidt

## **Summary of Facts and Submissions**

- I. The appeal concerns the decision of the examining division to refuse European patent application No. 02702140 for lack of novelty according to Article 54(1) and (2) of claim 1 of the main request, filed with letter dated 26 May 2010. Auxiliary requests 1 to 5 filed 14 May 2012 were not admitted under Rule 137(5) EPC as relating to non-searched subject-matter.
- II. The appellant requests that the decision under appeal be set aside and that a patent be granted in the version filed with letter dated 26 May 2010 and as refused by the examining division (main request), or alternatively on the basis of one of auxiliary requests 1 to 6, all filed with the grounds for appeal. Further, the appellant requests the reimbursement of the appeal fee.
- III. It is referred to the following documents:  
D1: JPH-A-0590003 cited by the examining division  
D1c: human translation of document D1 into English, provided by the Board
- IV. In a communication annexed to the summons to oral proceedings, the Board expressed its preliminary opinion that the application according to the main request and the first and second auxiliary request filed with the grounds for appeal did not meet the requirements of Article 54 EPC in view of documents D1/D1c. A copy of D1c was provided to the appellant by the Board to the appellant.  
The Board further expressed its preliminary opinion that auxiliary requests 3 to 6 were not to be admitted according to Article 12(4) RPBoA and that the decision of the examining division was sufficiently reasoned.

No further requests or arguments were received from the appellant. With letter of 12 October 2017, the appellant informed the Board that it would not be attending the oral proceedings. Oral proceedings were held in the absence of the appellant.

V. Claim 1 of the main request has the following wording:

*A chip resistor (20) being symmetrical to allow for tolerating higher instantaneous pulsed power and direct loading to a pick-and-place machine without concern for top-bottom orientation, comprising:  
a substrate (14) having opposite parallel symmetrical top (24) and bottom (26) surfaces, and a central longitudinal plane of symmetry;  
separate and spaced first (12) and second (22) resistive layers on the top (24) and bottom (26) surfaces, respectively, electrically connected in parallel to each other;  
the top (24) and bottom (26) surfaces of the substrate (14) being symmetrically located with respect to and equidistant from the central longitudinal plane;  
first and second terminals (16) for surface mounting, each terminal (16) being electrically connected to the first (12) and second (22) resistive layers, the terminals (16) being substantially symmetrical about the central longitudinal plane;  
characterized in that  
the first resistive layer (12) and the second resistive layer (22) each have an associated area, wherein the first resistive layer (12) area is substantially equal and symmetrical about the central longitudinal plane to the second resistive layer (22) area so that when electrical current passes through the symmetrical resistive layer areas, a temperature distribution*

*within the substrate (14) will be substantially symmetrical about the central longitudinal plane of the substrate (14) eliminating thermal bending thereof, and such that the chip resistor (20) with both resistive layers (12, 22) tolerates higher instantaneous pulsed power than either layer could provide separately and individually; and in that the substrate (14), resistive layers (12,22) and terminals (16) are symmetrical about the central longitudinal plane to allow for direct loading to the pick-and-place machine without concern for top-bottom orientation.*

- VI. Claim 1 of the first auxiliary request differs from claim 1 of the main request in substance in that
  - the chip resistor is explicitly defined to be **for pulse loading applications.**
  
- VII. Claim 1 of the second auxiliary request is identical to claim 1 of the first auxiliary request.
  
- VIII. Claim 1 of the third auxiliary request differs from the claim 1 of the first auxiliary request in that
  - **the first and second terminals and the first and second resistive layers are in direct contact with, and completely encase, the surfaces of the substrate.**
  
- IX. Claim 1 of the fourth auxiliary request differs from claim 1 of the first auxiliary request in that
  - **each terminal has a larger diameter portion and a smaller diameter portion extending over a portion of the top (24) surface of the substrate,**
  - **each terminal further having a larger diameter portion and a smaller diameter portion extending over a portion of the bottom (26) surface of the substrate;**and in that

- the first resistive layer extends at least partially over the smaller diameter portion of the first terminal, and the second resistive layer extends at least partially over the smaller diameter portion of the second terminal.

X. Claim 1 of the fifth auxiliary request differs from the claim 1 of the first auxiliary request in that

- each terminal has a step portion extending over a portion of the top (24) surface of the substrate,
- each terminal further having a step portion extending over a portion of the bottom (26) surface of the substrate; and in that
  - the first resistive layer extends at least partially over the step portion of the first terminal, and the second resistive layer extends at least partially over the step portion of the second terminal, whereby
    - the first and second terminals and the first and second resistive layers are in direct contact with, and completely encase, the surfaces of the substrate.

XI. Claim 1 of the sixth auxiliary request differs from claim 1 of the first auxiliary request in that

- each terminal has a thicker and a thinner portion extending over a portion of the top (24) surface of the substrate,
- each terminal further having a thicker and a thinner portion extending over a portion of the bottom (26) surface of the substrate; and in that
  - the first resistive layer extends at least partially over the thinner portion of the first terminal, and has a thickness lower than that of the thicker portion of the second terminal, whereby

- **the first and second terminals and the first and second resistive layers are in direct contact with, and completely encase, the surfaces of the substrate.**

XII. The arguments of the applicant, as far as they are relevant for the present decision, may be summarized as follows.

A mixture of several embodiments should not be relied upon when assessing novelty.

Further, the resistor of D1/D1c did not achieve all the effects the resistor according to the application achieved and D1/D1c did not disclose symmetry as required by the independent claim of the application. In addition, the terminals of D1/D1c were different from the ones defined in the independent claim. Furthermore, the chip resistor disclosed in D1/D1c was not suitable for pulse loading applications.

### **Reasons for the Decision**

1. Novelty of claim 1 of the main request, Article 54(1) and 54(2) EPC 1973

1.1 Feature analysis with regard to document D1/D1c

Document D1/D1c discloses a chip resistor being symmetrical (see figure 1 and [1], *square chip resistor*) comprising:

- a) a substrate 1 having opposite parallel symmetrical top and bottom surfaces and a central longitudinal plane of symmetry (see figure 1);
- b) separate and spaced first and second resistive layers 2, 2A on the top and bottom surfaces, respectively, electrically connected in parallel to each other (figure 1 and [7]),



- c) the top and bottom surfaces of the substrate being symmetrically located with respect to and equidistant from the central longitudinal plane (figure 1),
- d) first and second terminals 5, 5A suitable for surface mounting (figure 1), each terminal being electrically connected to the first and second resistive layers 2, 2A (via surface electrodes 4A, 4B, 4C, 4D; see [9] and figure 1), the terminals 5, 5A being substantially symmetrical about the central longitudinal plane (figure 1),
- e) the first resistive layer 2 and the second resistive layer 2A each have an associated area, wherein the first resistive layer area is substantially equal and symmetrical about the central longitudinal plane to the second resistive layer area (see figure 1).

Further, the resistances of the two resistive layers are equal according to  $D1/D1c$  (see [12], *resistance value of the two resistance materials are equal*). This automatically leads to a substantially symmetrical temperature distribution within the substrate about the central longitudinal plane of the substrate when electrical current passes through the resistive layers 2, 2A connected in parallel by the terminals 5, 5A (see [9]).

## 1.2 Discussion of the arguments of the appellant

### 1.2.1 Document D1/D1c

The appellant argued that a mixture of several embodiments should not be relied upon when assessing novelty (part II.B.2 Additional remarks of the grounds for appeal, pages 16 and 17).

The Board agrees, and the reasoning provided above is in conformity with this approach.

In the present case, paragraphs 1 to 7 and 12 of document D1/D1c concern the invention in general, as argued by the appellant, thus relating to both working examples/embodiments comprised in D1/D1c (see grounds for appeal, page 17, second paragraph).

Paragraphs 8 and 9 as well as figure 1 relate to the first working example/embodiment only.

Thus, paragraphs 1 to 9 and 12 as well as figure 1 can be considered together for assessing novelty, as reasoned above.

#### 1.2.2 Technical effects achieved / symmetry

The appellant argued that D1/D1c did not *explicitly* mention all the effects that, according to the description, were achieved by the chip resistor of the application (see grounds of appeal, e.g., page 9, fourth paragraph from the bottom, and page 13, third paragraph from the bottom).

The Board notes that some of these effects are also mentioned in claim 1.

However, in the view of the Board, the chip resistor of D1/D1c would also *unavoidably* achieve, by means of its structural and functional features, the effects of

- tolerating higher instantaneous pulsed power (lines 3 to 4 of claim 1); by means of the same mechanism as explained in the application on page 5, line 25 to page 6, line 24,

- tolerating higher instantaneous pulsed power than either layer could provide separately and individually (lines 22 to 23 of claim 1); namely a doubling (see again page 5, line 25 to page 6, line 24 of the application),

- eliminating thermal bending of the substrate (line 21 of claim 1); this is implied by the symmetrical temperature distribution of the resistor of D1/D1c,

and

- allowing direct loading to a pick-and-place machine without concern for top-bottom orientation to the same extent as the chip resistor according to claim 1 of the main request (lines 4 to 5 and 24 to 26 of claim 1); since the resistor of D1/D1c including the terminals 5, 5A is as symmetric about the center longitudinal plane as the one in figure 2 of the application.

### 1.2.3 Terminals

The appellant moreover argued with respect to novelty that D1 did not disclose the same terminals as claim 1. These arguments correspond to the ones brought forward during the examination phase (see grounds for appeal, page 15, part II. B. 1. and page 18, part III.).

However, the terminals 5, 5A of D1/D1c are each electrically connected to both resistive layers via surface electrodes 4A, 4B, 4C, 4D. This corresponds to what is defined in claim 1.

### 1.3 Conclusion

Thus, the chip resistor disclosed in document D1/D1c as the first working example, including the features common to all working examples of D1/D1c, exhibits all the structural and functional features of claim 1 of the main request either explicitly or implicitly. Consequently, it also achieves the effects mentioned in that claim.

Hence, the subject-matter of claim 1 of the main request is not new within the meaning of Article 54(1) and (2) EPC.

2. Novelty of claim 1 of the first auxiliary request, Article 54(1) and 54(2) EPC 1973

Claim 1 of the first auxiliary request differs from claim 1 of the main request in that the chip resistor is further explicitly defined to be suitable **for pulse loading applications**.

The appellant argued that the chip resistor of D1 was not suitable for pulse loading applications.

Document D1/D1c aims at providing chip resistors with optimized power capacity with regard to their size ([12]). The power capacity mentioned may well be a steady-state power capacity, as argued by the appellant. Even if that were the case, however, this would not render these resistors *unsuitable* for use in pulse load applications (contrary to the arguments of the appellant in part III. A. of the grounds for appeal), for the reason that there is no generally accepted definition of a *pulse load application* in terms of pulse power, duration and frequency. The application does not contain such a definition, either.

Instead, the suitability of any resistor for a given pulse load application depends only on the power, duration and frequency of the pulses actually occurring in that given application.

Therefore, the additional feature of claim 1 of the first auxiliary request does not confer any additional restriction to the claimed resistor.

Thus, the subject-matter of claim 1 of the first auxiliary request is not new, either.

3. Claim 1 of the second auxiliary request, Article 54(1) and 54(2) EPC 1973

Claim 1 of the second auxiliary request is identical to claim 1 of the first auxiliary request, contrary to what the appellant indicated in section B on page 2 of the grounds for appeal.

Consequently, the subject-matter of claim 1 of the present second auxiliary request is not new, either.

4. Auxiliary requests three to six, Article 12(4) RPBoA

Auxiliary requests three to six correspond in substance to auxiliary requests two to five on which the contested decision was based, as argued by the appellant (see pages 2 and 3 of the grounds for appeal). These requests were not admitted by the Examining Division according to Rule 137(5) EPC.

The additional features of auxiliary requests three to six relate to details of the structure of the terminals. These additional features were neither part of the original claim set nor defined anywhere in the original description. They can (if at all) only be deduced from original figure 2.

Further, as pointed out to the appellant in the communication annexed to the summons to oral proceedings (see section 8.), the Board can not see any contribution of the specific structure of the terminals of figure 2 to the general concept of the original claim set of making prior art resistors more tolerant to higher instantaneous pulsed power.

The Board notes that the appellant did not contest this finding.

Thus, the Board is satisfied that the Examining Division applied Rule 137(5) EPC correctly. Consequently, the Board does not admit auxiliary requests three to six according to Article 12(4) RPBoA.

5. Alleged procedural violation/requested reimbursement of the appeal fee

The appellant requested reimbursement of the appeal fee because the decision was not sufficiently reasoned, resulting in a procedural violation.

The Board notes that a reimbursement of the appeal fee according to Rule 103(1)a) is only possible if the Board deems the appeal allowable, which does not apply to the present case.

Irrespective of that, the Board does not concur with the appellant that the decision of the examining division was not sufficiently reasoned resulting in a substantial procedural violation, as set out in detail in the communication annexed to the summons to oral proceedings in section 9.

## **Order**

### **For these reasons it is decided that:**

The appeal is dismissed.

The request for reimbursement of the appeal fee is refused.

The Registrar:

The Chairman:



L. Malécot-Grob

G. Eliasson

Decision electronically authenticated